N. Ramasubramanian
Rajeswari Sridhar
M. Sridevi
M. Brindha
B. Shameedha Begum (Eds)

Computer Science & Information Technology

First International Conference on Secure Reconfigurable Architectures & Intelligent Computing (SRAIC 2019)
November 28 ~ 30, 2019, Tiruchirappalli, India

AIRCC Publishing Corporation

Volume Editors

N. Ramasubramanian
Professor, NIT, Trichy, India
E-mail: nrs@nitt.edu

Rajeswari Sridhar
Associate Professor, NIT, Trichy, India
E-mail: srajeswari@nitt.edu

M. Sridevi
Assistant Professor, NIT, Trichy, India
E-mail: msridevi@nitt.edu

M. Brindha
Assistant Professor, NIT, Trichy, India
E-mail: brindham@nitt.edu

B. Shameedha Begum
Assistant Professor, NIT, Trichy, India
E-mail: shameedha@nitt.edu

ISSN: 2231 - 5403
ISBN: 978-1-925953-11-4
DOI: 10.5121/csit.2019.91501- 10.5121/csit.2019.91506

Typesetting: Camera-ready by author, data conversion by NnN Net Solutions Private Ltd., Chennai, India

Preface

The First International Conference on Secure Reconfigurable Architecture and Intelligent Computing (SRAIC 2019), November 29th to 30th 2019 with a pre-conference tutorial on November 29th 2019 is being scheduled at Department of Computer Science and Engineering, National Institute of Technology, Tiruchirappalli, INDIA in association with Department of Computer Science and Engineering, Dr. B.R Ambedkar Institute of Technology, sponsored by TEQIP – III and supported by IEEE Computer Society.

The conferences attracted many Indian delegates, presenting a balanced mixture of intellect from the East and from the West. The goal of this conference series is to bring together researchers and practitioners from academia and industry to focus on reconfigurable architectures and intelligent computing leading to new collaborations in these areas. This conference invited potential researchers to contribute to the conference by submitting articles that illustrate research results, projects, survey work and industrial experiences describing significant advances in all areas of reconfigurable architectures and intelligent computing. The conference committee rigorously invited submissions for many months from researchers, scientists, engineers, students and practitioners related to the relevant themes and tracks of the workshop. All the submissions underwent a strenuous peer review process which comprised expert reviewers. These reviewers were selected from a talented pool of Technical Committee members and external reviewers on the basis of their expertise. The papers were then reviewed based on their contributions, technical content, originality and clarity. The entire process, which includes the submission, review and acceptance processes, was done electronically. The extended papers of the conference will be reviewed for possible publication in "International Journal of Society Systems and Science" by Inderscience and "International Journal of Knowledge based organizations" by IGI – Global publishers.

We would like to thank TEQIP – III, IEEE Computer Society, our Director, Deans, the General and Program Chairs, organization staff, the members of the Technical Program Committees, the Tutorial and Keynote speakers, and external reviewers for their excellent and tireless work. We sincerely wish that all attendees benefited scientifically and able to bridge the gap in their research aspects. We the organizers wish that the conference brings together collaboration in the successive years to come by having joint proposals amongst the researchers and industry experts who have gathered here.

N. Ramasubramanian
Rajeswari Sridhar
M. Sridevi
M. Brindha
B. Shameedha Begum

Patron's Message

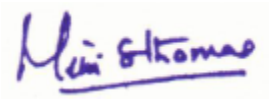
Mini Shaji Thomas,
Director, NIT, Trichy

"I believe in innovation and that the way you get innovation is you fund research and you learn the basic facts" says Bill Gates, CEO, Microsoft Corporation. We believed in this principle and used it to equip the Institution with the finest and latest infrastructure, state of the art libraries and laboratories, a formal and ideal learning environment with committed Faculty and supportive Administrative Staff.

I am happy to see that the Department of Computer Science and Engineering, National Institute of Technology, Trichy is organizing an International Conference for the first on the theme: "Secure Reconfigurable Architecture and Intelligent Computing" sponsored by TEQIP – III and supported by IEEE Computer society from 29th to 30th November 2019 with a pre-conference tutorial on November 28th 2019. I am also glad to learn that many academicians and research scholars especially from Asian continent are expected to participate in this conference.

International Conferences such as these provide an environment for academicians to interact, collaborate and share knowledge derived from their research in the field of Secure Reconfigurable Architecture and Intelligent Computing. I hope this conference would result in active coordination among researchers working in similar areas which would result in creative and innovative technologies leading to new research ideas for the benefit of society. The conference proceedings are published in AIRCC's "Computer Science and Information Technology" series. The extended papers of the conference will be reviewed for possible publication in "International Journal of Society Systems and Science" by Inderscience and "International Journal of Knowledge based organizations" by IGI – Global publishers.

As the Director, it gives me great pride to welcome the conference participants to enjoy their stay and make meaningful contributions that will, I am sure, widen the horizons of Intelligent computing.



(Mini Shaji Thomas)

Convener's Message

N. Ramasubramanian
Professor, NIT, Trichy.

"Understand well as I may, my comprehension can only be an infinitesimal fraction of all I want to understand" says English Mathematician and first computer programmer Ada Lovelace. These words made me believe that we need a common platform where researchers and students can share and exchange their ideas. We at the Department of Computer Science and Engineering, have just ventured into conducting International and National Conferences to share and impart knowledge to researchers and students.

In this direction, it gives me much pleasure to witness another major milestone for the department, to organize and conduct the First International Conference on Secure Reconfigurable Architecture and Intelligent Computing (SRAIC 2019), from 29th to 30th November 2019 with a pre-conference tutorial on November 28th 2019. The realization of success in organizing and hosting the conference goes a long way to not only showcase SRAIC as a major hub of CS research but also helps in transforming the Department of Computer Science and Engineering into a rich reservoir of research activity.

I wish, on behalf of SRAIC, to take this opportunity to thank all those who contributed in one way or other towards the success of the conference. My special thanks to the Tutorial Speakers and Keynote speakers who have participated in person and through video conferencing. I particularly appreciate the various paper presenters who have submitted well-researched and highly relevant presentations, and the SRAIC organizing committees for the long hours spent to ensure the success of the conference.

My heartfelt thanks to AIRCC for having agreed to publish the conference proceedings in their Computer Science and Information Technology Conference proceedings. My sincere thanks also goes to the conference sponsors, for the very generous assistance towards the organization of the conference. Continued consultations and cooperation of all parties mentioned above ensure that the first international conference in the Department of Computer Science and Engineering is indeed a remarkable success. Thank you once again and I encourage you to maintain this working spirit.

The conference program has been designed to provide ample opportunities for researchers to network and to share ideas and information about Secure Reconfigurable Architectures and Intelligent Computing. I hope this conference SRAIC 2019 will be enjoyable, memorable, and productive for participants and I look forward to the technological innovations that result from your networking and discussions.

N. Ramasubramanian

Organizer's Message

Rajeswari Sridhar
Head, CSE Dept, NITT.

"Research is what I'm doing when I don't know what I'm doing" says Wernher von Braun, developer of the rocket technology of Nazi Germany. In addition, I reinstate research and innovation are necessary and essential components of a knowledgeable and growing society. Research ideas leading to innovative products to serve the society are primary inputs for achieving excellence in Education. The products that are off-springs of the research inputs, work as catalysts in the socio-economic progress of the Institution and in-turn the Country.

With this as a primary concept, National Institute of Technology, Trichy a leading Educational Institution in India, imparts quality education on par with international standards. The aim of National Institute of Technology, Trichy (NITT) is to create world class facilities to support Research and Innovation. To facilitate this support, with great pleasure and enthusiasm we formally announce and cordially invite you to the First International Conference on Secure Reconfigurable Architecture and Intelligent Computing (SRAIC 2019), to be held at National Institute of Technology, Trichy, India, from 29th to 30th November 2019 with a pre-conference tutorial on November 28th 2019.

The theme of the conference is Secure Reconfigurable Architecture and Intelligent Computing with the focus on thrust areas of Computer Science. This innovative educational forum will enable you to advance your knowledge and rewire the contemporaries which will open up new professional contacts amongst the National and International experts in this field. SRAIC 2019 is designed to be an academic feast, with a structured programme in a manner where participants will have ample time to interact after the sessions, which will be enriched by the presence of distinguished International and National Faculty.

With the right vision, right people and programs in the right place, we at the NITT make an attempt of creating the right set of contributions for different disciplines of research. The aim of education at National Institute of Technology, Trichy is to assist the students in developing their intellectual, aesthetic, emotional, moral and spiritual being. We, at NITT, impart futuristic, stress free education and instill high degree of discipline among them thereby setting global standards and making our students think logically and analytically.

I believe SRAIC would help achieve the above-mentioned aspects and I am sure would be a colossal success and bring tributes.

Rajeswari Sridhar

General Chair	Organization
N. Ramasubramanian	National Institute of Technology- Trichy, India
Rajeswari Sridhar	National Institute of Technology- Trichy, India
M. Sridevi	National Institute of Technology- Trichy, India
M. Brindha	National Institute of Technology- Trichy, India
B. Shameedha Begum	National Institute of Technology- Trichy, India

Program Committee Members

S. Selvakumar	Director, IIIT, Una
N. Ramasubramanian	Professor, NIT, Trichy
K. Viswanathan Iyer	NIT, Trichy NIT, Trichy
Leela Velusamy	Professor, NIT, Trichy
Mary Saira Bhanu	Professor, NIT, Trichy
C. Mala	Professor, NIT, Trichy
Rajeswari Sridhar	Associate Professor, NIT, Trichy
Gandadharan G. R.	Associate Professor, NIT, Trichy
Dominc	Associate Professor, NIT, Trichy
M. Sridevi	Assistant Professor, NIT, Trichy
M. Brindha	Assistant Professor, NIT, Trichy
B. Shameedha Begum	Assistant Professor, NIT, Trichy
R. Mohan	Assistant Professor, NIT, Trichy
S. Jaya Nirmala	Assistant Professor, NIT, Trichy
E. Sivasankar	Assistant Professor, NIT, Trichy
Kunwar Singh	Assistant Professor, NIT, Trichy
B. Nithya	Assistant Professor, NIT, Trichy
Santhana Vijayan	Assistant Professor, NIT, Trichy
S. Sangeetha	Assistant Professor, NIT, Trichy
U. Srinivasulu Reddy	Assistant Professor, NIT, Trichy
Alagusundaram	Professor, DBRAIT, Andaman
Harshabardhan S	Assistant Professor, DBRAIT, Andaman

Technical Committee

K. Chandrasekaran	NIT Surathkal
Jaidhar C. D.	NIT Surathkal
G. Deepa	Manipal institute of technology
P. C. Siddalingaswamy	Manipal institute of technology
SRIRAM .G. SANJEEVI	NIT Warangal
Rashmi Ranjan Rout	NIT Warangal
N. Renugadevi	NIT Warangal
Suresh Babu E	NIT Warangal
Noor Mahammad SK	IIITDM Kancheepuram
Sivaselvan B	IIITDM Kancheepuram
Manoj Singh Gaur	MNIT Jaipur
Meenakshi Tripathi	MNIT Jaipur
Arka Prokash Mazumdar	MNIT Jaipur
Ramesh Babu Battula	MNIT Jaipur
Ayan Seal	IIITDM Jabalpur
Pritee Khanna	IIITDM Jabalpur
Mamata Dalui Chakraborty	NIT Durgapur
Saravanan Chandran	NIT Durgapur
Tanmay De	NIT Durgapur
Nanda Dulal Jana	NIT Durgapur
Sandip Karmakar	NIT Durgapur
Goutam Sanyal	NIT Durgapur
Anirban Sarkar	NIT Durgapur
Bibhash Sen	NIT Durgapur
Jayadeep Pati	IIT Ranchi
Sudip Roy	IIT Roorkee
Vijay Bhaskar Semwal	MANIT-Bhopal
Bibhudatta Sahoo	NIT Rourkela
Durga Prasad Mohapatra	NIT Rourkela
Darshan Vishwasrao Medhane	IIIT Pune
TANMOY HAZRA	IIIT Pune
Albert Sunny	IIT Palakkad
Chandra Shekar Laskhminarayanan	IIT Palakkad
Sahely Bhadra	IIT Palakkad
R.S.Yadav	MNNIT Allahabad
Krishn K. Mishra	MNNIT Allahabad
Dushyant Kumar Singh	MNNIT Allahabad
Rajitha B	MNNIT Allahabad
Naveen Kumar	IIIT Vadodara
B. Surendiran	NIT Puducherry
Ansuman Mahapatra	NIT Puducherry
Damodar Reddy Edla	NIT Goa
Veena Thenkanidiyoor	NIT Goa
Keshavamurthy B.N.	NIT Goa

Rajendra Prasath	IIIT Andhra Pradesh
Viswanath Pulabaigari	IIIT Andhra Pradesh
KARTHICK S	NIT Andhra Pradesh
K HIMABINDU	NIT Andhra Pradesh
NAGESH BHATTU SRISTY	NIT Andhra Pradesh
SRILATHA CHEBROLU	NIT Andhra Pradesh
Kaushal Kumar Shukla	IIT Varanasi
Amrita Chaturvedi	IIT Varanasi
Anish Chand	IIIT Chittoor
Balaji Raman	IIIT Chittoor
Prerana Mukherjee	IIIT Chittoor
Rajendra Prasath	IIIT Chittoor
Viswanath Pulabaigari	IIIT Chittoor
T. Veni	NIT Calicut
Arun Raj Kumar P	NIT Calicut
Vasudevan A. R	NIT Calicut
Virender Ranga	NIT Kurukshetra
Maheshwari Prasad Sing,	NIT Patna
Mantosh Biswas	NIT Kurukshetra
Kishore kumar Senapati	Birla Institute of Technology
RAJU BHUKYA	NIT Warangal
Narendran Rajagopalan	NIT Puducherry
Chittaranjan Hota	Birla Institute of Technology & Science, Pilani-Telangana
Rekh Ram Janghel	NIT Raipur
Sanjoy Pratihar	IIIT Kalyani
B. Surendiran	NIT Puducherry
NEENA GOVEAS	Birla Institute of Technology & Science, Pilani-Goa
Krishna Pratap Singh	IIIT Allahabad
B. Vijayakumar	BITS Pilani, Dubai Campus.
PARTHA PAUL	Birla Institute of Technology, Mesra
Sudip Roy	IIT Roorkee
Annappa	NIT- Surathkal
SUDIP KUMAR SAHANA	Birla Institute of Technology, Mesra
Govind P. Gupta	NIT Raipur
Mak Sharma	School of Computing and Digital Technology-Birmingham-United Kingdom
Asif Ekba	IIT Patna
Manish Kumar	IIIT, Jhalwa-Allahabad
K K Shukla	IIT Varanasi
Anurag Singh	NIT-Delhi
Mamata Dalui Chakraborty	NIT-Durgapur
Pradeep Singh	NIT Raipur
Meenakshi D'Souza	IIIT-Bangalore
Sanjay K. Sahay	Birla Institute of Technology & Science, Pilani-Goa
Keshavamurthy B.N.	NIT-Goa
Kabita Thaoroijam	IIIT-Manipur
Sathyanarayana Vollala	IIIT–Naya Raipur

Advisory Committee

Albert Sunny	IIT Palakkad
Chandra Shekar Laskhminarayanan	IIT Palakkad
Sahely Bhadra	IIT Palakkad
Asif Ekbal	IIT Patna
Jayadeep Pati	IIT Ranchi
Sudip Roy	IIT Roorkee
Sudip Roy	IIT Roorkee
Kaushal Kumar Shukla	IIT Varanasi
Amrita Chaturvedi	IIT Varanasi
K K Shukla	IIT Varanasi

Technically Sponsored by

IEEE Computer Society

Technically Sponsored by

TEQIP-III

CODETANTRA

Organized By

First International Conference on Secure Reconfigurable Architectures & Intelligent Computing (SRAIC 2019)

NIT Trichy -National Institute of Technology

TABLE OF CONTENTS

First International Conference on Secure Reconfigurable Architectures & Intelligent Computing (SRAIC 2019)

ANALYSIS OF FAULTS IN AN N-BIT SELF CHECKING REGISTER

T. Shunbaga Pradeepa[1] and S. Uma Maheswari[2]

[1]Assistant Professor, Department of Electronics and Communication Engineering, Coimbatore Institute of Technology, Coimbatore
[2]Professor, Department of Electronics and Communication Engineering, Coimbatore Institute of Technology, Coimbatore

ABSTRACT

Soft errors which are random errors induced by radiations may be produced due to transient faults and upsets in electronic systems. From the survey, it has been observed that the existing error correcting techniques and models have some limitations. The conventionally used error detection method named Triple Modular Redundancy (TMR) method has large overhead which makes it uneconomical. In this paper, the existing techniques like Time Redundancy based error Detection (TRDED) has been implemented and verified for different intervals of errors. It has been observed that only particular errors can be detected and no corrections are done. The modified circuits abbreviated as SETTOFF can be used for Soft Error and Timing Error Tolerant Flip Flop. These circuits which have both error correction and detection has been implemented and verified for different intervals of time. Since the chances of induced errors are increasing, there is a great necessity for developing a technique to provide more reliability and performance. Targeting towards the above features, self-checking register architecture for multi-bit error detection has been proposed and analyzed using Xilinx ISE Simulator for transient fault occurrence and has been analyzed.

KEYWORDS

Transient Fault, Self-checking register, Single Event Upset (SEU), Multi bit error detection, Single Event Transient (SET)

1. INTRODUCTION

Errors that occur randomly are Soft errors. They are induced by radiations that may be produced due to transient faults and upsets in electronic systems. Transient faults occur in 2 different ways. One is Single Event Upset that will change the state value in the storage cell. The other is Single Event Transients which generate transient voltage pulses in combinational gates. Memory elements are easily affected by SETs and sometimes they turn into soft errors. SEUs are a major concern in both dense memory arrays and sequential logic. The SEUs can be protected efficiently by conventional Error Correcting Code (ECC) techniques. But, since ECC is distributed across the entire system, they are not applicable in sequential logic. Therefore, there exists a challenge in achieving efficient error mitigation in general logic. The most widely used safety technique is Triple Modular Redundancy (TMR). This method eliminates errors in general logic. Although TMR is highly reliable, it requires large area which makes it uneconomical for most non-safety-critical electronics. Demands in Technology and customer are pushing performance and energy efficiency. However, the soft errors are becoming a major concern at the same time. To balance these conflicts, it is better to provide a convenient safety method in supporting non-safety-critical electronics. The First contribution of the work is the design and implementation of an error

N. Ramasubramanian et al.(Eds) : SRAIC-2019
pp. 01-17, 2019. © CS & IT-CSCP 2019 DOI: 10.5121/csit.2019.91501

tolerant D flip flop. In this method, to analyze cost-efficient error-tolerance in general logic a new design was done. The design is named Soft Error and Timing Error Tolerant Flip Flop. It is abbreviated as SETTOFF. This design can correct error upsets and detects transient errors. The errors that occur naturally are Timing Errors (TE).

The objective of this work evolves from the great interest in developing a technique to provide a better performing safety method that supports non-safety-critical electronics and in achieving more reliability and performance in detecting and correcting errors due to upsets and transients. Most sequential circuits do not have error correcting capability. So, they are easily induced to soft error especially in case of redundant circuits. If the combinational logic blocks with redundancies are unprotected, it will produce SET pulses which in turn may lead to occurrence of errors. If the redundancy is stable the particle striking can produce SEU as like in latch. So there exists a great need to achieve efficient error mitigation logic. The existing techniques use replication to improve the error tolerance level in any electronic system. But there exists some drawbacks. The techniques covers the errors occurred in the actual circuit but if they occur in the safety replication module those errors are not protected. Those circuits are not checking themselves. It has become essential for Integrated Circuits to have some kind of circuits that detects soft errors as well as timing faults. Such protection is needed for all designs. One such tolerant design is TMR, but this seems to be costly.

Improvement in soft and timing error detection using time redundancy method have been implemented in Lorena Anghel and Michael Nicolaidis [4] based on time redundancy. Lin, M. Zwolinski, and B. Halak [15] have discussed a new architecture for Flip-Flop called SETTOFF which improves circuit performance to radiation hits against the existing ones. But, the cost area and performance are high. Yang Lin et al. has proposed [14] a technique to check circuits by itself for soft error based on SETTOFF. Sheng Lin et al. has proposed [11] circuits based on Schmitt trigger. The circuit uses conventional latch which increases the area consumed. Hsuan-Ming Chou et al. has presented [3] a design to protect from soft error targeting different applications with trade-off in performance, power, and reliability.

The flow of paper is like: Section 1 describing the overview and its related literature survey. Section 2 describes about the triple modular redundancy fault tolerant techniques. Basic idea about transient fault detection is given in Section 3. The study SETTOFF is briefed in Section 4. The architecture of proposed self-checking register is described in Section 5. Section 6 includes the implementation results of this work followed by conclusion in Section 7.

2. ARCHITECTURE OF TRIPLE MODULAR REDUNDANCY

Triple modular redundancy (TMR) is a method adopted in early days to obtain better safety system. The system has a majority voter. It reads data from three duplicate circuits. It then compares for majority of the outputs.

2.1. TMR Systems

TMR is a kind of fault tolerant system that is implemented in most computing system in the form of N modular redundancy. As the value of N is assumed as 3 meaning Tri, it is called Triple Modular Redundancy. This method has three systems performing the same process and the result of the process is taken by considering the majority value of the output. In this if one system is faulty, the other two systems will mask the fault in the system and it will correct the error automatically. The TMR is applicable to many redundant forms and also it is applicable in Error Correction Codes. TMR makes use of three identical and redundant form of the original system to

compute its output. If there are no errors or faults in the systems all the redundant modules will produce the same output. If there are any errors then the outputs will be different.

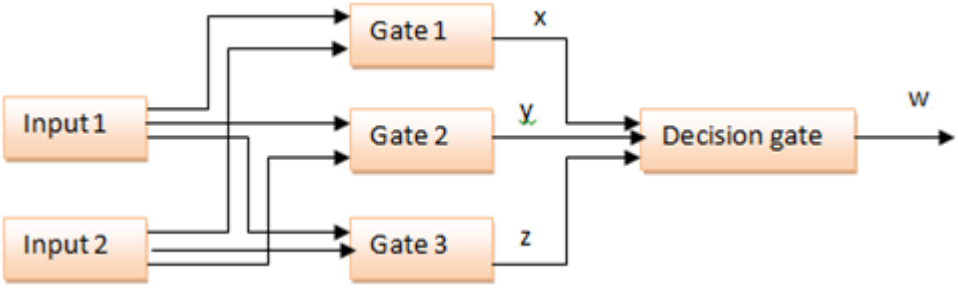


Figure 1. Triple Modular Redundant architecture

The circuit in Figure 1 represents the Triple Modular Redundant architecture where majority logic is used for finding the exact output in the circuit. If the circuits work properly without error, the outputs are same. The outputs will be different if the circuit has any failure. Majority gate is used in the circuit. It will help in finding the actual output. The logic output will be high value if more than two outputs are logic high. The logic output will be a low value if more than two inputs are logic low. The logic equation of the majority gate can be given as in Equation (1) where x, y and z are the inputs and w is the output of the majority gate.

$$w = (xy) \text{ or } (yz) \text{ or } (xz) \quad (1)$$

This has used AND logic as well as OR logic. Essentially the majority logic gate is a voting mechanism.

Consider the following scenarios that might occur in the majority gate. Let's say that logic 1 represents that there is no failure and logic 0 means the system has some failure.

Case (i) if there are no errors in the system, then all three modules will produce an output of 1, and the majority gate also produces a value of 1.

Case (ii) if any failure occurs in one of the modules then it produces an output of 0, but the other two modules are error free and produces an output of 1, the majority gate produces an output of 1. It is seen that even if one of the modules fail the error is masked by the other two modules.

Case (iii) if all the modules are producing an output of 0 then it will be reflected in the majority gate output. Conventionally, a fault-tolerant machine uses replicated elements which are operating parallel.

The TMR may be a robust form of error correction scheme but it doesn't indicate in which module the error has occurred. Also replication of the modules three times increases the hardware size required for fault free implementation. Although TMR is highly reliable, the large area consumption makes it uneconomical for most non-safety-critical electronics applications. There are other techniques to achieve cheaper solutions, but they are normally less reliable than TMR.

3. TIME REDUNDANCY BASED ERROR DETECTION

The Time Redundancy Based Detection abbreviated as TRD technique detects SET. It is found at the input of a flip flop by comparing the sampled data at two time instants delayed by delta. The error tolerance overhead of TRD is small as there is no duplication done. An SET pulse whose width is not greater than delta can be detected since it doesn't overlap the two time instances. The

TRD technique will detect timing errors that are caused due to previous logic modules, and the SEU occurring in the flip flop before the second time instance. Since the triplication is done the correct value is easily identified. The hardware redundancy achieves good tolerance in transient fault detection. The system is costly as because it is not suitable in commodity products. So, an alternate method of injecting transient faults is used.

3.1. Operating Principle

SET occurring in logic blocks can be corrected by themselves within a short period of time. They also recover automatically. There is no hardware duplication in the technique shown in Figure 2. TRD can detect SET for an the input of the flip flop whose pulse width can be maximum of Dtr <= delta - Dsetup - Dcomp,

where Dsetup is the time for setup of the error flip flop and Dcomp is comparator delay. The same SET if captured by the main flip flop at a time interval of t0, can be recovered at

t0 + δ - Dsetup - Dcomp , whereas the comparator will produce an error output when the inputs are not consistent.

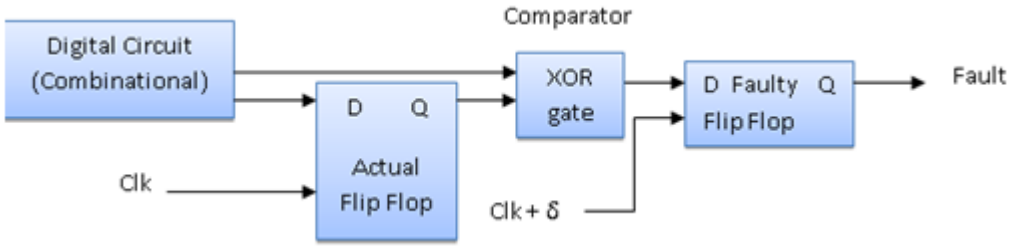


Figure 2. TRD Flip Flop

When the delay of TE is not greater than Dtr the fault can be detected and corrected for the input D. This architecture can also detect SEU in the main flip flop from t0 to t0 + δ − Dsetup − Dcomp, which is called the TRD interval. TRD can detect but cannot correct errors. SEU in the main flip flop but outside the TRD interval cannot be detected by this module.

4. ERROR TOLERANT FLIP FLOP FOR SOFT AND TIMING ERROR

SETTOFF [15] overcomes the drawbacks of previous techniques and achieves a higher error-tolerance with lower cost. The errors occurring during a write cycle of SETTOFF are detected and are easily corrected. Other errors which corrupt the data stored in SETTOFF are detected and corrected internally. If these errors are found to occur during a hold cycle, it is difficult to find it. The SETTOFF architecture is shown in Figure 3. The main flip flop is a normal flip flop. The last stage element has a pair of inverters. These inverters drive the output of the flip flop. They are now replaced by a correction XOR-gate. Therefore, in normal operation, the output variable Q is inverse of actual node N. The TRD interval of the clock phases high and low are as shown in Figure 4.

Module I is an adapted TRD architecture. It contains a XOR gate for detection and delayed clock is used to drive faulty Flip-Flop. The delay element δ is the sum of Dhclk (period of the high clock phase), Ddxor (delay of XOR-gate detector) and Dsetup (faulty Flip-Flop set up time). The TRD interval is equal to δ - Ddxor - Dsetup= Dhclk. During the write cycle of the main flip flop the error flip flop is enabled. Module I detect the type of error based on interval of TRD. It will be detected as SET if the L1 stage has a pulse width which is not greater than Dhclk. It detects as

timing error when a delay of module is not more than Dhclk and it detects as SEU if there is a change of state in node N during Dhclk. The error flip flop generates a signal when error is detected. Module I detects errors occurring during the write operation. Module II detects and corrects SEU occurring during the other half of the clock phase. Transition detector is present which monitors the internal node N. There is an XOR-gate which is used for correction purpose. Those SEU that corrupt the last stage of actual flip flop are considered, whereas others are masked. When TD is disabled the output (Error_SEU_bar) will remain high. This indicates errors are not present. The correction XOR-gate inverts N to Q.

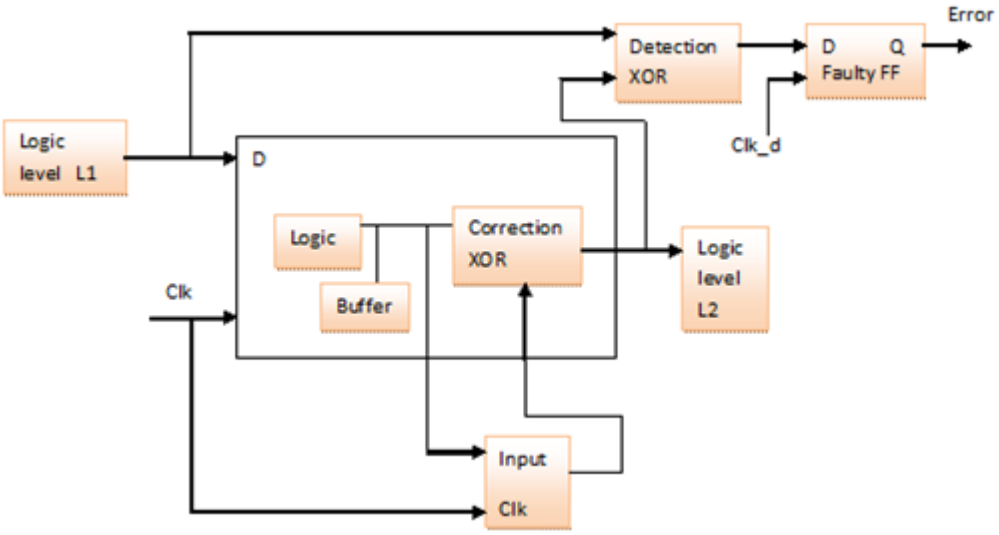


Figure 3. SETTOF Architecture

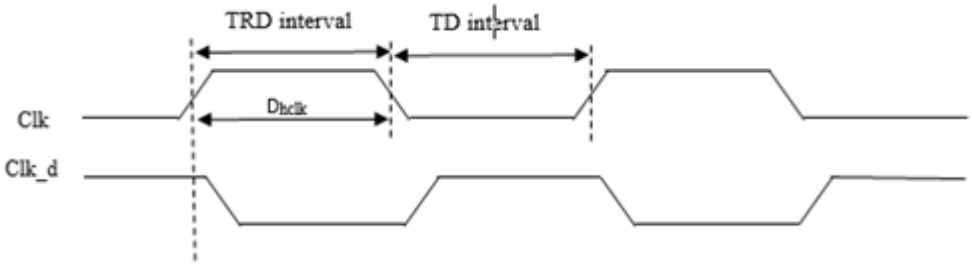


Figure 4. SETTOFF's TRD and TD interval [13]

To further illustrate this, consider the three conditions shown in Figure.5.

Condition (i) Consider that SEU is correcting while writing in the flip flop, it will capture the input and checks if there have been any change in the bit value in the rising edge of the clock. Also, Error_SEU_bar is asserted and make the correction XOR-gate invert N to Q.

Condition (ii) the next case is when SEU is correcting when it is holding the data. Flip flop typically holds any of the two architectures either multiplexer based architecture or the clock gating based architecture. In a multiplexer based architecture, the input is in a hold cycle if the Flip-Flop captures an error, but the output Q is selected by a multiplexer to feed back into the input D. The Flip-Flop then captures the corrected Q to overwrite the SEU stored in the last inverter pair during the hold cycle. Error_SEU_bar is set to 1 at the same time.

Condition (iii) in a clock-gating-based architecture, the driving clock in the flip flop is gated where there is no input capturing in hold cycle. The bit-Flip error remains at node N. This ensures that the flip of the bit remains corrected at Q. The process generates a correction glitch in the output of SETTOFF due to the delay in the propagation of the TD. The width of the fault is very small. This is due to the fact that the TD is relatively fast and the correction process is incorporated in the flip flop architecture. Even if the correction fault propagates, it is not fatal. SETTOFF has the ability of both error detection and correction. Some cases of errors have been detected and corrected using the modified D Flip Flop. SETTOFF can efficiently tolerate error upsets and timing errors.

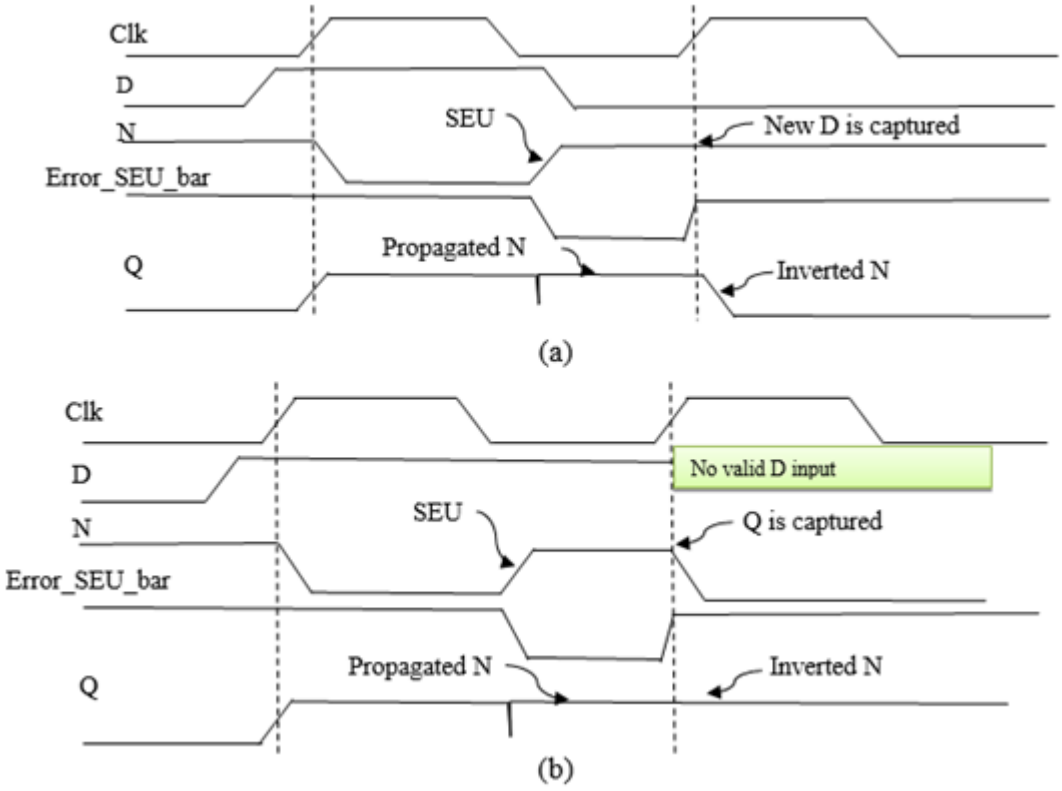


Figure 5. SETTOFF Operating principle [13]

5. SELF- CHECKING ERROR TOLERANT REGISTER

Self-checking capability is not available in almost all pipeline protection techniques and hence they are easily affected by soft errors. The probability that the circuit is affected is determined by the area and size of the redundancies. But, the charge is used to determine the circuit's vulnerability. If the redundant modules are unprotected then ECC is needed at appropriate stages. The proposed technique takes has a self checking method implemented in register architecture.

Then bit self checking register [14] is shown in Figure 6. It has n SETTOFF blocks which are shared with a self checker block. It also has a glitch filter (GF), and also includes a TD checker. The errors are combined together and are stored in the flip flop. As Module II is affected the error affects the output of a TD. The presence of self checker makes the process of monitoring the outputs. It then detects errors in Module II when there are any faulty transitions at these outputs.

The outputs of each bit are connected to the parity checker through n input XOR tree. The output is logic high when a fault is detected. This fault detection is made to pass through the Glitch

Filter. These transients may in turn induce glitches in the parity checker [16] output. The glitches are filtered and prevent them from passing. The errors that are detected can also be corrected.

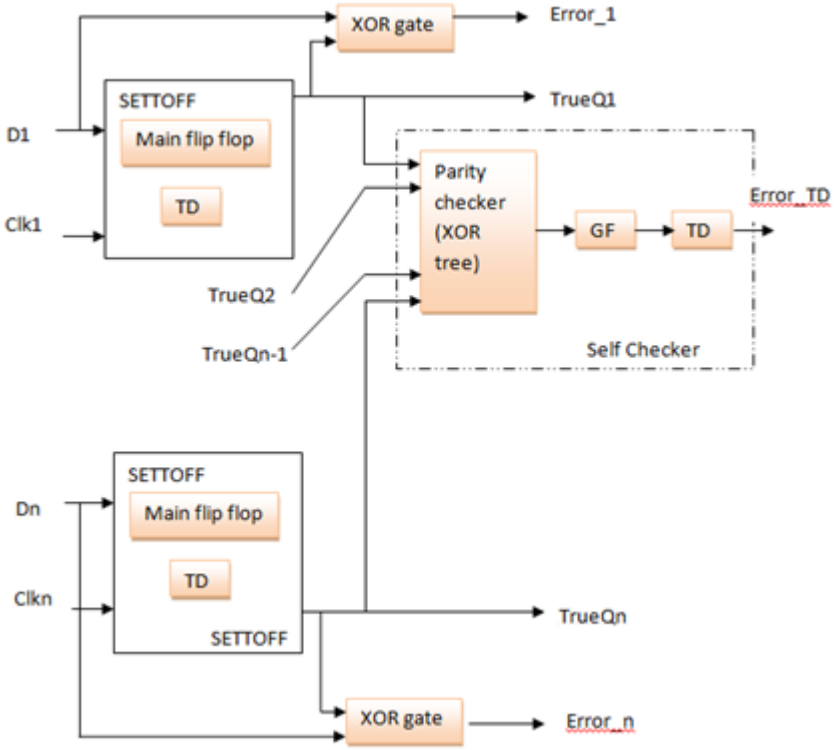


Figure 6. n-bit self-checking register

5.1. Proposed Self-Checking Register for Multi-Bit Error Detection

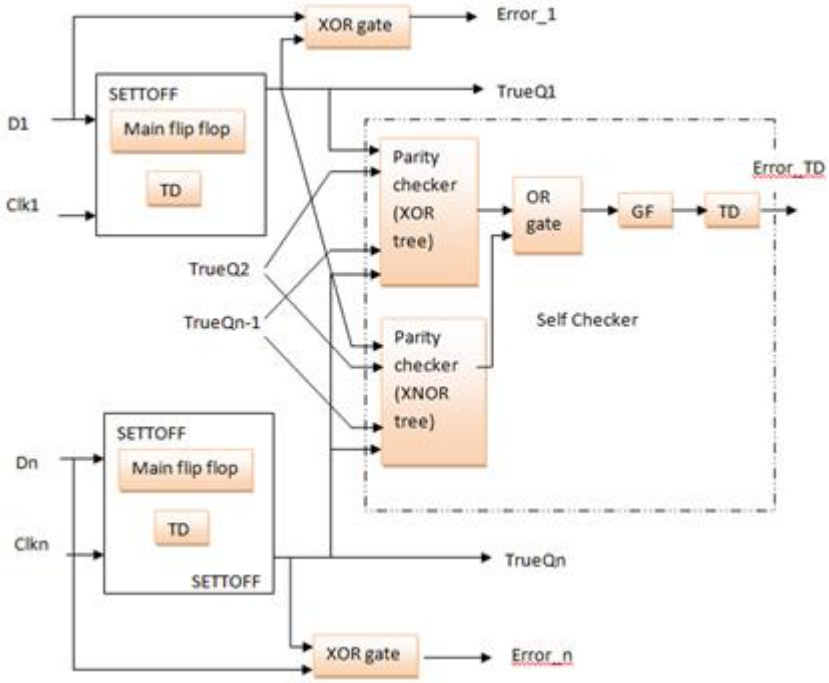


Figure 7. Proposed n-bit self-checking register with multi-bit error detection

The Figure 7 gives the n bit self-checking register architecture block. It has n SETTOFF and also has a self checking mechanism inbuilt as already in the Figure 6. This modified self checker can detect both odd and even number of soft errors. A self checker which is inbuilt monitors the outputs of all SETTOFF. The presence of parity checker helps in detecting odd number of errors using n input XOR tree. To detect even number of errors an n input XNOR tree is used. If errors are detected, the parity checker circuit generates a change in state. Thus, Self checking register gives more protection in pipeline architectures. The self checker has the capability of monitoring the outputs of each Flip Flops.

6. RESULTS AND DISCUSSIONS

The simulation results obtained in implementing various error tolerant techniques including time redundancy based error detection SETTOFF and the proposed self checking register for pipeline architectures are presented. Error tolerance analysis has been done using Xilinx ISE and Microwind Dsch tool was used for circuit analysis of SETTOFF.

6.1. Error Tolerance Analysis

The discussed error resilient techniques were analyzed for different time intervals of forced errors.

6.1.1. Time Redundancy based Error Detection (TRD)

Figure 8 shows the RTL schematics of the TRD Flip Flop. It consists of an XOR gate with D Flip Flop. The XOR gate acts as the comparator. Comparator generates high value when an error is found.

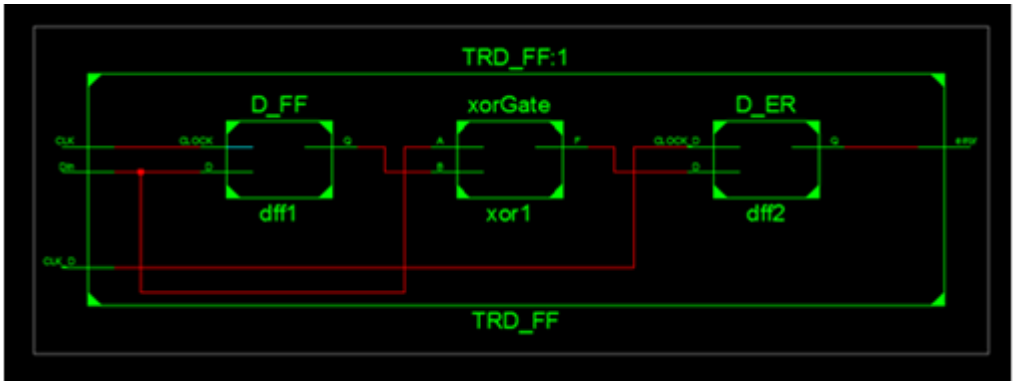


Figure 8. RTL schematics of TRD

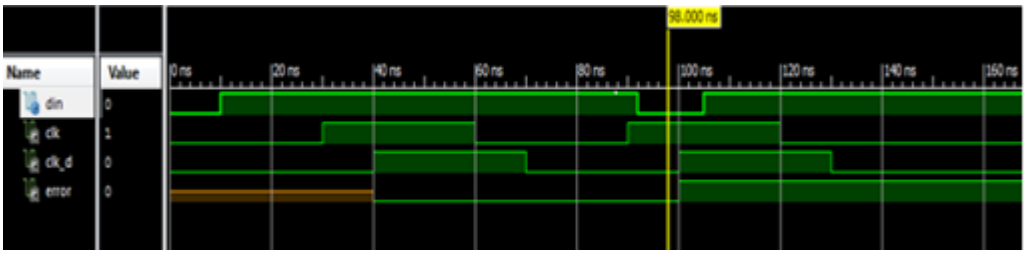


Figure 9. Error occurring from 92 ns to 105 ns

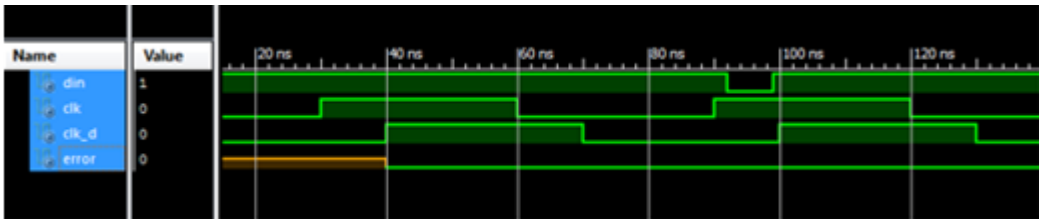


Figure 10. Error occurring from 92 ns to 99 ns

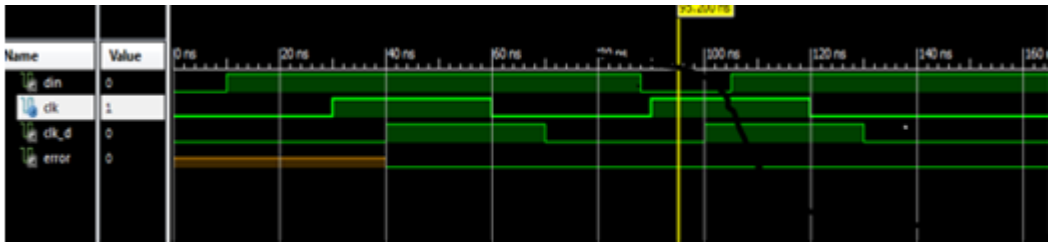


Figure 11. Error occurring from 88ns to 105 ns

Figure 9 to Figure 12 shows the waveforms obtained for different intervals of errors that have been forced on the input Din. Clock period is taken as 60 ns and delay is given to the error flip flop as 10 ns. Since delay of clock transition occurs at 100 ns, the errors occurring as transitions before 90 ns and before 100 ns as well as after 90 ns and after 100 ns have been detected. But upsets which have transitions after 90 ns and before 100 ns are not getting detected. As well as, transitions occurring before 90 ns and after 100 ns are not getting detected.

Table 1. Error tolerance analysis in TRD

S.No	Error type	Inference
1	Captured transients	Output degraded, abided
2	Error upsets (FF)and (TRD)	Output degraded but not abided

Error tolerance analysis of TRD architecture is briefed and given in Table 1 and it shows that captured transients occurring external to the main Flip Flop will be corrupting the output and can be tolerated using the TRD architecture. But error upsets occurring in main Flip Flop and TRD architecture are not getting corrected even though they corrupt the output. So it can be inferred that TRD architecture doesn't have the capability to correct the error upsets occurring in the main Flip Flop.

6.1.2. SETTOFF

RTL schematic of SETTOFF is given in Figure 13. It consists of detection and correction modules for the conventional Flip Flop.

TRD part consists of the detection XOR gate and the error D Flip Flop. Correction part has correction XOR gate and the transition detector. The corrected output is taken from the correction XOR gate and error indication is taken from the TRD part.

The error detection waveforms given in Figure 14 to Figure 16 are same as in TRD architecture. Here clock period is taken as 60 ns and delay is 20 ns.

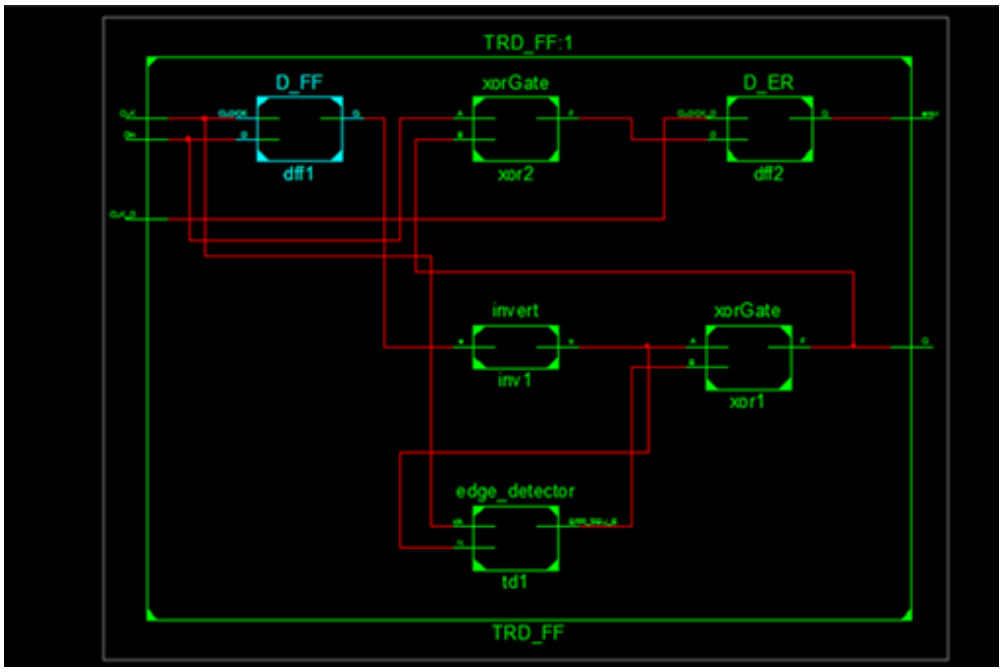


Figure 12. RTL schematic of SETTOFF

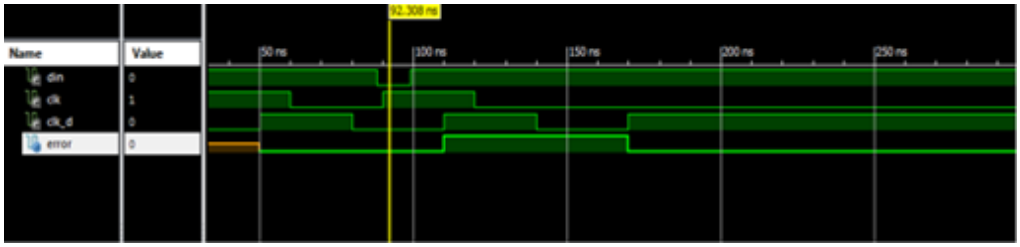


Figure 13. Error occurring from 88 ns to 99 ns

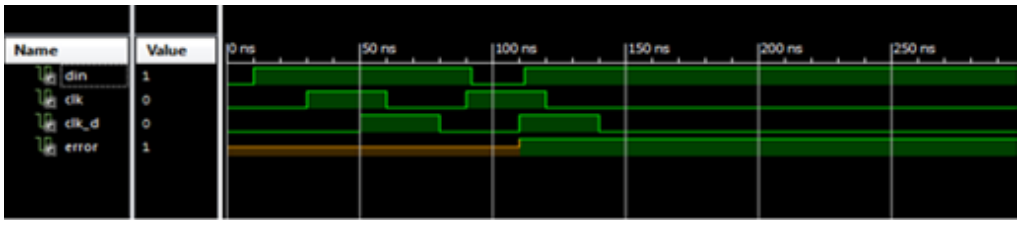


Figure 14. Error occurring from 92 ns to 112 ns

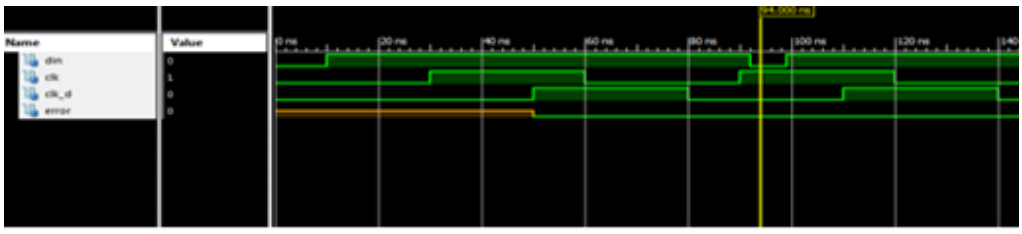


Figure 15. Error occurring from 92 ns to 99 ns

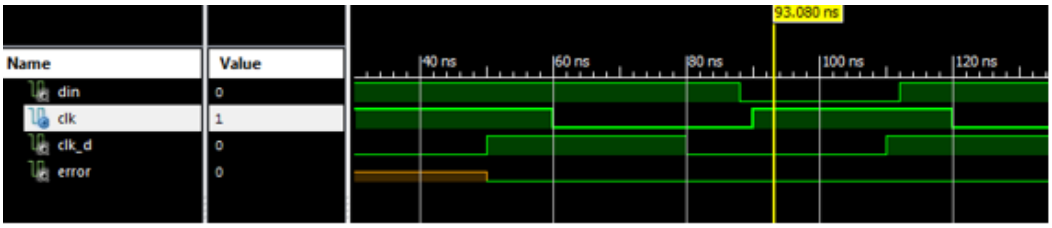


Figure 16. Error occurring from 88 ns to 112 ns

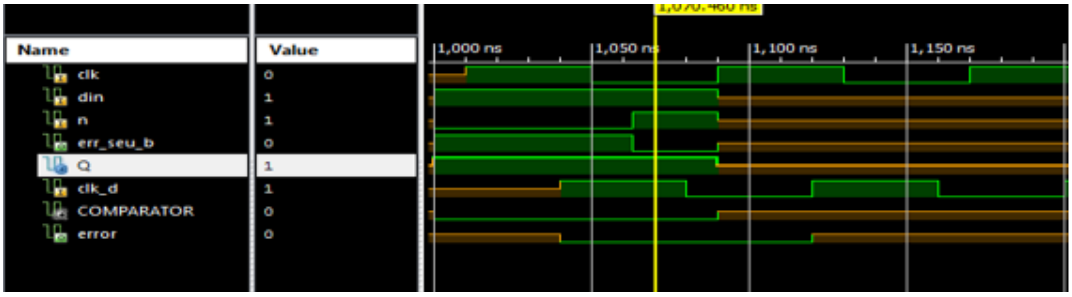


Figure 17. Captured Q value

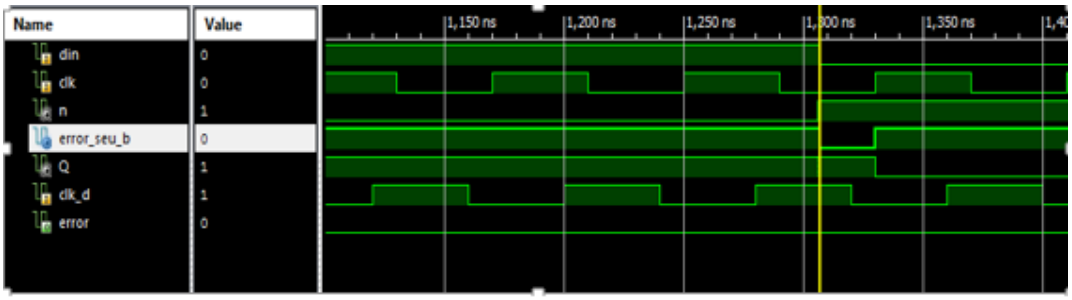


Figure 18. Propagation of n

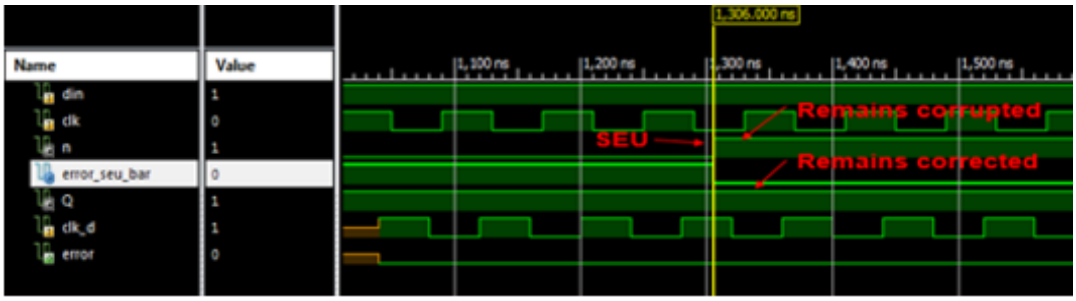


Figure 19. Corrected Q

The delayed clock transition occurs at 110 ns. The errors having transitions before 90 ns and before 110 ns have been detected. But upsets which have transitions after 90 ns and before 110 ns are not getting detected. As well as, transitions occurring before 90 ns and after 110 ns are not getting detected.

For analyzing the correction process, errors have been injected at node ‘n’. In all the above three cases which are given in Figure 18 to Figure 19, value of Q won’t be interrupted. In Figure 17 Q value will be captured when upset is occurring at node ‘n’. Figure 18 shows that the value at node

'n' will be propagated to output Q when error occurs. When the value at node 'n' remains as corrupted, the value at output Q remains as corrected and this is given in Figure 19.

Table 2. Error tolerance in SETTOFF

S.No	Error type	Inference
1	Captured transients	Output degraded, abided TRD
2	Error upsets (FF)	Output degraded, abided TD based architecture
3	Errors (TRD)	Output not degraded and abided
4	Errors in (TD)	Output degraded and not abided

Table 2 gives the error tolerance analysis of SETTOFF. Particular intervals of errors can be detected and correction occurs for SEUs induced at the node 'n', which is the input of correction XOR gate. When compared to TRD architecture, SETTOFF has the capability of correcting the error upsets in the main Flip Flop.

6.1.3. Self checking register

The self checker module has a parity checker for checking errors, a glitch filter for filtering and a transition detector as given in Figure 20.The error signals from each Flip Flop is given to an OR gate.

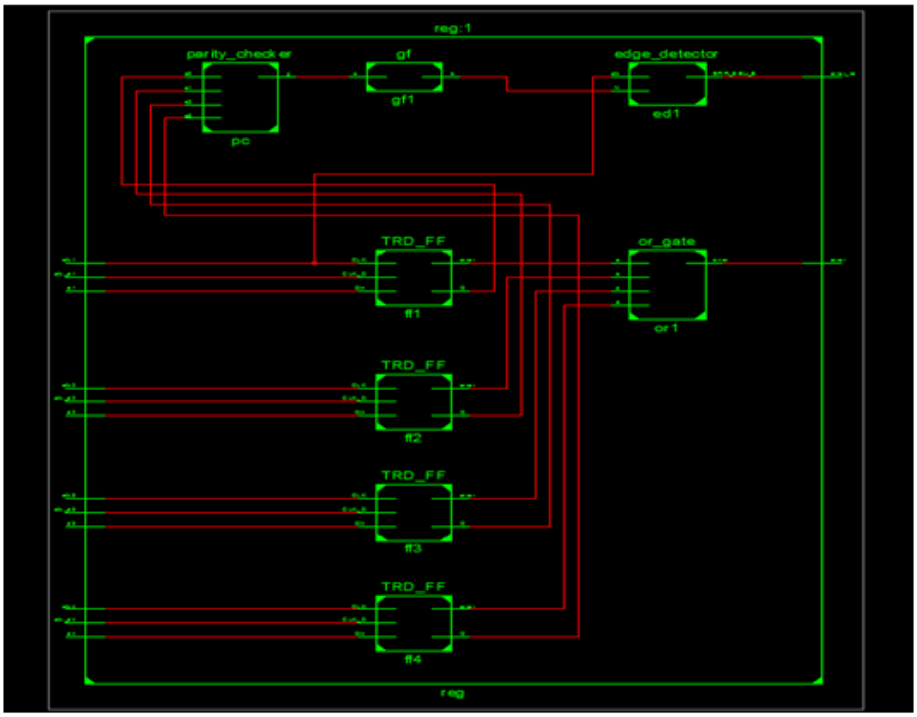


Figure 20. RTL schematic of self-checking register

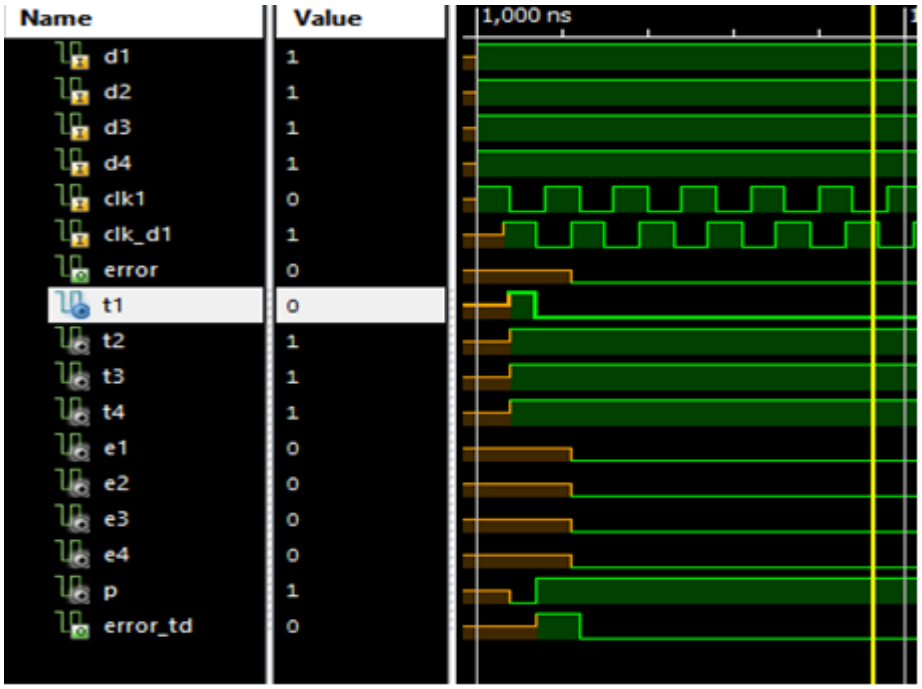


Figure 21. Output waveforms of self-checking register for single error detection

A single event transition is applied at the output of the first flip flop and the transition occurring at parity checker output is detected by the transition detector. As an indication of the error occurred at the first Flip Flop output, the output of the transition detector, error_td signal, gets asserted.

6.1.4. Self-checking register for multi-bit error detection

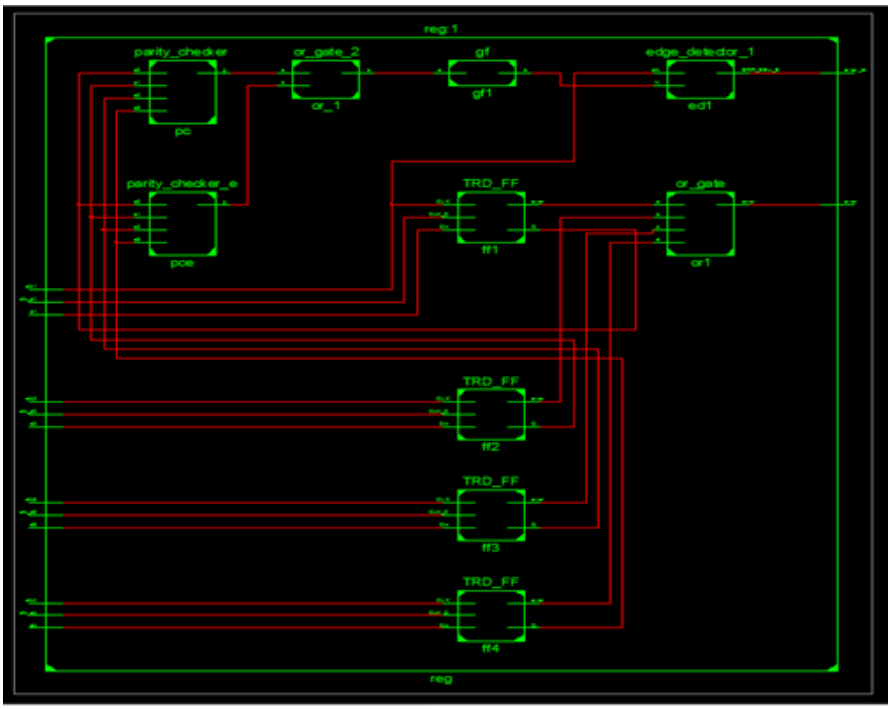


Figure 22. RTL schematic of self checking register for multi-bit error detection

The architecture in Figure 22 show self checking register for multi-bit error detection. An additional parity checker is given along with the self-checker to detect the multi-bit errors. The outputs from the parity checkers are given as the inputs to an OR gate and the output from this gate is then given to the glitch filter.

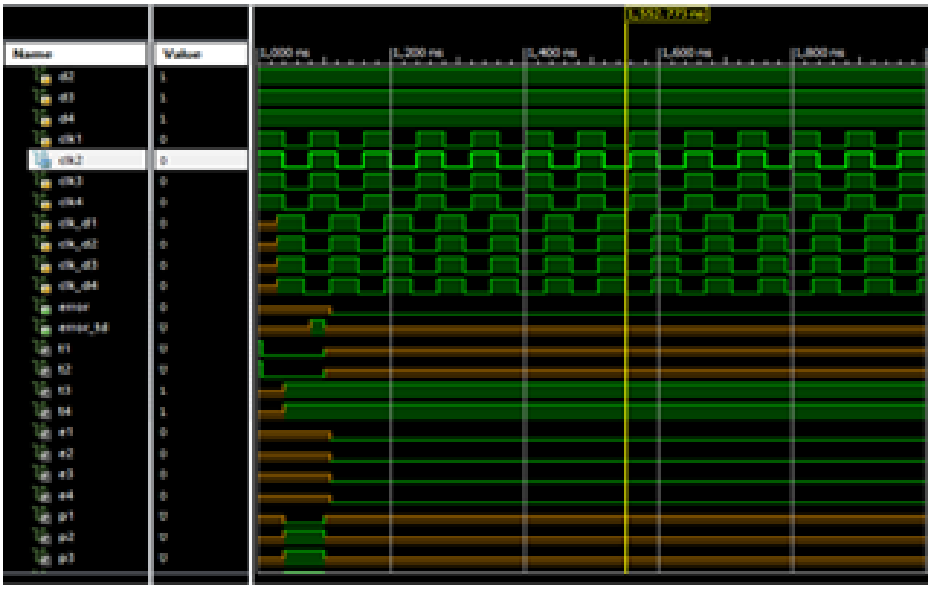


Figure 23. Output waveforms of self-checking register for single error detection

Table 3 Analysis of error tolerance in Self-checking register

S.No	Error type	Inference
1	Captured transients	Output degraded, abided TRD
2	Error upsets (FF)	Output degraded, abided TD
3	Errors (TRD)	Output not degraded and abided
4	Errors (TD)	Output degraded, abided Self-checker
5	Errors (self-checker)	Output not degraded and abided

Table.3. summarizes the analysis of error tolerance in self checking register. Self-checking register has more error tolerance capability. It detects the errors occurring in the TD-based architecture also compared to SETTOFF architecture.

6.2. Circuit Analysis

Figure 24 shows the circuit diagram of SETTOFF which has been implemented in Microwind Dsch tool. Fault analysis results are given in Figure 25 and Figure 26. Figure 25 shows the truth table of SETTOFF which is similar to that of conventional D Flip Flop. Test vector analysis of SETTOFF with stuck at faults at clock, input and internal nodes are given in Figure 26.

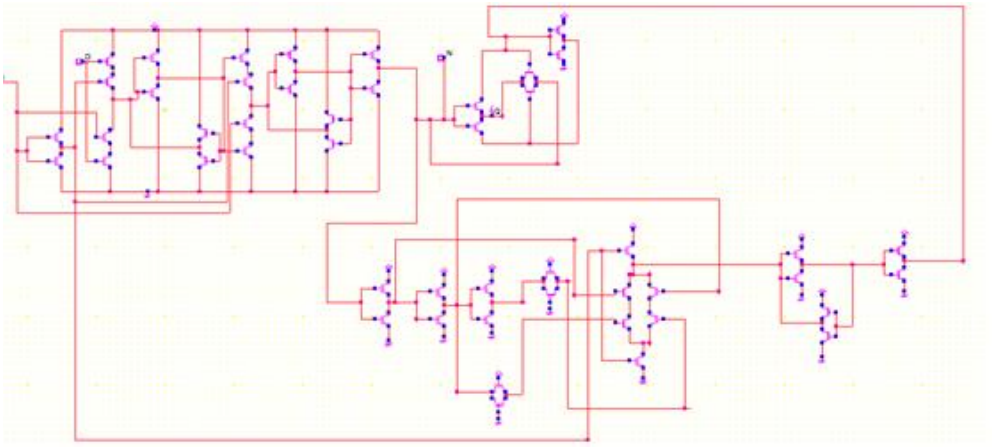


Figure 24. Circuit diagram of SETTOFF

Truth-Table | Test Vectors

clk	D	N	Q
0	0	0	65535
0	0	1	65535
0	1	0	65535
0	1	1	65535
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Figure 25. Truth table of SETTOFF

Truth-Table | Test Vectors

clk,D,N	000	001	010	011	100	101	110	111
Q(fault-free)	65535	65535	65535	65535	0	0	1	1
clk@0	x	x	x	x	x	x	x	x
clk@1	0	0	1	1	0	0	1	1
D@0	x	x	x	x	0	0	<0>	<0>
D@1	x	x	x	x	<1>	<1>	1	1
N@0	x	x	x	x	<1>	<1>	1	1
N@1	x	x	x	x	0	0	<0>	<0>
Detect score					2/6	2/6	2/6	2/6

Figure 26. Test vector analysis of SETTOFF

Error tolerance analysis gives a comparison between the different techniques. The proposed one has more error tolerance capability.

7. CONCLUSION

A register with self checking capability has been proposed. The proposed system has been analyzed by introducing faults of different time intervals. It is found that the proposed system is error tolerant towards single event upset and timing errors. The system detects the error as well as corrects by itself with the help of in built self checking capability. The multiple errors are also detected and corrected. The fault analysis can be extended to other modules of digital sub blocks so that failures can be prevented. The system has a drawback of consuming more area. Techniques to reduce the area can be done in future.

REFERENCES

[1] C. L. Chen, M. Y. Hsiao, (1984) "Error-correcting codes for semiconductor memory applications: A state-of-the-art review", IBM Journal of Research and Development. Vol.28, Issue.2, pp. 124 – 134.

[2] C.H. Chen, D. Blaauw, D. Sylvester, Z. Zhang, (2014) "Design and evaluation of confidence-driven error-resilient systems", IEEE Transactions on Very Large Scale Integration (VLSI) systems,Vol.22 , Issue.8, pp. 1727–1737.

[3] Hsuan-Ming Chou, Ming-Yi Hsiao, Yi-Chiao Chen, Keng-Hao Yang, Jean Tsao, Chiao-Ling Lung, Shih-Chieh Chang, Wen-Ben Jone, and Tien-Fu Chen, (2015) "Soft-error-tolerant design methodology for balancing performance, power, and reliability", IEEE Transactions on Very Large Scale Integration (VLSI) Systems. Vol.23 , Issue.9, pp.1628–1639.

[4] L. Anghel and M. Nicolaidis, (2000) "Cost reduction and evaluation of a temporary faults detecting technique," Proceedings Design, Automation and Test in Europe Conference and Exhibition 2000 (Cat. No. PR00537), Paris, France, pp.591-598.

[5] M. Ebrahimi, A. Evans, M. B. Tahoori, R. Seyyedi, E. Costenaro and D. Alexandrescu, (2014) "Comprehensive analysis of alpha and neutron particle-induced soft errors in an embedded processor at nanoscales", Design, Automation and Test in Europe Conference and Exhibition (DATE), Dresden, pp.1-6.

[6] M. Favalli and C. Metra, (2004) "TMR voting in the presence of crosstalk faults at the voter inputs",IEEE Transactions on Reliability, Vol. 53, No. 3, pp. 342-348.

[7] M. Nicolaidis, (1999) "Time redundancy based soft-error tolerance to rescue nanometer technologies", Proceedings 17th IEEE VLSI Test Symposium (Cat. No.PR00146), Dana Point, CA, USA, pp. 86-94.

[8] M. Zwolinski, (2001) "A technique for transparent fault injection and simulation in VHDL", Microelectronics Reliability, Elsevier Ltd., 41 (6), pp.797- 804.

[9] N.D.P. Avirneni and A. Somani, (2012) "Low Overhead Soft Error Mitigation Techniques for High-Performance and Aggressive Designs", IEEE Transactions on Computers, vol. 61, no. 4, pp.488-501,April 2012

[10] N. Gaitanis, (1988) "The design of totally self-checking TMR fault-tolerant systems", IEEE Transactions on Computers, Vol. 37, No. 11, pp. 1450-1454.

[11] S. Lin, Y. Kim and F. Lombardi, (2011) "Design and Performance Evaluation of Radiation Hardened Latches for Nanoscale CMOS", in IEEE Transactions on Very Large Scale Integration (VLSI) Systems,Vol.19, No. 7, pp. 1315-1319.

[12] S. Mitra, N. Seifert, M. Zhang, Q. Shi and K. S. Kim, (2005) "Robust system design with built-in soft-error resilience", Computer, Vol.38, No.2, pp. 43-52.

[13] T. Calin, M. Nicolaidis and R. Velazco, (1996) "Upset hardened memory design for submicron CMOS technology", IEEE Transactions on Nuclear Science, Vol. 43, No. 6, pp. 2874-2878.

[14] Y. Lin and M. Zwolinski, (2014) "A cost efficient self checking register architecture for radiation hardened designs", IEEE International Symposium on Circuits and Systems (ISCAS), Melbourne VIC, pp. 149-152.

[15] Y. Lin, M. Zwolinski and B. Halak, (2014) "A low-cost radiation hardened Flip-Flop", 2014 Design, Automation and Test in Europe Conference and Exhibition (DATE), Dresden, pp. 1-6.

[16] Y. Lin, M. Zwolinski and B. Halak, (2016) "A Low-Cost, Radiation-Hardened Method for Pipeline Protection in Microprocessors", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 24, No. 5, pp. 1688-1701.

AUTHORS

T. Shunbaga Pradeepa is obtained her B.E. Degree in Electronics and Communication Engineering and M.E. Degree in VLSI Design. She has 4 years of industry (R&D) experience, currently she is working as Assistant Professor in the Department of Electronics and Communication Engineering at Coimbatore Institute of Technology, Coimbatore. She has around 10 years of teaching experience. She is currently doing research in the automotive safety architecture design. Her research interests are in the design and testing of analog and digital systems, Embedded Systems, VLSI design.

Dr.Uma Maheswari obtained her B.E. Degree in Electronics and Communication Engineering from Government College of Technology, Coimbatore, M.E. Degree in Applied Electronics from Coimbatore Institute of Technology and Doctoral degree in Electrical and Electronics Engineering with specialization in Biometrics, from Bharathiar University, Coimbatore. She is presently working as a Professor in the Department of Electronics and Communication Engineering, Coimbatore Institute of Technology, Coimbatore. She holds around 32 years of teaching experience. Her research interests are VLSI Design, Digital Image Processing and Digital Signal Processing. She is also guiding research scholars in different disciplines.

A SMART SOLAR PV MONITORING SYSTEM USING IOT

V.Kavitha[1] and V.Malathi[2]

[1]PhD Scholar, Department of Electrical and Electronics Engineering, Anna University Regional Campus, Madurai, India

[2]Professor, Department of Electrical and Electronics Engineering, Anna University Regional Campus, Madurai, India

ABSTRACT

Renewable energy sources are proven to be reliable and accepted as the best alternative for fulfilling our increasing energy needs. Solar photovoltaic energy is the emerging and enticing clean technologies with zero carbon emission in today's world. To harness the solar power generation, it is indeed necessary to pay serious attention to its maintenance as well as application. The IoT based solar energy monitoring system is proposed to collect and analyzes the solar energy parameters to predict the performance for ensuring stable power generation. The main advantage of the system is to determine optimal performance for better maintenance of solar PV (photovoltaic). The prime target of PV monitoring system is to offer a cost-effective solution, which incessantly displays remote energy yields and its performance either on the computer or through smart phones. The proposed system is tested with a solar module of 125-watts to monitor string voltage, string current, temperature, and irradiance. This PV monitoring system is developed by a smart Wi-Fi enabled CC3200 microcontroller with latest embedded ARM processor that communicates and uploads the data in cloud platform with the Blynk application. Also the Wireless monitoring system maximizes the operational reliability of a PV system with minimum system cost.

KEYWORDS

Solar PV, Internet of Things, Mobile Application, Online Monitoring.

1. INTRODUCTION

Power generation is a major factor in many developing countries. Due to the improvement of the industrial and commercial sector, energy demand reaches its peak. Hence all are poignant towards renewable energy source to produce green energy for meeting out our energy consumption. This can help the society to decrease greenhouse gas emission and ozone layer depletion for future generation. Among this solar photovoltaic technique is gaining popularity due to huge availability, reduced cost, easy installation, and maintenance. Currently, Internet of Things (IoT) is an evolving technology that makes things smarter and user-friendly when connected through the communication protocol and cloud platform. The efficiency of the solar panel is influenced by basic parameters such as current, voltage, Irradiance, and temperature. Hence real-time solar monitoring system is essential for increasing the performance of the PV panel by comparing with the experimental result to initiate preventive action. In recent years there had been a lot of research attempts made in solar energy. A simple forecasting database is modeled using MySQL to collect the raw data, filter un-relevant values and produce forecast without the assistance of any modern automation tools. In addition, machine intelligence techniques are used for forecasting to obtain robust performance [1]. A real-time supervising

N. Ramasubramanian et al.(Eds) : SRAIC-2019
pp. 01-33, 2019. © CS & IT-CSCP 2019 DOI: 10.5121/csit.2019.91502

and data acquisition model for Solar PV module is proposed using LABVIEW to determine the performance of different solar PV ratings. This is a powerful tool for exploring the operation of different PV modules with respect to real-time data [2-3]. Microcontroller based displaying system is proposed to monitor the different factors that affect the performance of PV panel. The measured parameters are evaluated with the standard operating condition to provide necessary action for better performance of PV [4].

A low-cost solar panel monitoring is developed based on IoT for online visualization and improving the performance. This helps to take preventive maintenance and tracking the fault location [5]. An IoT based cloud monitoring system is proposed and developed using the Raspberry pi for remote PV plant [6]. The basic characteristics of a PV system are analyzed using LABVIEW tool for real-time measurement to study the fault diagnosis in PV plant [7]. A smart monitoring system is developed with a microcontroller and Labview to gain the maximum efficiency with the use of sun trackers [8]. A remote Solar monitoring and control system is proposed for implementation at the plant level and promotes the decisional process for central control station which has the crucial role for processing, storage, warning and displaying [9].PV monitoring system is developed based on wired and wireless networks to transmit the parameters to a remote coordinator that offers a web-based application for remote access [10]. A practical graphical user interface is developed using Lab view for online monitoring for solar PV. Arduino controller is used for analyzing the measured parameters and sends the data to the server for making a useful decision which improves the performance of PV panel [11]. A cost-effective smart architecture is proposed to optimize the efficiency of the PV panel by detecting the performance degradation through continuous monitoring system [12]. HEM algorithm based smart controller is implemented for choosing the source priority to maximize the use of Solar PV for home power management [17].Therefore, the proposed work illustrate the real-time Solar PV monitoring system using cost efficient Smart Controller communicate with the cloud platform provides large storage space and fast dataaccess.

The paper is structured as follows: Section II describes the conventional work. Section III presents the proposed work and its functionality. Section IV illustrates the results of Solar monitoring system. Section V summarizes the proposed work and its application.

2. RELATED WORK

A virtually reliable Solar PV monitoring system [2] is developed with LABVIEW software is shown in Fig.1 a practical development tool for computing the performance of a 5-Watt Solar Module. The electrical parameters like voltage, current, temperature, humidity and irradiance are measured using sensors and store the data in the DAQ (Data Acquisition) unit, which provide an interface to the PC. LABVIEW tool plot the I-V and P-V graph based on the data acquired and also compute the Maximum voltage, Maximum current, Fill factor and efficiency of the solarpanel.

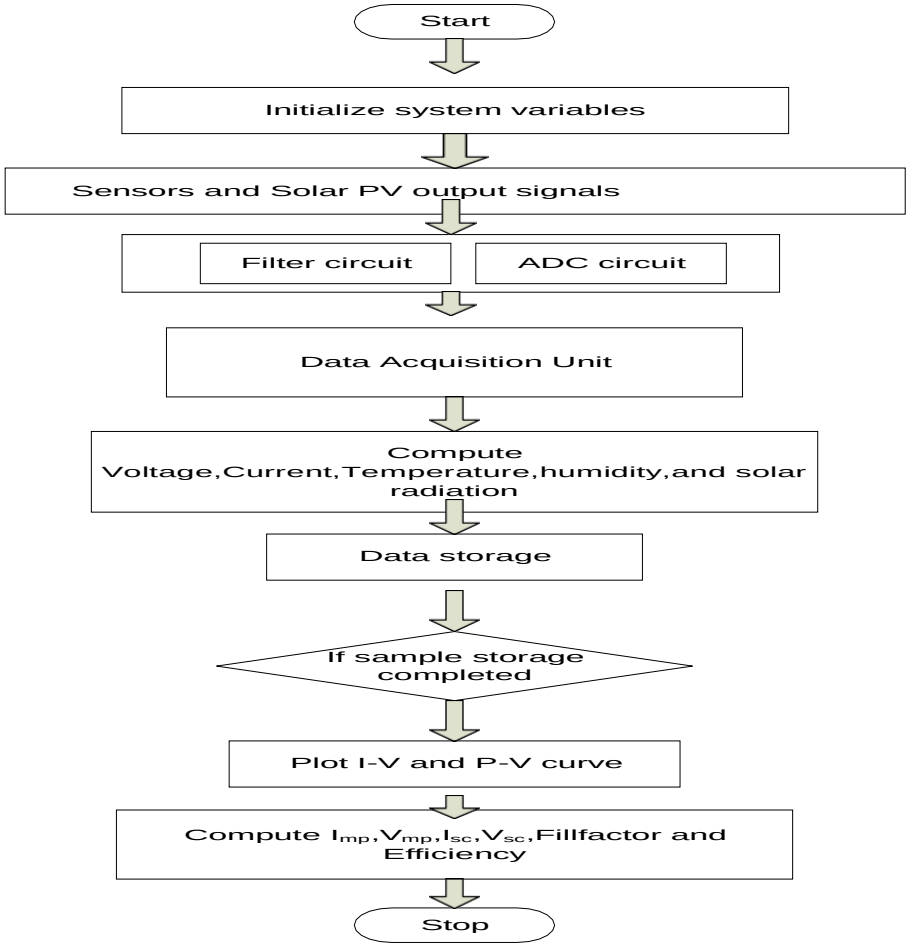


Figure.1 Virtual Solar PV monitoring system using LABVIEW

3. PROPOSED WORK

The real-time solar energy monitoring system is proposed based on the three-layer architecture of Internet of Things (IoT). The three-stage architecture is shown in Fig 2. The lower layer contains sensing and actuating devices like sensors, actuators, RFID, camera, and controllers since it is a combination of sensing and processing layer. The next layer is a middle layer which encompasses network layer with wired and wireless network like LAN, Bluetooth, Zigbee, 4G, Wi-Fi etc., act as a gateway to route the packets (data) to the transport layer that contains TCP/IP, UDP, for further transmission of data to the upper end. The final stage is the application layer deliver user interface and cloud platform for remote access.

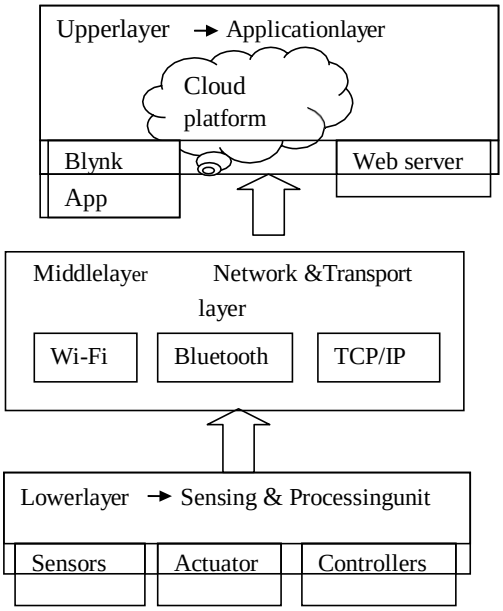


Figure.2 Three-layer architecture of Internet of Things

The block diagram of IoT based solar monitoring system is shown in Fig.3.This illustrates the outline of our proposed work. Poly Crystalline silicon of 125-watt solar panel is used for a monitoring system. The voltage and current sensors are used to measure the respective voltage and current from the panel. The temperature sensor is placed on the solar PV module to measure the current temperature which greatly affects the efficiency of the solar panel. Pyranometer is an instrument to measure the amount of solar irradiance in a planar surface in terms of W/m^2. The Microcontroller plays a pivotal role in handling the measured data for processing and forwards the data to the cloud platform through Wi-Fi module for concurrent observation and decision making.

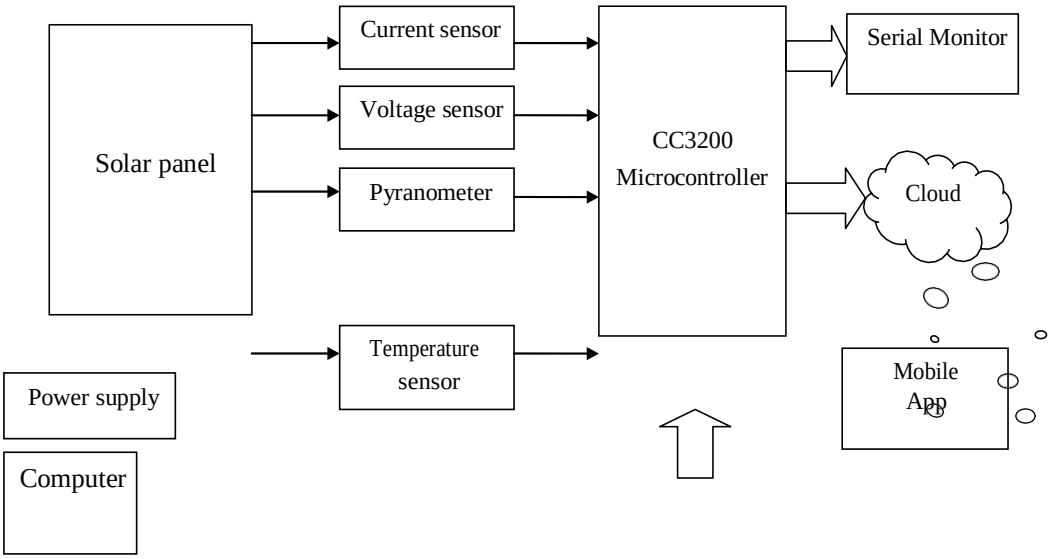


Figure.3 Real-time Solar Energy Monitoring System

3.1. Lower Layer

The sensing units are Voltage sensor, ACS 712 current sensor, pyranometer and temperature sensor. A voltage sensor is a divider circuit that can measure the voltage drop through series resistance. This circuit is useful for measuring voltage above 5 volts. The voltage is calculated based on the resistance factor and reference voltage. The voltage divider circuit is shown in Fig.4 The expression for calculating voltageis

Voltage = (Analog value / Resistance Factor) Reference Voltage*

Resistance factor is calculated with the value of series resistance R_1 and R_2.

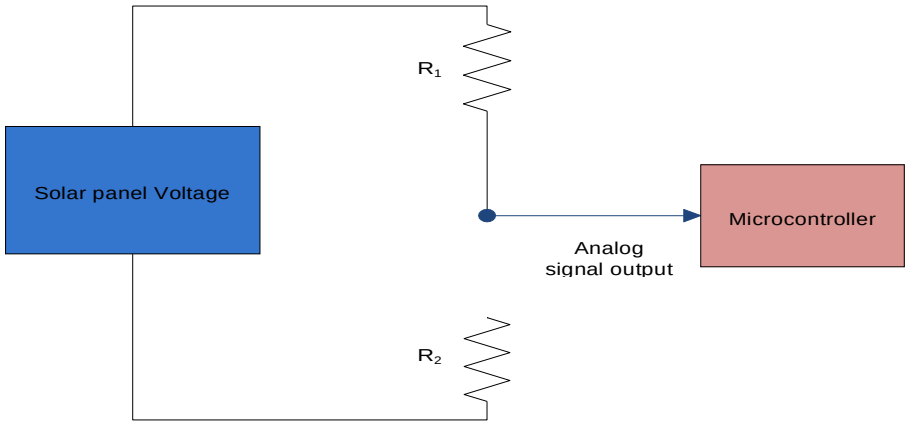


Figure.4 Voltage divider circuit

A current sensor used for measuring solar PV panel is the ACS712 Hall Effect sensor, which can measure up to 20 Amps. This can be effective to measure both DC and AC current. Hall effect sensor connects with the microcontroller through three terminals Analog input, power supply, and ground. The current sensor module is shown inFig.5

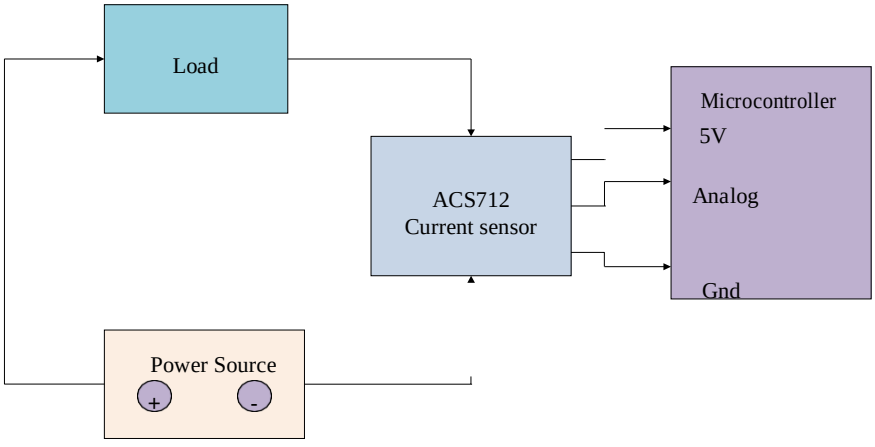


Figure.5 Schematic layout of the current sensor

CM21 pyranometer shows high precision for measuring the solar radiance in a plane surface due to direct and diffused solar radiation. The high quality optical domes help to reduce the directional error less than 10 W/m2. It has high sensitivity for data acquisition system and provides low impedance for interference and noise. It has the maximum spectral range of 300-

1200 nm with sensitivity between 7 and 17 μV/Wm^{-2}. The operating temperature of this instrument is -40°C to +80°C.The construction of pyranometer [13] is shown in Fig.6. In general, the global radiation is determined using the output voltage of pyranometer and its sensitivity. For the calculation of solarirradiance

$E = U_{emf} / Sensitivity$
E = solar irradiance inW/m^2
U_{emf} = output voltage of pyranometer in μV Sensitivity =Sensitivity of pyranometer inμV/W/m^2

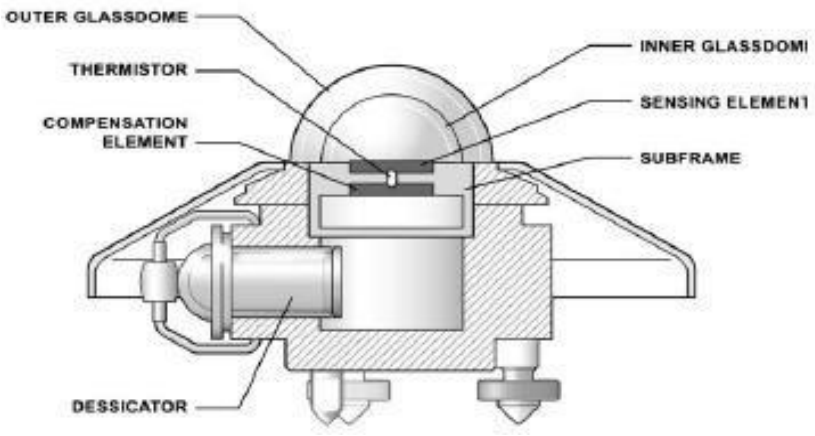


Figure 6. The general structure of CM21 Pyranometer

The sensor for measuring the temperature of the solar panel is LM35 an analog sensor. It is a low cost, a tiny sensor to measure the environmental temperature from -50°C to +150°C. The operating voltage of this IC is 5v. There is an increase of 0.01v for all rise in temperature. The formula for converting the voltage to temperature is

$$Temperature = Voltage / 10mV/°C$$

CC3200 MICROCONTROLLER:

A CC3200 simple link is a system-on-chip (SoC) controller with inbuilt Wi-Fi connectivity designed for IoT Application. The wireless MCU (Microcontroller Unit) includes a high-speed ARM cortex M4 processor to develop a real-time application with the Single IC (Integrated chip). The controllers has embedded memory of 256KB RAM, serial Flash boot loader and ROMdrivers.TheMCUhas12-bitAnalog-to-Digital Converter(ADC)with four channels and 27 programmable general purpose input output (GPIO) pins. The Wi-Fi module contains 802.11b/g/n radio provides a fast and secure internet connection with advanced encryption standards. The power management subsystem includes a DC-DC converter to maintain a broad range of supply voltages. The Fig.7 shows [14] the hardware overview of the controller.

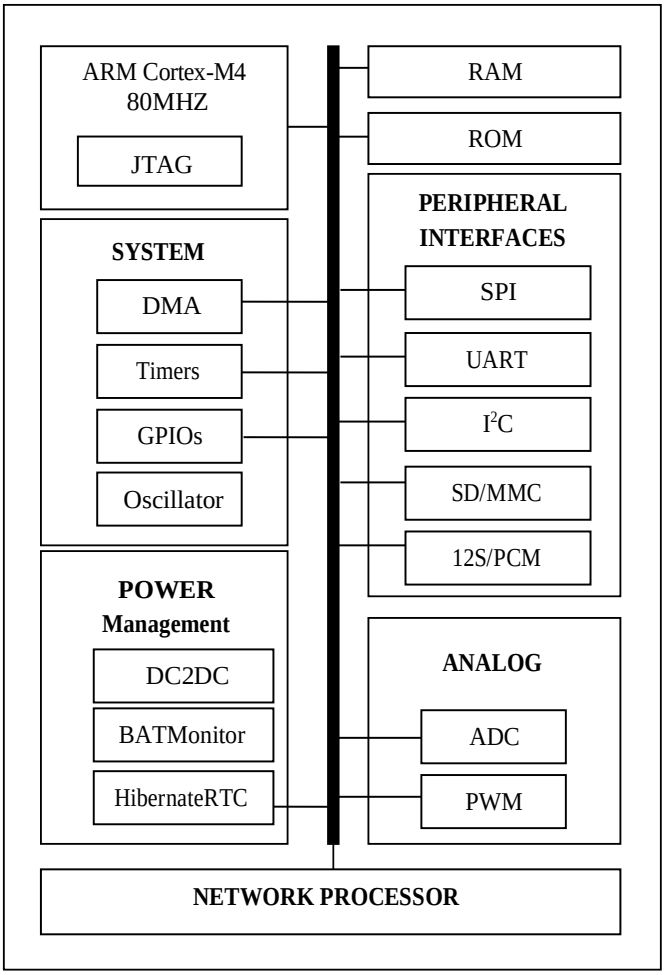


Figure 7. Hardware overview of CC3200

3.2. Middle Layer

In the middle layer, the smart controller processes the sensed data and transmits the information through Wi-Fi protocol which acts as a gateway to communicate with the upper end. The communication protocol like TCP/IP, UDP provides standard rules to ensure secure data transmission to the application layer.

3.3. Upper Layer

The Final layer is the application layer which can store the real-time data in a cloud platform for easier access, data visualization, and right decision making. This proposed work facilitates a cloud-based mobile application; Blynk [15] is used for tracking the operation of solar PV in real-time.

Blynk is a free source cloud platform offers user-friendly IoT application. We can develop a secure scalable and fast application with pre-designed elements to view the data virtually. It supports many hardware platforms and connectivity types for deploying any number of devices online. It gives a continuous solution for the remote application which saves time and resources with the very low cost.

4. RESULTS AND DISCUSSION

A polycrystalline 125-Watt photovoltaic module is taken for the experimental implementation and testing the performance with standard ratings of the solar panel as mentioned in Table 1. The proposed work is carried out in a solar energy testing center at Madurai Kamaraj University. The hardware setup is shown in Fig.8 and Fig.9. A high precision pyranometer is used to measure the solar radiance on a plane surface. LM 35 a sensing device to measure the current temperature in the solar panel. These two parameters highly influence the performance of the solar panel[16].

Since irradiance is corresponding to current and temperature affects the voltage of the solar module. Hence the power generation of the solar panel relies on temperature and irradiance. The proposed system programming codes are developed in C language via Energia IDE. This is a non-proprietary integrated development environment designed for Texas Instruments like CC3200 Microcontroller. The blynk libraries are included in the programming function to communicate and transfer the sensed values to the Cloud platform. The electrical characteristics are monitored and displayed successfully through a mobile application. The result in Fig.10 shows the real-time Solar PV monitoring system through Blynk. The inference of output is the increase in temperature reduces the voltage generation in PV and also the rise in irradiance shows a moderate increase in current. Hence these two parameters become the deciding factor for the performance of solar module. The results shown in Fig.11 are displayed in the Web server. The Fig.13 shows the output in serial monitor of PC. The obtained result is nearer to the Standard ratings of a solar panel.

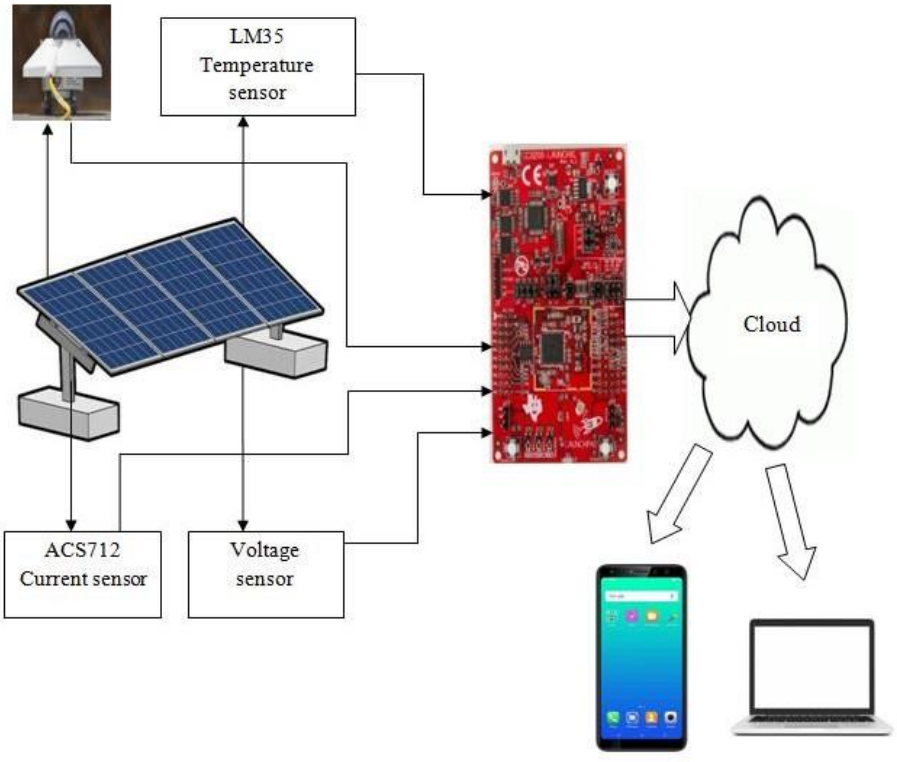


Figure.8 Hardware implementation of proposed work

Figure.9 Experimental setup of Solar PV Monitoring System

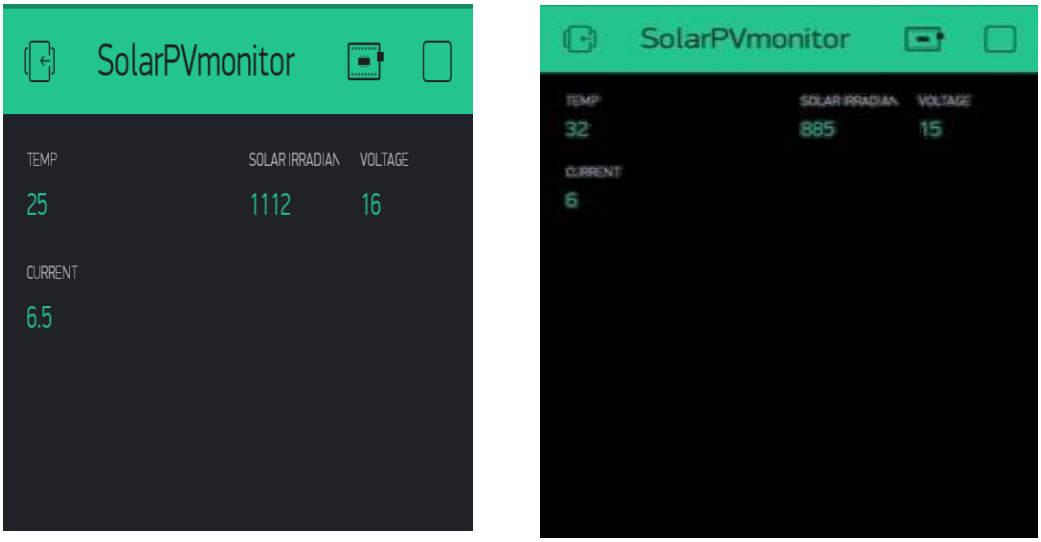


Figure.10 Real-time Solar PV monitoring system using Blynk

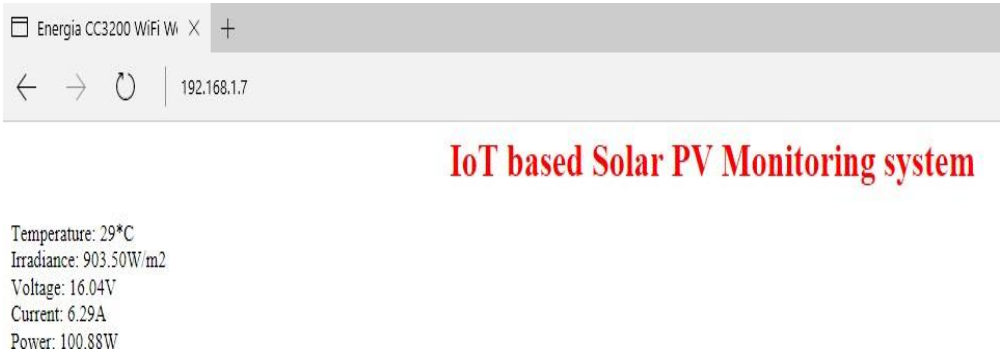


Fig.11(a)

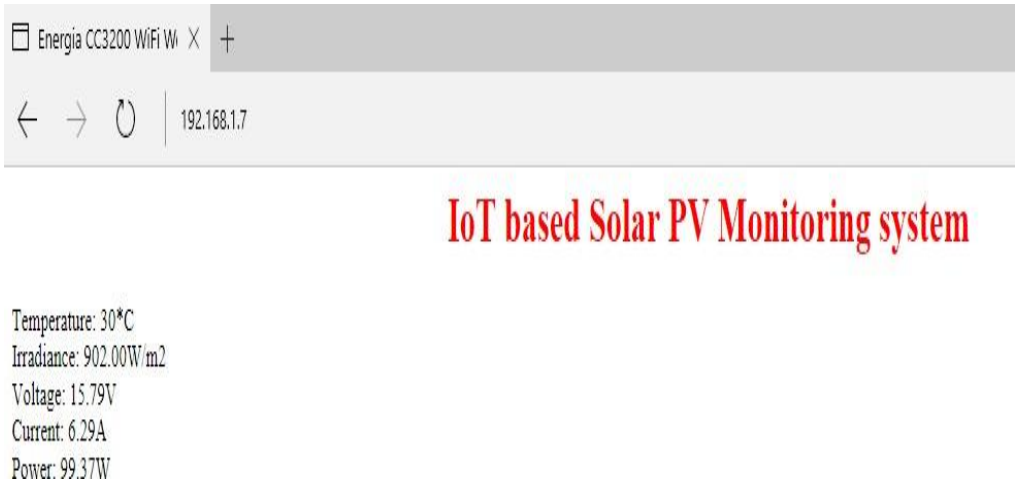
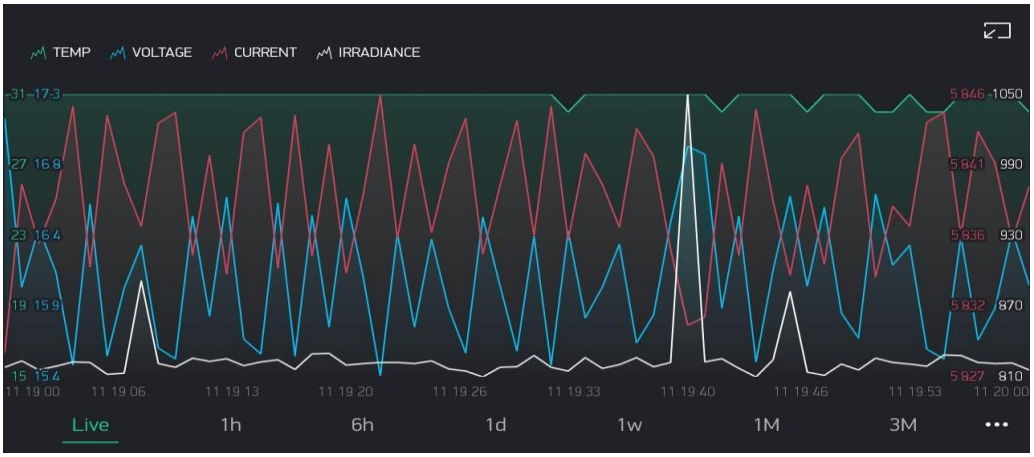


Fig.11(b)

Fig.11 (a-b) Solar PV Monitoring output through Web server

Fig.12 represents graph of solar power monitoring system through blynk application. The experiment is carried out for a week with different time intervals from 10.00AM to 05.00PM in a Solar Energy testing centre at Madurai, India. The electrical parameters of PV module are analyzed by continuous monitoring for estimating the behavior of solar panel. The graph shows the variation in temperature due to climatic condition which influences the voltage generation and irradiance affects the current parameter of PV module. The standard operating temperature of the solar panel is 25°C. Generally, the temperature above the standard test condition may reduce the performance of solar panel [16]. The decrease in temperature shows the rise in voltage as shown in Fig 12(a), (b), (c), (d), (e), (f) and the current directly correlate with irradiance. Hence, the change in solar radiation impacts the current characteristics in PV panel. The temperature reduces from 31°C to 30°C during morning hours from 10.30 AM to 11.30AM; the voltage goes to peak and then oscillates until reaching the stable state, at the instance irradiance is also maximum at this temperature which is shown in Fig.12 (a) and (b). The result of 12(c) represents the fall in temperature after 11.30AM and simultaneously the irradiance shows sharp reduction in spectral range. The Fig.12 (d) display the rise in temperature after 01.00 PM, at this stage irradiance level increase as current increases and the voltage generation reduces when there is a rise in temperature. The graph plotted in 12 (e) and (f) is observed after peak hours (i.e.) 02.00 PM to 05.00 PM. During the interval the temperature changes frequently from high to low and low to high and also solar radiation varies according to environmental condition. Hence the result shows the maximum power generation of solar panel which is nearly close to standard rating ofPV.

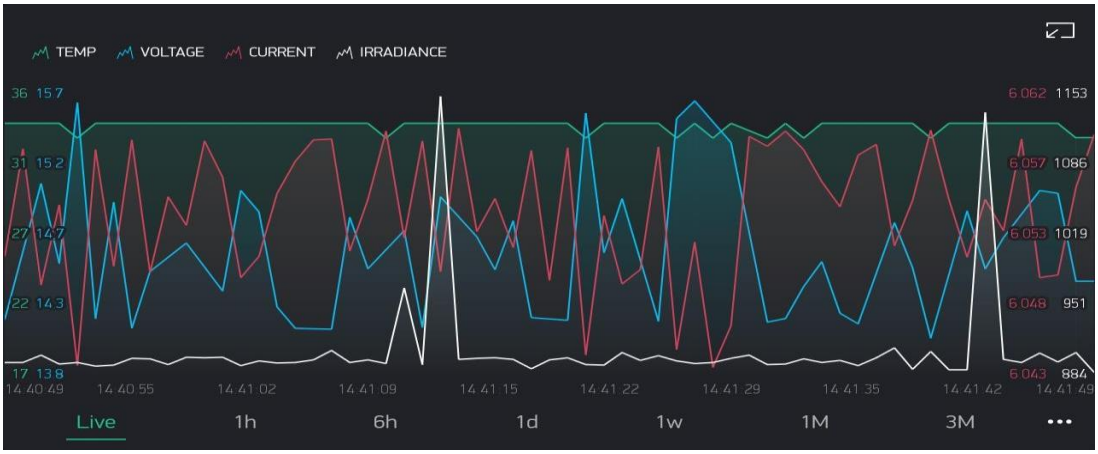
(a) Solar power monitoring at 10.50AM



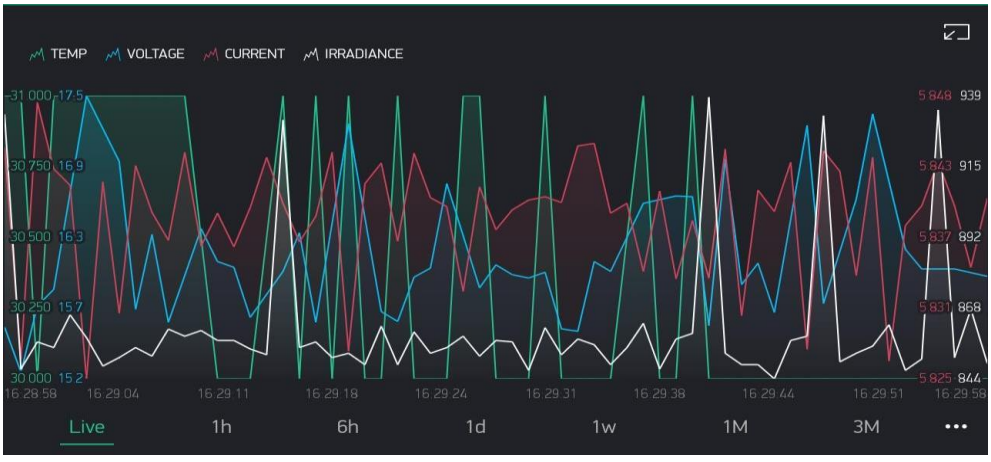
(b) Solar power monitoring at 11.20AM

(c) Solar power monitoring after11.30AM

(d) Solar power monitoring after 1.00PM



(e) Solar power monitoring after 2.00PM



(f) Solar power monitoring after4.00PM

Fig.12(a-f) Graphical view of solar energy monitoring system through blynk application

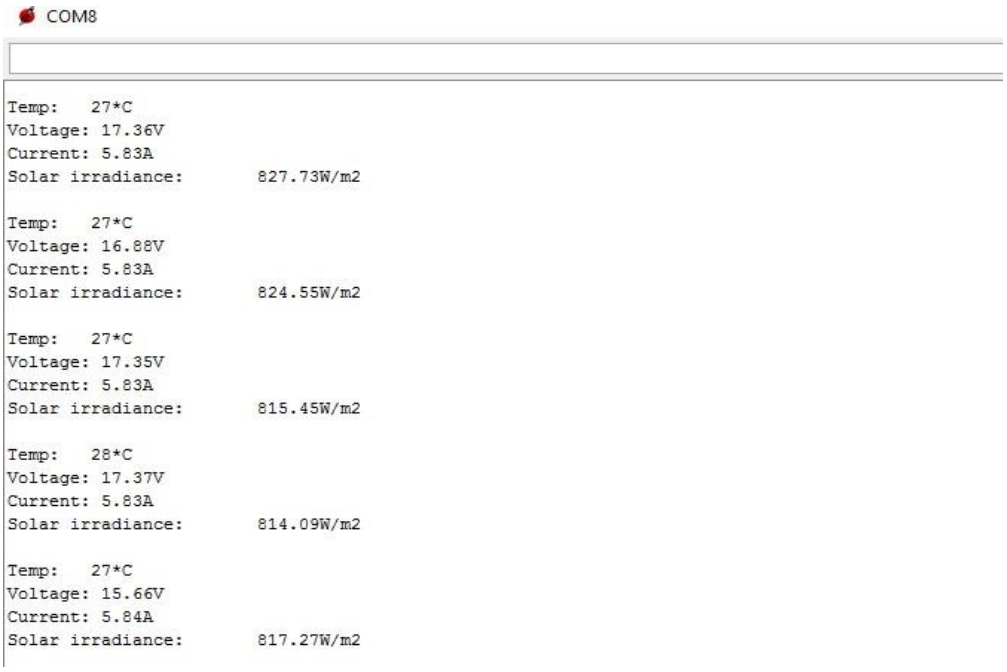


Fig.13 Solar PV Monitoring Output through Serial Monitor

Table.1 125-Watt Solar PV ratings

S.No	Electrical ratings	Value
1.	Rated Maximum power (P_{max})	125Wp ± 3%
2.	Open-Circuit Voltage(V_{oc})	21.6 V
3.	Short Circuit Current (I_{sc})	7.66 A
4.	Voltage at Maximum power (V_{mp})	17.65 V
5.	Current at Maximum Power(I_{mp})	7.08 A
6.	System voltage	1000V_{max}

5. CONCLUSIONS

An IoT based virtual solar energy monitoring system is developed using a low-cost smart microcontroller. The cloud-based Blynk application shows the measured solar parameter in real-time through mobile. The monitored parameters show the optimized result that matches approximately with Electrical ratings of solar module tested under Standard Test Condition (STC). The proposed work helps to predict the performance of the Solar PV module through remote access. This can be extended for a large-scale solar plant to take preventive action by regularly monitoring the performance of the solar plant. It will be highly useful for the industrial and commercial application.

ACKNOWLEGDEMENTS

The authors want to thank the Head of the department of Solar Energy for carrying out this work in solar testing centre at Madurai Kamaraj University and colleagues for their remarkable comments to improve the work and assistance in proof reading.

REFERENCES

[1] Hugo T.C. Pedro, Edwin Lim, Carlos F.M. Coimbra(2018), “A database infrastructure to implement real-time solar and wind power generation intra-hour forecasts”, *International Journal of Renewable energy Elsevier*, Vol.123,pp.513-525.

[2] Amit Kumar Rohit, Amit Tomar, Anurag Kumar, Saroj Rangnekar(2017), “Virtual lab-based real-time data acquisition, measurement and monitoring platform for solar photovoltaic module", *International Journal of Resource-Efficient Technologies*,pp.1-6.

[3] N.A. Othman, N.S. Damanhuri, I.R. Ibrahim, R. Radzali, M.N. Mohd (2010), “Automated Monitoring System for Small Scale Dual-Tariff Solar PV plant in UiTM Pulau Pinang", Proceedings of the World Congress on Engineering(WCE) U.K, Vol.2, pp.1-3.

[4] Kangkana Hazarikaa, Pradyumna Kumar Choudhurya(2017), “Automatic monitoring of solar photovoltaic (SPV) module", Science direct proceedings Vol. 4,pp.12606–12609.

[5] Soham Adhya, Dipak Saha, Abhijit Das, Joydip Jana, Hiranmay Saha (2016), "An IoT Based Smart Solar Photovoltaic Remote Monitoring and Control unit", IEEE International Conference on Control, Instrumentation, Energy & Communication (CIEC), pp.432-436.

[6] Renata I. S. Pereira, Ivonne M. Dupont, Paulo C. M. Carvalho, Sandro C. S. Juca (2017), " IoT Embedded Linux System based on Raspberry Pi applied to Real-Time Cloud Monitoring of a decentralized Photovoltaic plant", *International Journal of measurement Elsevier*,Vol.2,pp.1-18.

[7] Aissa Chouder, Santiago Silvestre, Bilal Taghezouit, Engin Karatepe(2013), “Monitoring, modeling and simulation of PV systems using LabVIEW”, *International Journal of Solar energy Elsevier*, Vol.1,pp.337-349.

[8] Bipin Krishna, Kaustav Sinha (2013), “Tracking of Sun for Solar Panels and Real-Time Monitoring Using LabVIEW”, *Journal of Automation and Control Engineering* Vol. 1, pp.1-4.

[9] R. Nagalakshmi, B. Kishore Babu, D. Prashanth (2014), “Design and Development of a Remote Monitoring and Maintenance of Solar Plant Supervisory System", *International Journal Of Engineering And Computer Science*, Vol.3, pp.9382-9385.

[10] P. Papageorgas, D. Piromalis, K. Antonakoglou, G. Vokas, D. Tseles and K. G. Arvanitis(2013), "Smart Solar Panels: In-situ monitoring of photovoltaic panels based on wired and wireless sensor networks", International Conference on Advancements in Renewable Energy and Clean Environment,Vol.36,pp.535-545.

[11] Haider-e-Karar, Aziz Altaf Khuwaja, Abdul Sattar (2015), "Solar Power Remote Monitoring and Controlling Using Arduino, Labview and Web browser", IEEE International Conference on Power Generation System and Renewable Energy Technologies,pp.1-4.

[12] Bruno Ando, Salvatore Baglio, Antonio Pistorio(2015), “Sentinella: Smart monitoring of photovoltaic system at panel level”, *IEEE Transaction on Instrumentation and measurement*, Vol.64,pp.2188-2199.

[13] www.kippzonen.com/Download/52/CM-21-Pyranometer

[14] https://store.ti.com/cc3200-launchxl.aspx

[15] https://www.blynk.cc/

[16] Haider Ibrahim, Nader Anani,(2017)" Variations of PV module parameters with irradiance and temperature", International Conference on Sustainability in Energy and Building, Energy Procedia, Vol.134,pp.276–285.

[17] Rajalingam S., Malathi V (2016), "HEM algorithm based smart controller for home power management system", *International Journal of Energy and Buildings ELSEVIER*, Vol.131,pp.184-192.

AUTHORS

V.KAVITHA received B.E degree in Electronics and Communication Engineering from Anna University in the year of 2007. She has completed M.E in Embedded System Technologies under Anna University in 2013. She is currently doing Ph.D in full-time at Anna University Regional Campus Madurai. Her research interests include Internet of Things, Smart Grid, and Renewable energy.

V.MALATHI is working as Professor in the department of Electrical and Electronics Engineering in Anna University Regional Campus, Madurai. She completed her Bachelor D egree in College of Engineering Guindy and her Master's degree in Thiyagaraja College of Engineering, Madurai. She completed her Ph.D in Anna University Chennai and her areas of interest are Intelligent Techniques and its Applications, Smart Grid, FPGA based Power System and Automation.

A LOW COST METHANE ABSORPTION FUELING SYSTEM IN WIRELESS SENSOR NETWORKS USING SBC-MS

A.Rehash Rushmi Pavitra[1] and Dr. E. Srie Vidhya Janani[2]

[1,2]Department of Computer Science and Engineering,
Anna University Regional Campus, Madurai

ABSTRACT

The isolated accessible Methane (CH_4) Absorption Fueling System (MAFS) is matured based on the mechanics of Wireless Sensor Network (WSN) comprised of gas sensing capable motes complementing a MAFS-WSN. Discrete routing protocols have been designed earlier for data collection in both compatible and divergent networks. This research presents a novel Scheduling based Clustering (SBC) with Mobile Sink (MS) strategy (SBC-MS) which supplements data collection in MAFS-WSN. The SBC-MS strategy attempts to exploit the vital parameters of energy and distance in selecting the appropriate cluster head that well suits MAFS-WSN in reliable gas detection. The MSs are exploited to reduce the energy expenditure in data communication. Extensive experimentations have been carried out with the proposed SBC-MS to ensure the QOS of MAFS-WSN in terms of schedulability and reliability. The simulation results prove that SBC-MS outperforms the earlier clustering technique M-LEACH in terms of network lifetime, energy consumption, end-to-end delay and data rate.

KEYWORDS

Methane Absorption Fueling system, Gas Sensing Capable Motes, Mobile Sinks, Scheduling and Clustering.

1. INTRODUCTION

The Wireless Sensor Networks (WSNs) endeavor solitary benefits and adaptability in premises of low-power and low-cost deployment in variety of applications which in turn has facilitated the originator to design self-governing sensors [12]. In recent years a variety of air pollution monitoring applications finds their way feasible through WSNs. The ambient air monitoring sensors greatly complement towards a systematic monitoring of air quality. The concentration of Carbon Dioxide (CO_2) in MAFS is quantified by spectroscopic sensors as Non-Dispersive Infra-Red (NDIR) sensors. The level of CH_4 is deliberated in terms of Parts Per Million (PPM) such sensors are often used as gas detectors.

NDIR CO_2 Gas Sensor and Methane Sensor (TGS2611-E)

A light weight spectroscopic sensor termed to be a Non-Dispersive Infra-Red (NDIR) sensor quantifies the gas absorption of radiation at an acknowledged wavelength. The cramped size semiconductor type sensors possess high selectivity of methane gas ensure low cost and low power consumption. The MAFS-WSN works on the principle of transformation of carbon dioxide (CO_2) into methane (CH_4) over a catalyst, which in

N. Ramasubramanian et al.(Eds) : SRAIC-2019
pp. 35-45, 2019. © CS & IT-CSCP 2019 DOI: 10.5121/csit.2019.91503

turn can be precisely recycled as a fuel. Methane (odorless) is an essential intention gas owing to its immense combination in natural gas [13]. The NDIR CO_2 Gas Sensors are also capable of identifying and associating themselves to form a network confined for air quality monitoring.

2. RELATED WORK

WSNs contribute an outstanding, simple to set up, and economical solution thereby favoring a time automated monitoring of the atmosphere. Consequently, a variety of atmosphere monitoring systems have been proposed. A real time pollution monitoring System [1] employs nodes with fixed gas sensors confined for air quality monitoring. Also, the multi-hop data aggregation algorithm exploits the sensor data to generate overall network statistics together ensuring a feasible view of the network.

With relevance to the Mobile Ad Hoc Network (MANET) routing algorithm [8], a set of mobile nodes deployed in the network seem to figure out the status of gas in contrasting field together alerting the smart phone users. The algorithm not only measures the level of air pollution over cities but also ensures the traceability of sender and receiver across the cloud.

The air quality monitoring is identified to be better in terms of data classification [9] with decision tree algorithm. The algorithm isolates a set of data into predefined classes thereby defining a tree structure for accurate monitoring of air quality level.

The monitoring of greenhouse gases has been made possible through a solar powered unmanned aerial vehicle [2].

The gas detectors seem to find their utility in Wireless Gas Sensor Network (WGSN) to detect and monitor harmful gases in utility areas and industries [3]. The WGSN not only encounters the leakage of harmful gases but also approximates the concentration they amount to in the atmosphere thereby setting up a corresponding audio-visual alarm.

By combining wireless sensor network (WSN) and Global System for Mobile (GSM) technology a low-power consumption monitoring system complements to detect gas leakage ensuring home security [4].

The minimum concentration of Methane in air that amounts to ignition has been analyzed with reference to a key parameter Lower Explosive Limit (LEL) [5].

WSN stationed with Meshlium gateway [6] complements towards CO and CO_2 pollution monitoring. The data communication from gas sensors to server over the Meshlium gateway seems to be efficient.

Continuous Air Quality Monitoring Stations (CAQMS) [7] supplement a custom Information System to store, visualize and analyze the air quality related data which are further presentable in a database.

A Hybrid Spatio-Temporal [HST] scheme is suggested [10] to efficiently forecast air pollution interacting with ubiquitous mobile sensor network. The analyses of existing techniques are laid out in Table 1.

Table 1. Analysis of existing techniques

Scheme	Technique	Parameters	Results	Deficiency
Data Aggregation Algorithm [1]	Multi-hop	Temperature, Concentration of CO_2	Increased stability period and strong output signal	Motes expose a high power consumption
MANET Routing Algorithm [8]	Static	Data type, Speed of transmission, Coverage of system	Monitoring of humidity, temperature and gas level	High energy expenditure
Classification Algorithm [9]	Chain based	Accuracy, sensitivity and specificity	High Accuracy	High latency and processing overhead
MOX and NDIR [2]	Statistical information	Reliable performance, Payload constraints	Effective 3D monitoring	High energy consumption
Zigbee Standard [3]	Fixed node	Optimum Received signal strength indication	Better leakage detection	Decrease in network throughput
Embedded Logic [4]	Multi modal	Single bit output	High reliability	Minimum network lifetime.
Wi-Fi Security [5]	Statistical Information	Data quality level, Data quality assessment	Optimal data security and throughput	Poor event detection
End Device(Meshlium Gateway) [6]	Database	Perform data readout, Visualize the data	Data forwarding using Zigbee	Dependency over local database
CAQMS [7]	Star topology	Correlation value	Better system reliability and energy autonomy	High Latency
HST [10]	Grid data	Accuracy prediction, Capacity	Data collection via Bluetooth	Highly prone to errors

3. SYSTEM MODEL

Primary Assumptions:

The formal system model is based on some fundamental assumptions on the different network nodes and mechanisms involved.

- Non-Dispersive Infrared Sensors with an appropriate introverted ID to measure CO_2.
- SBC-MS strategy to ensure reliable gas detection.
- MS computerized with a non-zero value is assumed to migrate within the network.

4. NETWORK MODEL

Initially, three tankers of same size (100 tons) T1, T2 and T3 are deployed in the network field of 600*600 square meter area. The CO_2 absorption tanker T1 absorbs the relevant gas from the atmosphere. The tanker T2 coated with Zr nanoparticles is responsible for Methane conversion. Subsequently, the tanker T3 is employed to act as the Gas Storage System (GSS) to store CH_4. TheNDIR sensor nodes are deployed randomly in the first thereby ensuring a hierarchical clustering phenomenon. A Mobile Sink (MS) is used for the data collection task. Figure 1. demonstrates the network model, where migrates towards the first tanker to collect information on the level of CO_2 from the NDIR sensors.

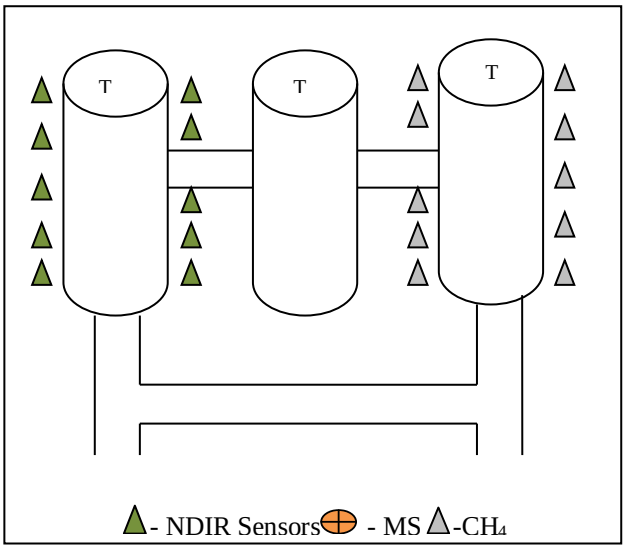


Figure 1. Network Model of MAFS

5. PROPOSED WORK

The Scheduling based Clustering with Mobile Sink strategy balances the energy consumption across the network ultimately increasing the lifetime of MAFS-WSN. The data collection strategy with MS reduces direct transmissions from sensors to BS thereby increasing the lifetime of the individual sensors [14]. The relevant information on the level of CO_2, CH_4 is sent by the MS to BS over the gateway progressively. BS is deemed to be the system organizer that approximates the level of CH_4 in Parts Per Million (PPM) as available in the gas storage system. Figure 2. Shows the key theme for the MAFS-WSN.

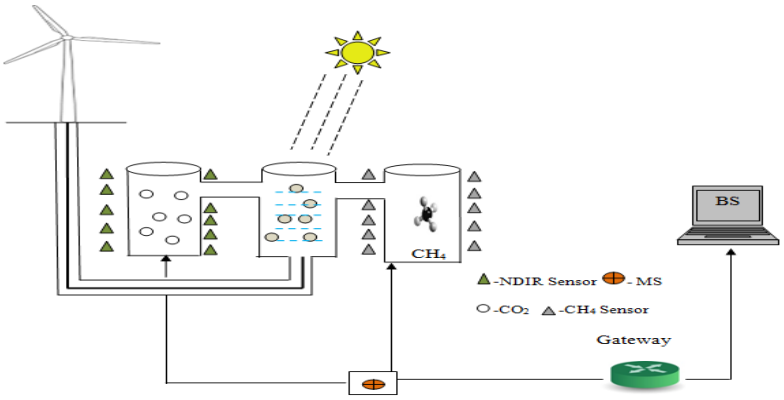


Figure 2. Key theme for the MAFS-WSN

5.1. Development of the Proposed Mafs

MAFS system is used for the real time monitoring of greenhouse gases such as CO_2, CH_4.The wind turbine converts atmospheric hydrogen into electric power. The first tanker involves a Metal Organic Framework (MOF) coated with (Ru/Zr) that further complements gas saturation and catalysis to capture CO_2.

The second tanker is filled with water. The zirconium atoms yielded through the first tanker dissolves in the water to form Zirconium Dioxide (ZrO_2) [11]. When the electric energy and ZrO_2 fuse they form hydroxide radicals and hydrogen ions to generate hydrogen gas.

$$CO_2 \xrightarrow[3H_2]{} CH_4 \quad (1)$$

Subsequently, the combination of CO_2 with hydrogen produces CH_4 (natural gas). The combination process exploits solar energy to ensure high production of CH_4 with a meager amount of catalyst. To illustrate the proposed scheme in detail by dividing them into three phases; (1) CO_2 gas monitoring (2) Basis of SBC-MS CH Selection (3) Gas Storage System (4) Data transmission.

5.2. Co_2 Gas Monitoring

We deploy definite NDIR sensors (non-dispersive infrared) with measuring proposition based on gas absorption of emission at a known wavelength. The internal structure of NDIR CO_2 sensor involves an Infrared lamp, a measuring chamber and absorption detector are stated in Figure 3. The difference between the amount of Infrared light among the source and the detector is measured. This difference is directly proportional to the number of carbon dioxide molecules present in the gas [15]. The specifications of an NDIR sensor are shown in Table 2.

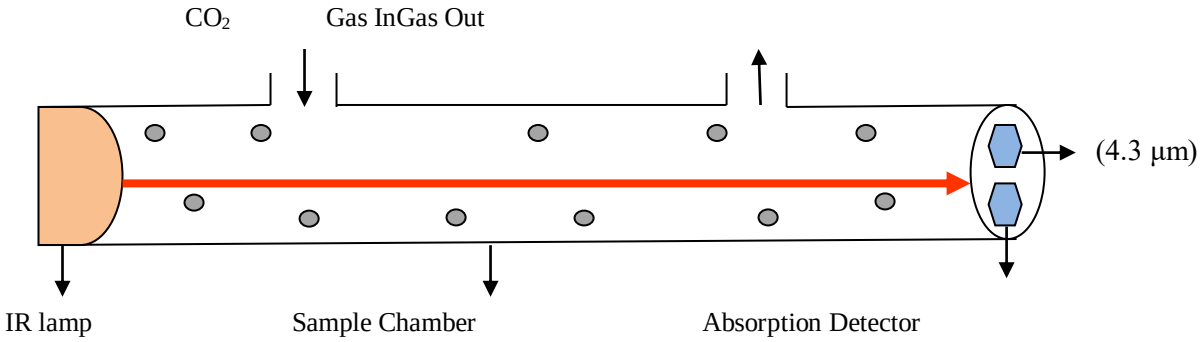


Figure 3. Internal Structure of NDIR CO_2 sensor

The CO_2 gas molecules inside the chamber can be quantified with the Lambert-Beer's Law.

$$I = I_0 \times e^{-kx1x\,[co2]} \quad (2)$$

I = light power intensity after absorption by CO_2, measured at the detector ($W \cdot m^{-2}$)
I_0 = light power intensity at the source ($W \cdot m^{-2}$)
k = absorption index of CO2 at 4.3 µm (dimensionless)
l = length of the absorption path (cm)

Table 2. NDIR Sensor Specifications

Parameters	Value
Operating Temperature	$0^0c - 50^0c$
Storage Temperature	$-30^0c - 70^0c$
Measurement Range	0 – 10000 PPM (Parts per million)

5.3. Basis of Sbc-Ms in CH Selection

CH Selection procedure

Consider two nodes N1 and N2 with different energy levels. CH selection process is employed to choose an optimal CH in terms of residual energy and distance from the surface level of the BS. Assuming N1 is selected as a CH [19], it broadcasts hello message packet to its neighboring sensors within its transmission range. On the other hand, Cluster Member (CM) nodes in a cluster send their data to the corresponding CH. Periodically MS move towards the CHs collect data and transmit data to the BS, over a gateway.

5.4. Gas Storage System

The Gas Storage System is deployed with small size semiconductor type Methane (CH_4) sensors Figure 4. shows the circuit diagram of Methane (CH_4) sensors. Initially two input voltage heater voltage (V_H) and circuit voltage (V_C) is enforced across the sensor element which has a resistance (R_s) between the sensors, electrodes and the load resistor (R_L) connected in series. The (V_C) may be applied periodically. The sensor signal (V_{RL}) is calculated eventual as a change in voltage over the R_L. The (Rs) is obtained with relevance to equation (4); The SBC-MS strategy discussed earlier is adopted. The specifications of Methane sensor are shown in Table 3.

$$R_{S=} \quad \frac{V_C - V_{RL} \; x \, R_L}{V_{RL}} \qquad (9)$$

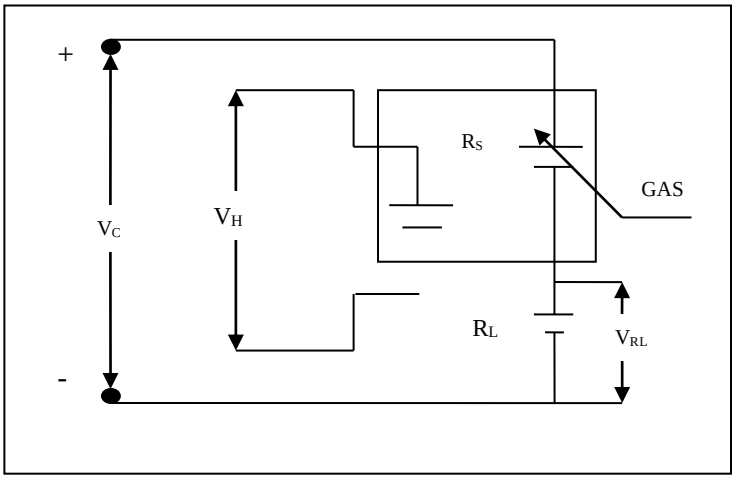


Figure 4. Circuit diagram of Methane Sensor

Parameters	Value
(V_C) and (V_H)	5.0V ± 0.2V AC/DC
Operating & storage temperature	-40˚C ~ +70˚C
Load resistance (R_L)	(0.45kΩ min)

Table 3. Methane Sensor Specifications

5.5. Data Transmission

In MAFS-WSN, after node organization and schedule generation, the consequent step is data transmission. Sensor nodes collect data and transfers to CH; CH sends acknowledgment to the MS. The sink moves towards the CH and collects data and sends to the BS medium of gateway. The flow chart process is to finding gasconcentration in the network is demonstrated in Figure 5.

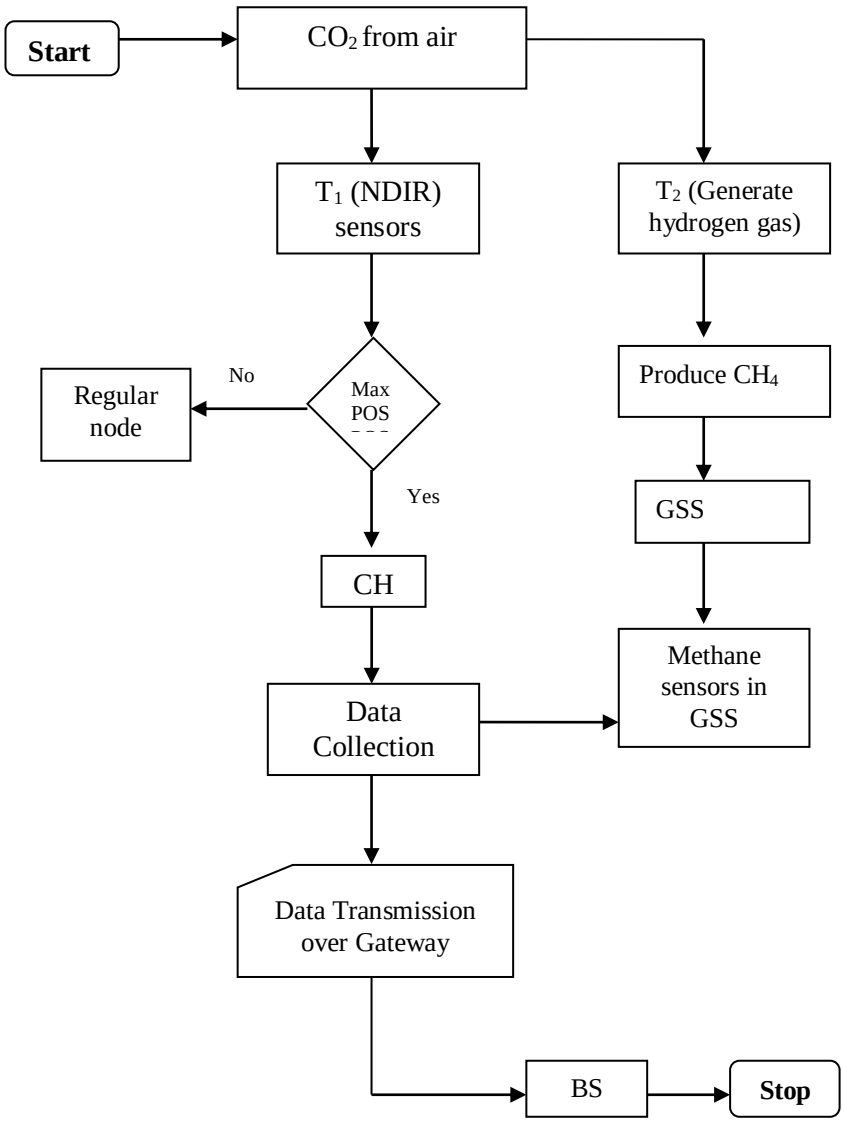


Figure 5. Flow chart of SBC-MS

6. SIMULATION RESULTS

The mathematical analysis was demonstrated using simulations on MATLAB [17, 18] in which 100 nodes are deployed randomly in 600m x 600m region. The initial energy of each node is set to be 5J. A comparative analysis of SBC-MS with the earlier clustering technique MLEACH was performed with the simulation parameters stated in Table 4 and a variation of graphs were plotted which ultimately prove SBC-MS to outperform MLEACH.

Table 4. Simulation Parameters

Parameters	Values
Network Size	600 x 600
Number of Nodes	100
Initial Energy	5J
Number of Sink	1
Transmission Range	25m
Sink Speed	5m/s

6.1. Performance Evaluation

Concentration of CO_2: The results of the CO_2 concentration performed with the NDIR sensor. Figure 6. shows the concentration of CO_2 in terms of PPM at an operating temperature of 20^0c. The dashed line indicates the amount of CO_2 gas in a certain region.

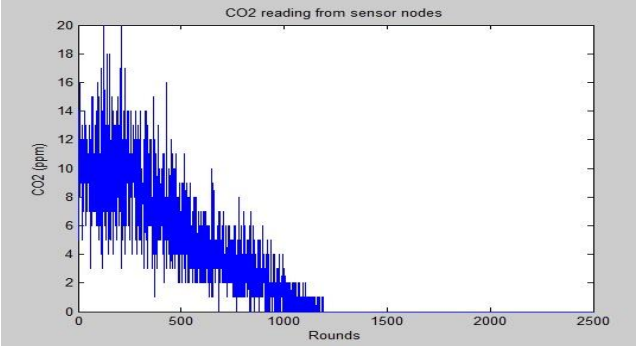


Figure 6. Concentration of CO_2

Network Lifetime: Network lifetime is quantified in terms of the total number of nodes alive over different ranges of common rounds. The analysis results prove that all the 100 nodes are alive after the completion of rounds in SBC-MS. Figure 7. compares the proposed SC-MS with the existing MLEACH in terms of network lifetime [16].

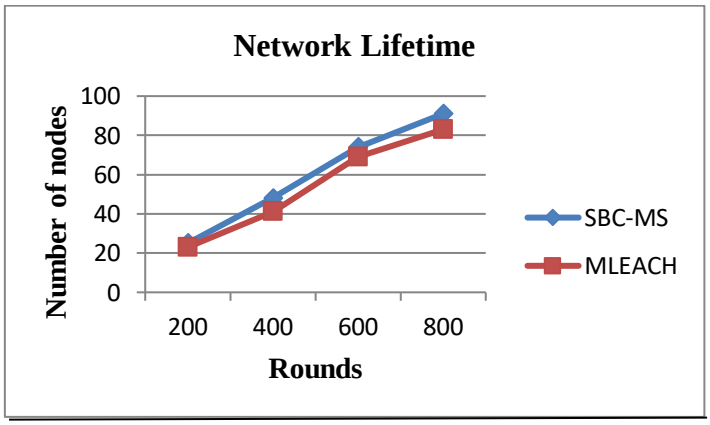


Figure 7. Network Lifetime

End-to-End Delay: The simulation work attempts to quantify end to end delay (in seconds) of the proposed SBC-MS and MLEACH subjected to an increasing number of sensor nodes deployed. The SBC-MS seems to be convincing in terms of delay, when compared to MLEACH is represented in Figure 8 [16]. Since MSs is involved in data collection task, transmission delay

reduces phenomenally in SBC-MS.

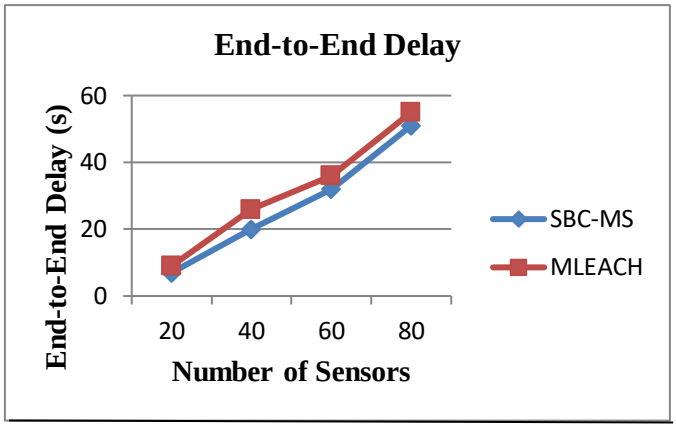


Figure 8. End-to-End Delay

Date Rate: The amount of data transmitted from CH to MS is quantified in bps as shown in Figure 9 [16]. SBC-MS outperforms MLEACH in terms of data rate thereby avoiding remote transmission.

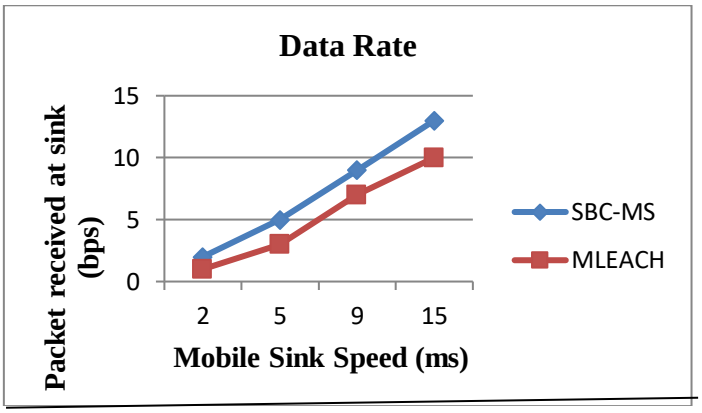


Figure 9. Data Rate

7. CONCLUSION

The fuel system was successfully developed for the direct use of hydrate as a source of fuel for automotive engines. Also, the proposed MAFS-WSN exploits solar energy which seems to be an effective method of hydrate dissociation for automobiles. The modification in the conventional gas transport system reduces the cost of methane extracted from biogas that can further complement to energy independent technologies thereby assisting in utilization of renewable energy. The MAFS-WSN is proven to be better in terms of schedulability and reliability with the proposed SBC-MS algorithm.

REFERENCES

[1] Movva Pavani and P.Trinatha Rao, "Real Time Pollution Monitoring Using Wireless Sensor Networks,"Information Technology, Electronics and Mobile Communication Conference (IEMCON), 2016.

[2] Alexander Malaver, Nunzio Motta, Peter Corke and Felipe Gonzalez,"Development and Integration of a Solar Powered Unmanned Aerial Vehicle and a Wireless Sensor Network to Monitor Greenhouse Gases" Sensors, Vol.15, PP. 4072-4096, 2015.

[3] J.Sunil kumar, A.Dileep,"Wireless Gas Sensor Network for Detection and Monitoring of Harmful Gases in Utility Areas and Industries" International Journal of Innovative Engineering Research, Vol. 2, Issue 1, 2014.

[4] B. Shiva Kumar, T. Rama krishnaiah, "GSM technology based Wireless Sensor Network for Gas Monitoring" International Journal of Science, Engineering and Technology Research, Volume 3, Issue 9, September 2014.

[5] Nadime Azizi, Alecia Copeland, John Chun, Matt Ell, Khushbu Kanani, and Zuhair Khoury, "A Study of Methane Sensors in Internet-of-Things Technology" Proceedings of Student-Faculty Research Day, 2016.

[6] M. Udin Harun Al Rasyid, Isbat Uzzin Nadhori and Yodhista Tulus Alnovinda,"CO and CO2 Pollution Monitoring Based on Wireless Sensor Network" IEEE International Conference on Aerospace Electronics and Remote Sensing Technology, 2015.

[7] David Chavez M, River Quispe T, Jorge Rojas M, Andres Jacoby K and Guillermo Garayar L, "A Low-Cost, Rapid-Deployment and Energy-Autonomous Wireless Sensor Network for Air Quality Monitoring" International Conference on Sensing Technology, 2015.

[8] Suganya E, Vijayashaarathi S, "Smart Vehicle Monitoring System for Air Pollution Detection using Wsn" International Conference on Communication and Signal Processing, 2016.

[9] Bambang Sugiarto, Rika Sustika,"Data Classification for Air Quality on Wireless Sensor Network Monitoring System Using Decision Tree Algorithm" International Conference on Science and Technology-Computer, 2016.

[10] Ke Hu, Ashfaqur Rahman, Vijay Sivaraman and Pradeep Ray, "Improving Air Pollution Forecast with Ubiquitous Mobile Sensor Network" International Conference on Ubiquitous and Future Networks (ICUFN), 2014.

[11] R. Lippi, S. C. Howard, H. Barron, C. D. Easton, I. C. Madsen, L. J. Waddington, C.Vogt, M. R. Hill, C. J. Sumby, C. J. Doonan, and D. F. Kennedy, "Highly Active Catalyst for CO2 Methanation Derived from a Metal Organic Framework Template" Journal of Materials Chemistry A, PP.1-9, 2017.

[12] Jun Zheng, Abbas Jamalipour, "Introduction to Wireless Sensor Networks" Institute of Electrical and Electronics Engineers, 2009.

[13] Jasmeen Kaur, Viacheslav I. Adamchuk, Joann K. Whalen and Ashraf A. Ismail, "Development of an NDIR CO2 Sensor-Based System for Assessing Soil Toxicity Using Substrate-Induced Respiration" Sensors, Vol.15, PP. 4734-4748, 2015.

[14] Yongmin Zhang, Shibo He and Jiming Chen,"Near Optimal Data Gathering in Rechargeable Sensor Networks with a Mobile Sink" IEEE Transactions on Mobile Computing, Vol.16, Issue.6, 2017.

[15] Luciano B. Mendes, Nico W. M. Ogink, Nadège Edouard, Hendrik Jan C. van Dooren , Ilda de Fátima F. Tinôco and Julio Mosquera," NDIR Gas Sensor for Spatial Monitoring of Carbon Dioxide Concentrations in Naturally Ventilated Livestock Buildings" Sensors,Vol.15, PP.11239-11257, 2015.

[16] A.Rehash Rushmi Pavitra, E.Srie Vidhya Janani, "A Diplomatic Data Collection in Wireless Sensor Networks using MLEACH Algorithm" International Journal of Computer Sciences and Engineering, Vol.6, Issue.7, PP.2347-2693, 2018.

[17] Onwusuru I, Okolo Chidiebere C, Uka Chukwuma, Ohuabunwa Austine and Nwafor Chibuikem, "Introduction to MATLAB for Researchers and Engineering Students" Journal of Scientific and Engineering Research, Vol.4(6), PP.176-180, 2017.

[18] David Houcque "Introduction to Matlab for Engineering Students", 2005.

[19] Dahlila Putri Dahnil, Yaswant Prasad Singh and Chin Kuan Ho,"Connectivity-Aware and Minimum Energy Dissipation Protocol in Wireless Sensor Networks" International Journal of Distributed Sensor Networks, Vol.9, Issue.7, 2013.

AUTHORS

A. Rehash Rushmi Pavitra obtained her Bachelor of Engineering Degree in Computer Science and Engineering from Hindusthan College of Engineering and Technology, Coimbatore and received her M.E degree from Anna University Regional Campus, Madurai. She is a Research Scholar carrying out her research in Underwater Wireless Sensor Networks. Her main research interests include Underwater Wireless Sensor Networks with emphasis on Energy Efficiency and Data Aggregation.

Dr.E.Srie Vidhya Jananiis currently working as an Assistant Professor, in the department of Computer Science and Engineering at Anna University Regional Campus, Madurai. Also she obtained his Ph.D degree in Information and Communication Engineering from Anna University Chennai. She has published 15 research papers in reputed International, national journal and conferences. Her current areas of interests are Enhancing Energy Conservation in Wireless Sensor Networks, and Network Security.

AN EFFICACIOUS RUNTIME ADAPTIVE HYBRID DRAM/PRAM MEMORY IN FPGA PLATFORM

M. Isaivani[1], Dr. V. Malathi[2] and Dr.E.Sakthivel[3]

[1]Ph.D Scholar - Electrical Engineering, Anna University Regional Campus Madurai, Madurai, Tamil Nadu, India
[2]Professor, Department of Electrical and Electronics Engineering, Anna University Regional Campus Madurai, Madurai, Tamil Nadu, India
[3]Associate Professor, PSR Engineering College, Sivakasi, Tamil Nadu, India

ABSTRACT

Hybrid main memory comprising of DRAM and PRAM becomes quite popular because of the less standby power benefit of PRAM and high performance of DRAM. In this work, the runtime-adaptive control and DRAM bypassing methods are introduced in order to minimize DRAM refresh energy that occupies a considerable portion of total system power. The work is carried out by using Xilinx 12.1 simulation tool and the experimental result proves that in the proposed work power consumption is greatly reduced i.e., only requires 3 %, with less area overhead while maintaining the speed parameter by comparing with the conventional method .

KEYWORDS

Cache memory, Dynamic Random Access Memory, Phase-Change Random Access Memory, Write-back and Fill method

1. INTRODUCTION

Currently, Very Large Scale Integration (VLSI) circuits are miniature in size to promote device functionalities and performance parameters. DRAM becomes a performance impediment in many systems due to the pin count, speed and pin bandwidth are risen extremely slowly. DRAM is one of the highest power consumers in modern computing systems. So that, power budget of DRAM is quite similar to or sometimes, even surpasses the power budget of CPU. It is proven that DRAM in a commercial system uses 25–45% of total system power. With this scenario, energy efficient DRAM has become a crucial design constraint for the system design.

Even DRAM performance emerges as a critical issue in the modern server systems because of the universal utilization of data-centric applications. Since DRAM bandwidth is not scalable and considered as a limited resource, huge contention exists in DRAM that debases total system performance significantly. To enhance DRAM performance and to lower dynamic-energy consumption, the row-level access locality should be enhanced and the count of row activations should be decreased. The row activations are considerably reduced by performing more read and write operations for each activated row. More row activations result in higher wastage of energy.

N. Ramasubramanian et al.(Eds) : SRAIC-2019
pp. 47-57, 2019. © CS & IT-CSCP 2019 DOI: 10.5121/csit.2019.91504

This paper analyzes DRAM activities and implements cache line write-backs and fill methods together with the hybrid DRAM/PRAM memory .In the proposed hybrid main memory, PRAM operates as a background main memory due to its low stand-by power benefit and DRAM serves as a cache owing to its low latency and lower power consumption during read and write operations. This hybrid main memory system takes advantage of both memories while reducing the negative aspect of limitations in both of them.

2. LITERATURE SURVEY

A brief survey of various techniques involved in data compression is presented for main memory and cache memory [1]. A set- and-way management approach is proposed in [2] for a runtime-reconfiguration of a cache's size and associativety. Deterministic nap technique and early miss detection approach are proposed in [3] in order to diminish static as well as dynamic power. "Latency-Programmable System Emulation Memory" is implemented in [4] that permits read-and/or-write latency scale-up capability. Direct data access can be achieved in eDRAM cache by proposing tag-comparison in memory that enhanced energy efficiency [5]. The "eXplicitMulti-Threading (XMT)" paradigm is designed for a Parallel Random Access Model on-chip processor [6].PRAM-On-Chip Phase Change Memory (PCM) provides higher capacity than DRAM and evolves for a greater capacity memory [7,8, 9, 10]. Gen2 Hybrid Memory Cube is characterized from data-centric demands. HMC offers considerable accessing bandwidth while requiring less power [11, 12]. Novel write algorithms for PCM are discussed detail in [13]. Retention-aware placement method is employed in DRAM to lessen refresh power [14]. In [15], statistical populations' method is proposed for DRAM cache and also inherent error-control technique is utilized to minimize refresh rate. Different techniques are discussed for utilizing memory controller in order to enhance energy efficiency of DRAM and also to manage power in DRAM [16]. Another multi-partition based memory controller BIBIM is designed that combines DRAM and PRAM [17]. Memory access scheduling technique is introduced in [18] that reorder memory references to improve the energy efficiency. An effective Collective write-back and fill method is employed for DRAM cache in order to enhance the data throughput [19].

3. EXISTING SYSTEM

Collective Write-back-cum-Fill method [19] consists of the following two approaches: write-back strategy and fill strategy. It is executed by the feedback exists between Dynamic-Write-back-Unit (DWU) and Adaptive DRAM Placement (ADP) entities. The write-back strategy is carried out by DWU. When L3cache replacement occurs, checking is done on the victim line to find if it is dirty. If there is no any modified bit, the victim line is evacuated from L3cache without writing back to the DRAM cache. If the victim line is dirty, DWU will decide if write-back is to be done on DRAM cache. The line is added to the DRAM cache if affirmative decision is taken. Or else, DRAM cache hit/miss will be verified. The line should be introduced into DRAM cache with the condition that is a hit in order to maintain regularity. If not, the line is infused into main memory. Fill strategy is carried out by ADP entity which decides whether to add fill requests to DRAM cache.

The CWFP method requires two vital units: Integrated Set Monitors (ISM) and Lose-to-Gain Dispatcher (LGD). Based on the investigation of DRAM cache accessing management, the module ISM determines which activity to be performed on DRAM cache i.e., write-back or fill operation .An another appropriate entity called, Miss-Status Handling Register (MSHR) includes W and F bits to decide for write-back and fill cache operations respectively. This system offers LGD over ISM in the aim to avert needless write-back access to DRAM cache and it also aids to rectify the feasible wrong perception of ISM. Remarkably, LGD supports the

ISM's decision making capability and in the way DRAM interference got reduced. Moreover it evaluates the accuracy of write-back access based on per-core criteria and it curtails the cache resources allotment to useless write-backs.

- Though existing CWFP scheme reduced DRAM interference, inter-core contention and achieved greater speedup, it still suffered with higher power consumption of DRAM. The major amount of total power available in the system is consumed by this unit.
- The following section describes the proposed hybrid DRAM/PRAM scheme to address the above challenge.

4. PROPSED SYSTEM

4.1. PRAM Overview

DRAM has been adopted for the main memory in computer systems for several years. Many non-volatile memories like Phase change RAM (PRAM), Magnetic RAM (MRAM) and Ferroelectric RAM (FRAM) are developed for future generation technologies. In these non-volatile memories (NVM), PRAM becomes popular entity for main memory due to its advantageous properties of low power requirement and high density. A PRAM cell is made up of phase change material for bit representation. PRAM density is very much larger than DRAM (expected to be about four times). Moreover, unvarying property of phase material after power-off, it exhibits petty leakage energy irrespective of memory size.

4.2. Implementation

In this effective hybrid DRAM/PRAM method, DRAM plays as a last-level cache and operates as the working memory while PRAM performs as a massive background main memory. Figure 1 shows the architecture of this hybrid memory, where the memory controller manages the tag structure in DRAM and the counter governs each row in DRAM. By decaying the DRAM contents, power management can be achieved. If the data are clean, they are expelled from DRAM. For the modified data, they should be written back to PRAM before eviction. When the new data are written to DRAM which has been read from PRAM, global time-out value is set to the counter. The counter value is decreased by one periodically. It is again set to the time-out value after row access takes place. When the counter reaches zero, the row will be expelled. That removed row does not need refresh which leads to attain considerable energy saving. The following two methods are utilized to manage the power in the proposed scheme.

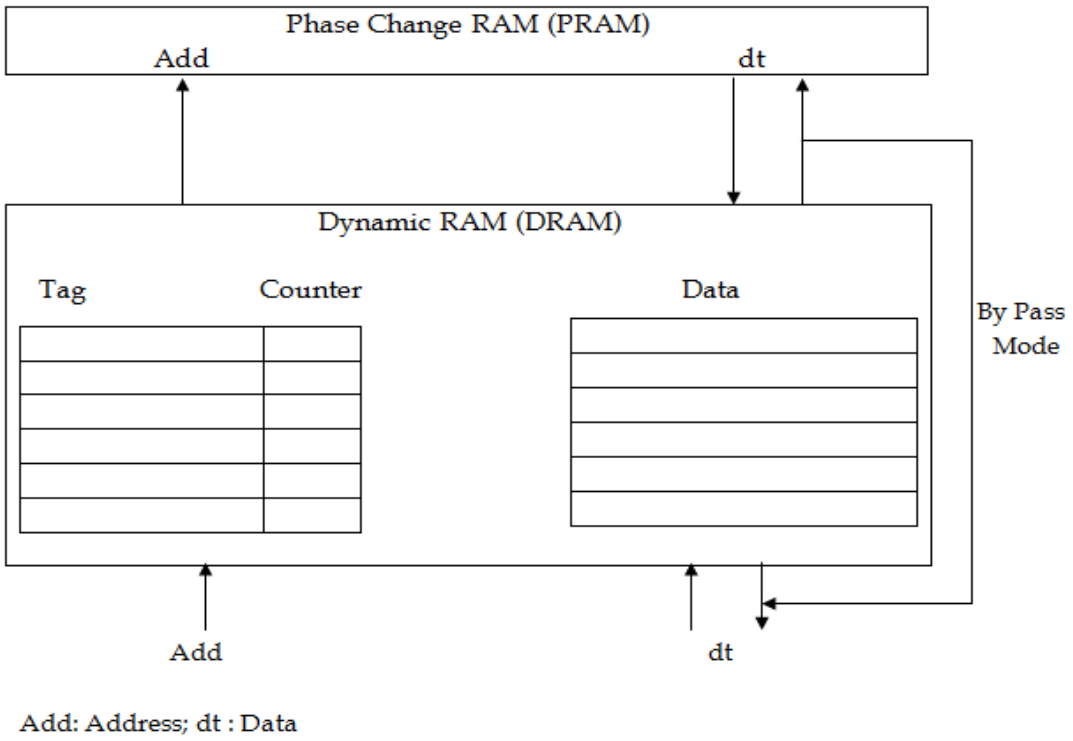


Figure 1. Hybrid DRAM/PRAM Memory Scheme

4.2.1. Runtime-Adaptive Control of Time-Out Value

This method is performed that reduces the total energy while satisfying system performance constraints. When time-out value increases, many rows in DRAM would be live and needs refreshes and so DRAM energy rises. But PRAM energy decreases and PRAM accesses are less because much data are accessed by DRAM with a huge hit rate. There is a best time-out value (BTO) that provides less total energy of the hybrid scheme by averting DRAM refreshes. The BTO value changes because of the dynamically varying manner in memory access.

4.2.2. Bypassing DRAM

DRAM bypassing is performed to the first read operation that fetches a miss in DRAM cache. When in the second access to the corresponding row in DRAM within the time-out value, the data in row are replicated to DRAM from PRAM and that row begins to be refreshed to perform further accesses. This method screens out memory accesses that have poor spatial locality and to enhance the DRAM refresh energy efficiency.

5. RESULTS AND DISCUSSION

The proposed system is implemented in Xilinx 12.1 tool and written in VHDL (Very large scale integration Hardware Description Language) coding to perform evaluation for both existing cache write-back and fill method with proposed runtime-adaptive hybrid DRAM/PRAM schemes.

5.1. Performance Parameters of Existing System

5.1.1. Area Consumption

The area requirements of slice registers, LUT, LUT –flip-flop pairs, bonded IOB buffers are 41, 44, 40, 18,1 respectively as shown in figure 2.

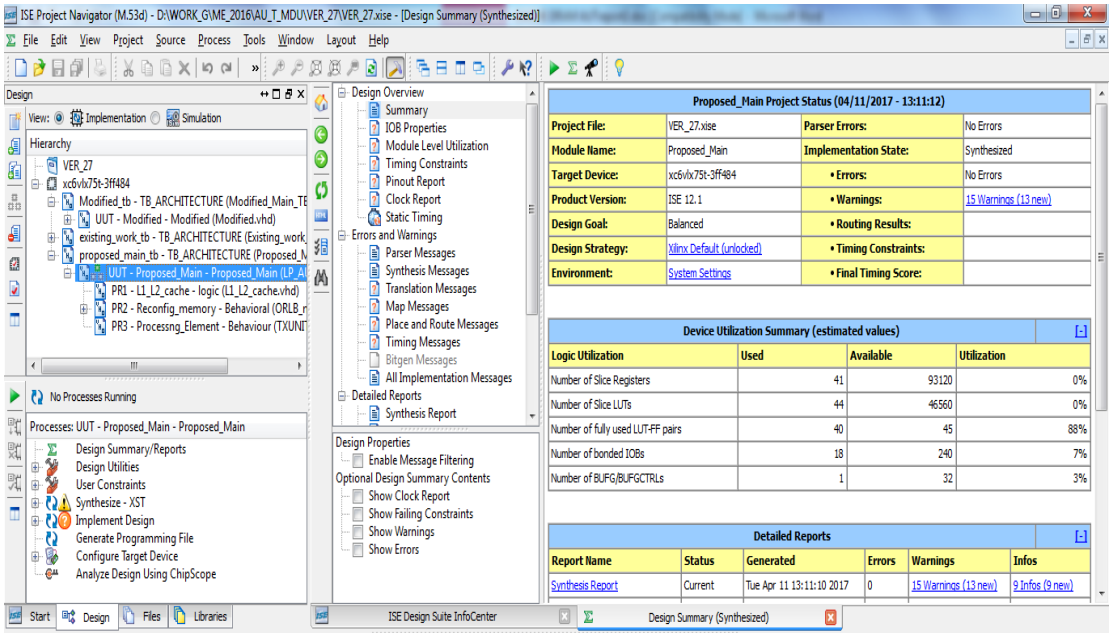


Figure 2. Area consumption of Existing System

5.1.2. Speed Evaluation

The output shows the minimum required time and maximum frequency are 1.425ns and 701.991MHz respectively. The minimum input arrival time before clock, maximum output required time after clock, maximum combinational path delay are 0.929ns, 0.567ns, 0.289ns respectively. It is shown in figure 3.

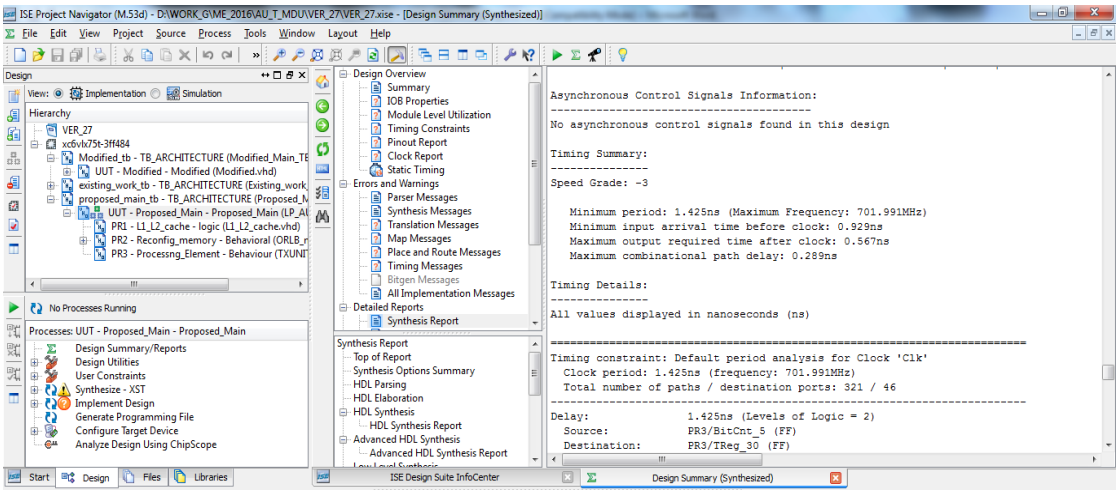


Figure 3. Speed Evaluation of Existing System

5.1.3. Power Consumption

The existing system which involves the collective write-back and fill method, requires 7.6% of total power available. It is computed from figure 4.

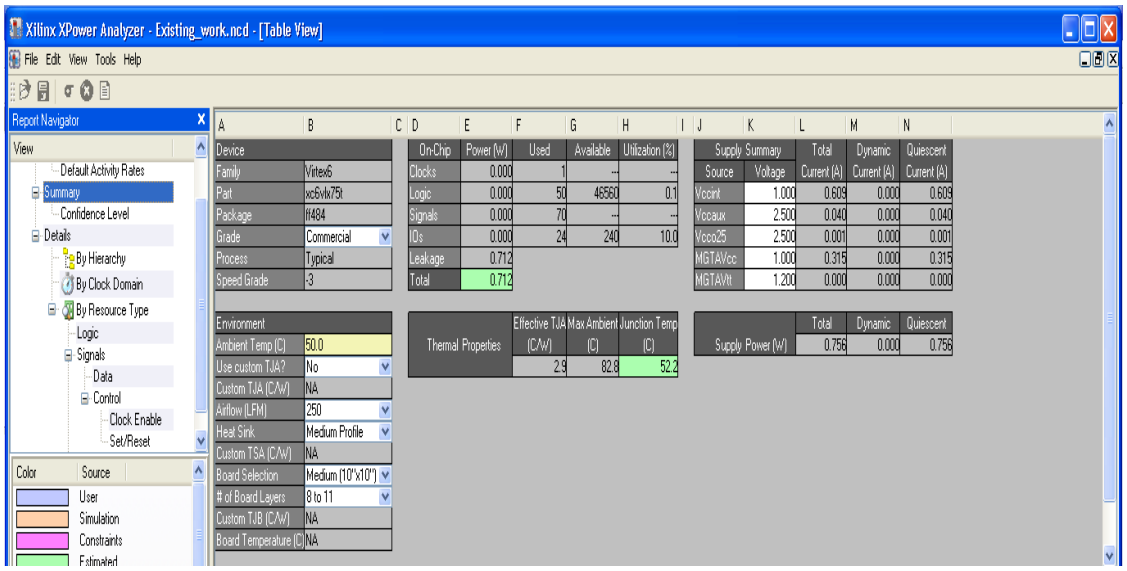


Figure 4.Power Consumption of Existing System

5.2. Performance Measurement of Proposed System

5.2.1. Area Consumption

The area requirements of slice registers, LUT, LUT –flip-flop pairs, bonded IOB buffers are 39,44,39,7,1 respectively as shown in figure 5. Thus the area consumption is reduced from the existing system.

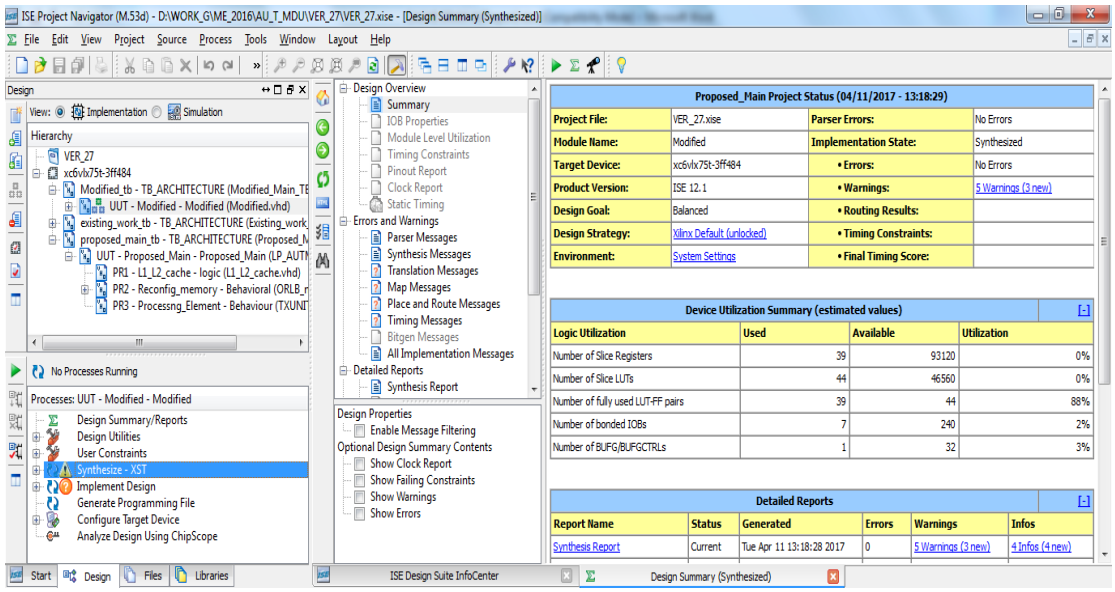


Figure 5. Area consumption of Proposed System

5.2.2. Speed Evaluation

The output shows the minimum required time and maximum frequency are 1.425ns and 701.991MHz respectively. The minimum input arrival time before clock, maximum output required time after clock are 0.920ns, 0.562ns respectively. It is shown in figure 6. The output of speed measurement is as same as the conventional method and this has to be enhanced in the future work. The delay is slightly better than the existing method.

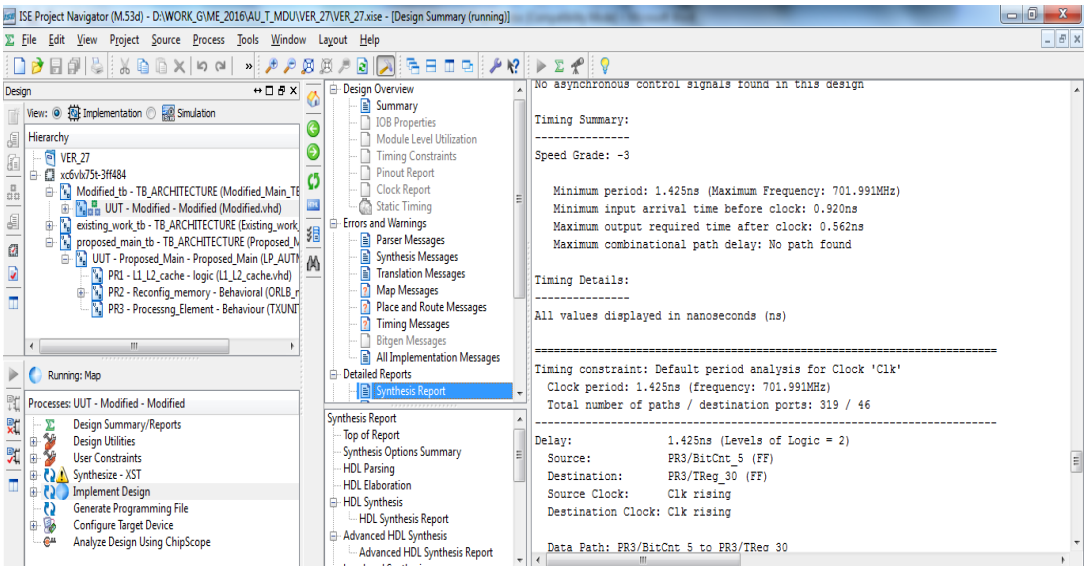


Figure 6. Speed Evaluation of Proposed System

5.2.3. Power Consumption

The proposed run-time adaptive hybrid DRAM/PRAM memory with cache write-back and fill method requires only 3% of total power which is greatly diminished while comparing with the conventional method. It is calculated from figure 7.

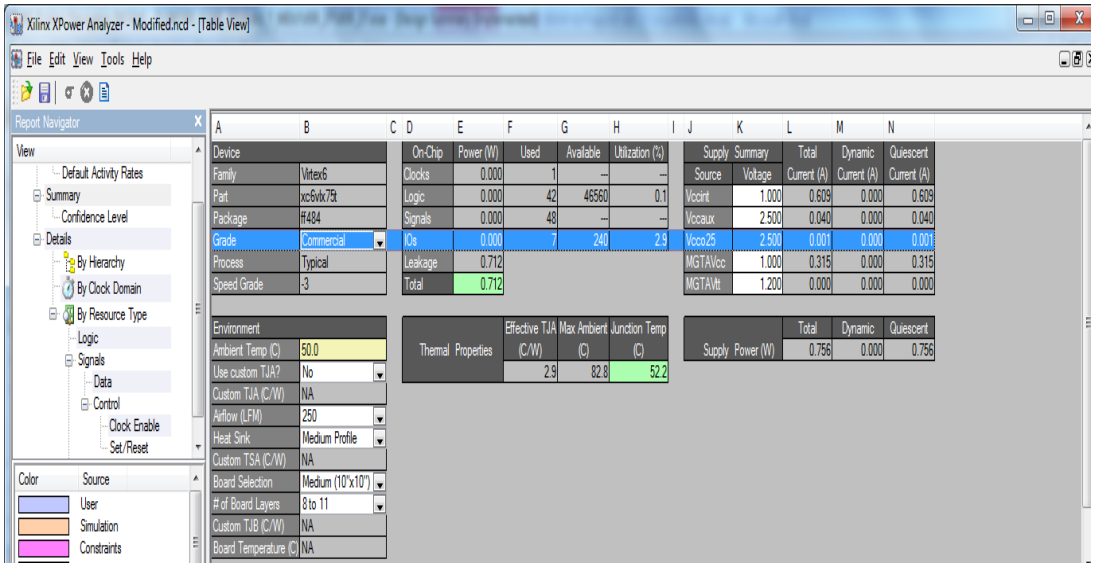


Figure 7. Power consumption of Proposed System

5.3. Simulation Waveforms

5.3.1. Existing System

The simulated result of DRAM cache with collective write-back and fill method is shown in below figure 8.

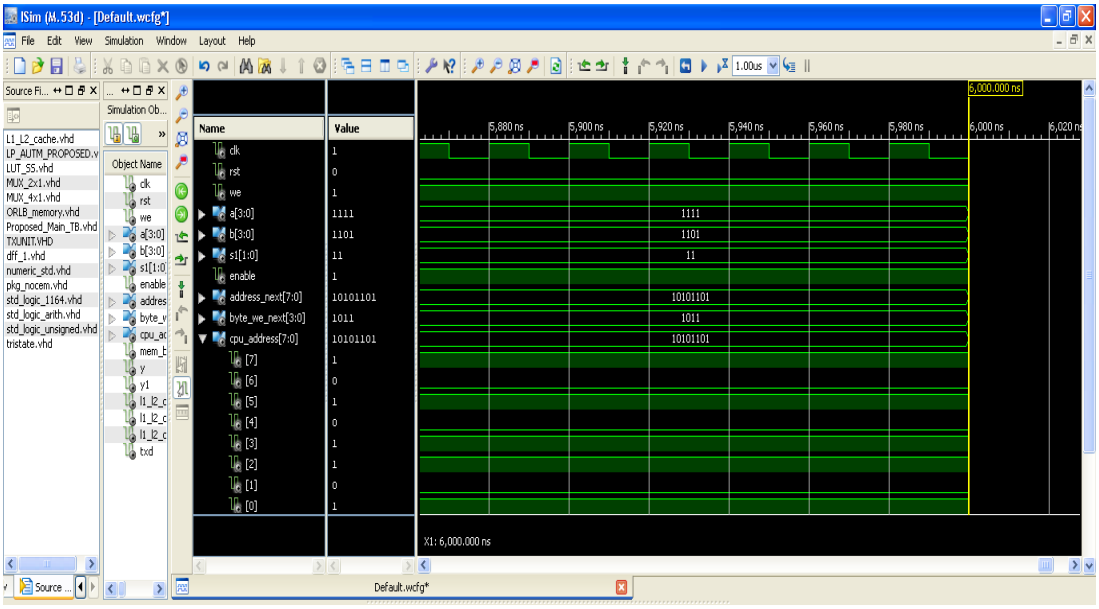


Figure 8. The Simulated Result of Existing System

5.3.2. Proposed System

The simulated result of hybrid DRAM/PRAM memory with cache collective write-back and fill method is shown in below figure 9.

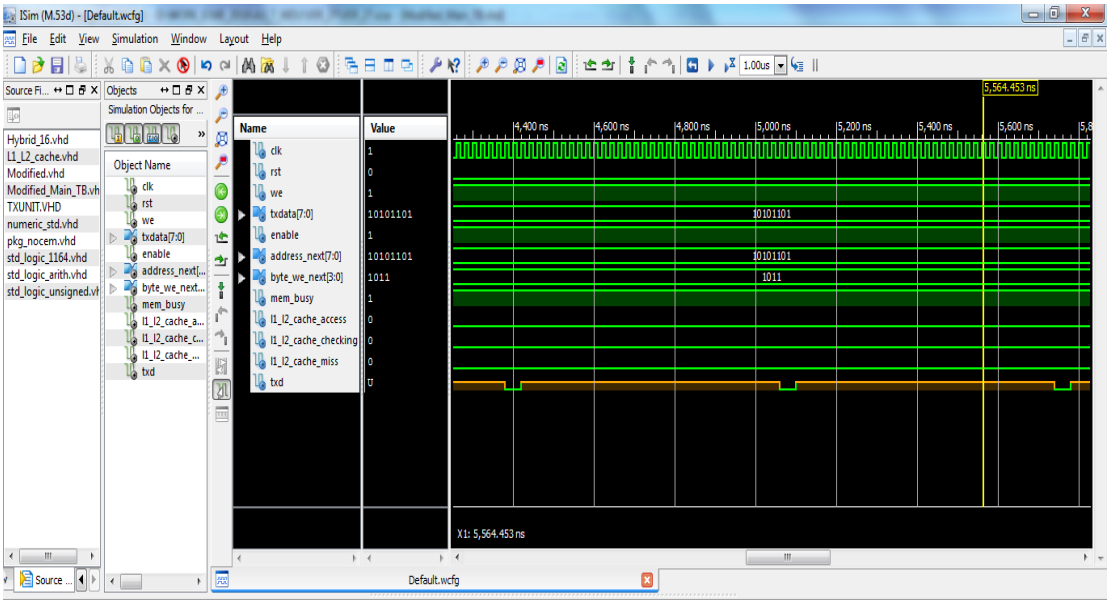


Figure 9. The Simulated Result of Proposed System

5.4. Performance Comparison

Table 1 Comparison Analysis

S. No	Approaches	Area	Power	Latency
1	Latency-Programmable System Emulation Memory [4]	NA	NA	120 ns
2	PRAM-On-Chip Processor [6]	NA	NA	193 ms
3	Hybrid Memory Cube[11]	NA	11w	68 ns
4	3D Stacked Memories [12]	NA	105 w	24 µs
5	BIBIM [17]	NA	NA	0.13 µs
6	CWFP [19]	SR - 41 LUT - 44 LUT-FF- 40 IOB - 18 Buffer - 1	71 mw	0.929 ns
7	Proposed Run-time Adaptive Hybrid DRAM/PRAM memory	SR - 39 LUT - 44 LUT-FF - 39 IOB - 7 Buffer - 1	21 mw	0.920 ns

Table 1 shows the comparison of area, power and latency parameters for various methodologies with the proposed approach. It is evident that the proposed methodology outperforms all other mentioned approaches in terms of the stated performance metrics.

6. CONCLUSION AND SCOPE OF FUTURE WORK

6.1. Conclusion

Thus, the system focuses on the new approach to reconfigure optimizing Hybrid DRAM/PRAM performance and energy consumption. Under this technique, dirty cache lines which are not been accessed recently have been written to DRAM while the respective row is activated by a read operation. This permits both read and write operations to target the particular one. The proposed hybrid memory offers lower standby power as well as higher performance for the server systems. In the proposed work power consumption isgreatly reduced i.e., only requires 3%, and it results with less area overhead while maintaining the speed parameter by comparing with the conventional method.

6.2. Future Scope

Future work should be done to verify the suitability of using the scheme proposed in this approach qualitatively and quantitatively on multi-core systems. Thus, the proposed scheme would need to be qualitatively and quantitatively evaluated, analyzed and improved in more detail to be efficiently working in multi, or even many-core systems.

REFERENCES

[1] Sparsh Mittal , Jeffrey S. Vetter, (2016) "A Survey Of Architectural Approaches for Data Compression in Cache and Main Memory Systems", IEEE Transactions on Parallel and Distributed Systems,Vol. 27, No. 5, pp1524 – 1536.

[2] Karthik T. Sundararajan, Timothy M. Jones, Nigel P. Topham, (2013) "The Smart Cache: An Energy-Efficient Cache Architecture Through Dynamic Adaptation", International Journal of Parallel Programming, Vol. 41, No. 2, pp305–330.

[3] Oluleye D. Olorode, MehrdadNourani, (2015) "Improving Cache Power and Performance Using Deterministic Naps and Early Miss Detection", IEEE Transactions on Multi-Scale Computing Systems, Vol. 1, No. 3, pp150 – 158.

[4] Mu-Tien Chang, I. Stephen Choi, DiminNiu, Hongzhong Zheng, (2018) "Performance Impact of Emerging Memory Technologies on Big Data Applications: A Latency-Programmable System Emulation Approach",GLSVLSI'18, Chicago, IL, USA.

[5] Keng-Hao Yang, Hsiang-Jen Tsai, Chia-Yin Li, Paul Jendra, Meng-Fan Chang, Tien-Fu Chen, (2017) "eTag: Tag-Comparison in Memory to Achieve Direct Data Access based on eDRAM to Improve Energy Efficiency of DRAM Cache", IEEE Transactions on Circuits and Systems, Vol. 64, No. 4, pp858 – 868.

[6] XingzhiWen , Uzi Vishkin, (2008) "FPGA-Based Prototype of a PRAM-On-Chip Processor", CF'08, Ischia, Italy.

[7] JaeminJang,Wongyu Shin, JungWhan Choi , Yongju Kim, Lee-Sup Kim, (2019) "Sparse-Insertion Write Cache to Mitigate Write Disturbance Errors in Phase Change Memory", IEEE Transactions on Computers, Vol. 68, No. 5, pp752 – 764.

[8] M. Abdulla, and M. Greenberg, (2010)"Will Phase Change Memory (PCM) Replace DRAM or NAND Flash?", Flash Memory Summit.

[9] B. C. Lee, *et al.,* (2009)"Architecting Phase Change Memory as a Scalable DRAM Alternative", ISCA '09 Proceedings of the 36th annual international symposium on Computer architecture, pp2-13, Austin, TX, USA.

[10] M. K. Qureshi, V. Srinivasan, and J. A. Rivers, (2009) "Scalable High Performance Main Memory System Using Phase-Change Memory Technology", ProceedingISCA '09 Proceedings of the 36th annual international symposium on Computer architecture, pp24-33, Austin, TX, USA.

[11] MayaGokhale, Scott Lloyd, Chris Macaraeg, (2015) "Hybrid Memory Cube performance characterization on data-centric workloads", ProceedingIA3 '15 Proceedings of the 5th Workshop on Irregular Applications: Architectures and Algorithms, Article No. 7, Austin, Texas, USA.

[12] RamyadHadidi, BaharAsgari, Burhan Ahmad Mudassar, SaibalMukhopadhyay, SudhakarYalamanchili, and Hyesoon Kim, (2017) "Demystifying the Characteristics of 3D-StackedMemories: A Case Study for Hybrid Memory Cube", In: 2017 IEEE International Symposium on Workload Characterization (IISWC), IEEE, USA.

[13] T.Nirschl, et al., (2007) "Write Strategies for 2 and 4-bit Multi-Level Phase-Change Memory", In: 2007 IEEE International Electron Devices Meeting, IEDM, USA.

[14] R. K. Venkatesan, S. Herr, and E. Rotenberg, (2006) "Retention-Aware Placement in DRAM (RAPID): Software Methods for Quasi-Non-Volatile DRAM", In: The Twelfth International Symposium on High-Performance Computer Architecture, HPCA, USA.

[15] P. G. Emma, *et al.*, (2008)"Rethinking Refresh: Increasing Availability and Reducing Power in DRAM for Cache Applications", IEEE MICRO, Vol. 28, No. 6, pp47-56.

[16] I. Hur and C. Lin, (2008) "A Comprehensive Approach to DRAM Power Management", In: 2008 IEEE 14th International Symposium on High Performance Computer Architecture, HPCA, IEEE, USA.

[17] Gyuyoung Park1, Miryeong Kwon1, Pratyush Mahapatra2, Michael Swift2, and Myoungsoo Jung, (2018) "BIBIM: A Prototype Multi-Partition Aware Heterogeneous New Memory", 10th {USENIX} Workshop.

[18] S. Rixner, *et al*., (2000)"Memory Access Scheduling", Proc. ISCA.

[19] Shouyi Yin, Weizhi Xu, Jiakun Li, Leibo Liu, Shaojun Wei, (2016) "CWFP: Novel Collective Writeback and Fill Policy for Last-Level DRAM Cache", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 24, No. 7, pp2548 – 2561.

AUTHORS

M Isaivani received B.E degree in Electronics and Instrumentation Engineering from Anna University in the year of 2006. She has completed M.E in Embedded System Technologies under Anna University in 2014. She is currently doing Ph.D. in full-time at Anna University Regional Campus Madurai. Her research interests include VLSI, Embedded System applications to Power System Protection.

V Malathi is working as a professor in the department of Electrical and Electronics Engineering and Dean in Anna University Regional Campus Madurai. She completed her Bachelor Degree in College of Engineering Guindy and her Master's Degree in Thiyagaraja College of Engg, Madurai. She Completed her Ph.D. in Anna University Chennai and her areas of interest are Intelligent Techniques and its Applications, Smart Grid, FPGA based Power System and Automation.

E Sakthivelreceived the Bachelor degree in Madurai Kamarajar University, Madurai and the Master's degree in Embedded system Technologies in Anna University, Thirunelveli and he completed his Ph.D. degree in Anna University, Chennai. Currently, he is working as an associative professor at PSR Engineering College. He has more than 10 years of industrial experience in VLSI Technology and Embedded System. His current research interests include Embedded Systems, Low-Power Design, Network On Chip, System-On-Chip, FPGA and ASIC based power electronics control circuits, FPGA based power system, Wireless Networks, Instrumentation and Object Recognition.

ATTRACTOR INFLUENCED PRNG FOR CRYPTOGRAPHIC KEY GENERATION ON FPGA

Hemanth Kumar Nalajala, Rajesh B, Sivaraman R, Sridevi A,
Amirtharajan Rengarajan and Sundararaman Rajagopalan

School of EEE, SASTRA Deemed to be University, Thanjavur, Tamilnadu

ABSTRACT

Random numbers play a significant role while implementing the crypto architectures on reconfigurable hardware. Chaotic attractors are reliable sources of deterministic random number generation due to their large keyspace capability. Chaos exhibits random perturbations in floating-point units which is a challenge while replicating the system of equations on hardware. The conversion of floating-point numbers to binary representation will take many quantization possibilities which certainly affect the randomness and sensitivity to initial conditions. This work aims to implement the chaotic Rössler attractor based Pseudo Random Number Generation (PRNG) on FPGA through simulation and real time experimentation. This attractor has been realized on Altera Cyclone II EP2C20F484C7 FPGA using hardware primitives. It required 201 LUTs with a power dissipation of 78.48 mW and time duration of 4 µS to generate 32,768 random bits. The randomness of this attractor was evaluated through entropy, correlation, bit distribution and NIST SP 800 – 22 analyses.

KEYWORDS

Chaos, PRNG, Quantization effects, Reconfigurable Hardware, Rössler attractor, Differential equations & FPGA

1. INTRODUCTION

Advancements in networking have revolutionized the communication in a commendable manner. Considering the huge amount of data being shared over the internet, it is necessary to preserve the various facets of information security. Cryptographic algorithms have a significant role in enhancing the confidentiality of data by all means [1]. In cryptography, key generation occupies a primary role for both the symmetric as well as asymmetric approaches. Random keys play a decisive role in improving the quality of cipher generated. Generally, keys are generated through Random Number Generators (RNGs) which are classified into two categories namely Pseudo Random Number Generator (PRNG) and True Random Number Generator (TRNG) [2]. Noticeably, PRNGs have been utilized widely in data encryption because of their high level of randomness. They employ mathematical equations or fixed architecture driven by a unique applicable initial condition and/or seed value [3]. Recently, hardware accelerated PRNG implementations are in greater demand due to the high speed requirements. Especially, Field Programmable Gate Array (FPGA) based PRNG algorithms have attained a substantial requirement due to their unique characteristics such as reconfigurability, algorithm agility, concurrency, faster time to market, easy prototyping and other on – chip / off – chip capabilities [4].

N. Ramasubramanian et al.(Eds) : SRAIC-2019
pp. 59-70, 2019. © CS & IT-CSCP 2019 DOI: 10.5121/csit.2019.91505

Some of the PRNG techniques are based on Linear Congruential Generator (LCG) [5], Quadratic Congruential Generator (QCG) [6], Linear Feedback Shift Register (LFSR) [7], Cellular Automata (CA) [8], etc. The utilization of the concept of chaos in information security brings enormous advantages because of its inherent properties such as sensitivity to initial condition and large perturbations [9]. Chaos can be exploited either in continuous or in discrete forms. Chaotic maps comprise 1D discrete equation(s) which are driven by suitable initial conditions and seed to generate random numbers.

In various works, logistic map [10], Tent map [11], Henon map [12], Bernoulli map [13] have been the frequently used 1D chaotic systems for random number generation. Despite the yield of good randomness from the chaotic maps, their keyspace is limited which make them vulnerable to brute force attacks. To enhance the keyspace along with randomness, chaotic attractors are suggested. Chaotic attractors are multi – dimensional continuous chaotic systems which consist of more number of control parameters. Lorenz, Lu, Chen and Rössler attractors have been identified as good random number generators due to their versatility while implementing their architecture on FPGA.

Zidan et al. proposed a PRNG based on Lorenz and Chen chaotic attractors which were implemented on Xilinx Virtex 4 FPGA. This implementation has been verified through lyapunov exponent and autocorrelation confidence region. This work required 658 slices of configurable logic blocks and 97 flip-flops to accommodate the design at an operating frequency of 13.17 MHz [14]. Azzaz et al. implemented the Lorenz attractor on Xilinx Virtex II FPGA using Runge – Kutta 4th order approach which utilizes 1926 slices yielding 124 Mbps as throughput for the operating frequency of 15.5 MHz [15]. Further, Schmitz and Zhang designed a continuous chaotic system through Rössler attractor using VHDL on Xilinx ZYNQ 7000 series FPGA. This implementation consumed 433 slices and 96 registers. In addition, this design utilized 12 DSP blocks to achieve 2850 Mbps of throughput [16]. Zhang has suggested yet another implementation of Lorenz attractor on Xilinx Spartan 3E and ZYNQ 7020 FPGAs which required 1029 and 338 slices respectively. It also required 8 DSP blocks with 0.153 mW of power dissipation for the 32-bit implementation of attractor [17]. Rezk et al. enhanced the Lorenz and Lu attractor's implementation using hardwired shifting and multiplexing schemes. This PRNG was designed using VHDL and implemented on Xilinx XC5VLX50T FPGA whose randomness was evaluated through NIST SP 800 – 22 batteries of tests. This design operated at a frequency of 78MHz and consumed 100 slices and 96 flip-flops to generate pseudo random numbers [18].

In general, the transformation of differential equations into time domain representation has been performed through three different approaches namely Euler's method, Mid – point method and Runge – Kutta 4th order approach. The above-mentioned implementations have utilized all the three approaches where Euler's method has significant advantage in terms of area and throughput. With this inference, the proposed work focuses on the implementation of Rössler attractor on Cyclone II FPGA using Verilog HDL with Euler's method. The significant advantages of the proposed work are:

- Lightweight continuous chaotic system
- NIST SP 800 – 22 verified random source
- Moderate throughput with 50 MHz operating clock frequency

2. PRELIMINARIES

In this work, the architecture of chaotic Rössler attractor for designing PRNG on FPGA is proposed. The chaotic attractors are discrete dynamical systems which have attributes namely more sensitivity to initial conditions, deterministic, ergodicity, stochasticity and periodicity. The

randomness of chaotic system has been tested through bifurcation and Lyapunov exponent analysis. The Rössler attractor is known for its simplicity and more chaotic span. It is a system comprising three non-linear ordinary differential equations defined by Otto Rössler [19]. These differential equations define a continuous-time dynamical system that exhibit chaotic dynamics. The set of three dimensional equations of Rössler attractor are given in equations (1 – 3):

$$\frac{dx}{dt} = -y - z \qquad (1)$$

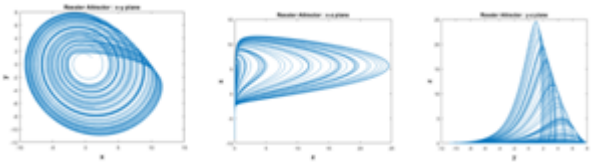
$$\frac{dy}{dt} = x + ay \qquad (2)$$

$$\frac{dz}{dt} = b + z(x - c) \qquad (3)$$

Where a, b and c are the control parameters and x0, y0 and z0 are the initial conditions which trigger the process of generation of time series. Table 1 presents the control parameters chosen and assumed initial conditions of Rössler attractor whereas Fig.1 (a – c) depict the responses of complex behavior in x, y and z directions.

Table 1. Control parameters and initial conditions.

Parameters	Case -1	Case - 2	Case - 3
a	0.2	0.2	0.15
b	0.1	0.2	0.20
c	14	5.7	5.7
x_0	1	1	0.1
y_0	1	1	5.0000000001
z_0	0	0	25



(a) (b) (c)

Figure 1. Complex behavior of Rössler attractor: (a) X - Y plane (b) Y - Z plane and (c) Z - X plane [19].

3. PROPOSED METHODOLOGY

In this proposed work, the Rössler attractor has been designed with the combination of multiplier, adder and subtractor whose architectural representation is shown in Fig. 2. The following steps were carried out to generate random numbers by implementing the attractor design on FPGA.

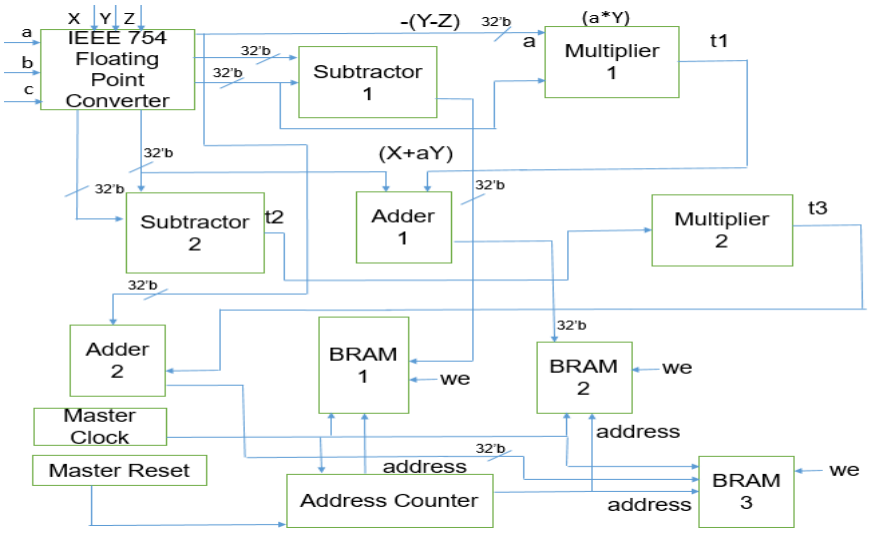


Figure 2. Block diagram of the proposed work.

Step I: Convert the control parameters and initial conditions of Rössler attractor from floating point to binary values using IEEE 754 single precision conversion.

Step II: From the observation of Fig. 2, design requires two subtractors, adders and multipliers. Design the primitive components using Quartus II 13.0 mega functions.

Step III: Develop the Finite State Machine (FSM) using HDL to control and drive the operation of X, Y and Z planes. Also, generate the necessary control signals for memory and end of operation.

Step IV: Create the first state of FSM to perform the required mathematical operations of attractor and make the second state to feedback the results to the attractor variables to \ generate the random numbers continuously.

Step V: Store the random values in Block Random Access Memory (BRAM) of FPGA for further analysis.

Rössler attractor has been designed using Verilog HDL and the functionality was verified through Modelsim 6.0 platform as shown in Fig. 3. Quartus II 13.0 EDA tool was used for implementing the design on FPGA after creating the equivalent Register Transfer Level (RTL) schematic where the architecture has been represented in terms of logic gates and registers as portrayed in Fig. 4. Figure 5 (a – c) show the BRAM screen shots of ten 32 – bit random numbers generated by the FPGA through Rössler attractor with the parameters of case – 3.

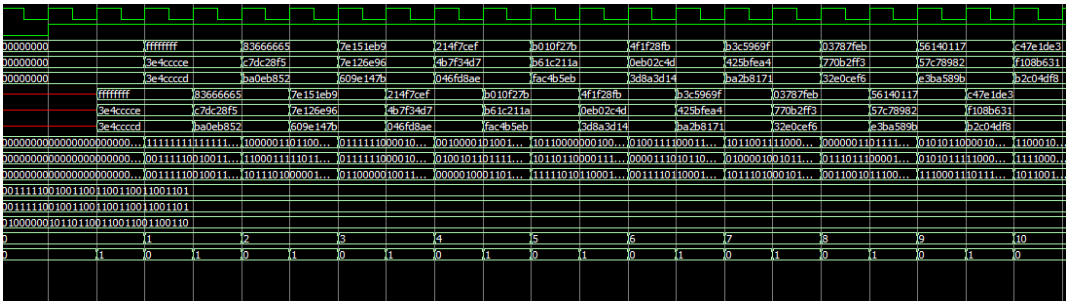


Figure 3. Simulation result of Rössler attractor.

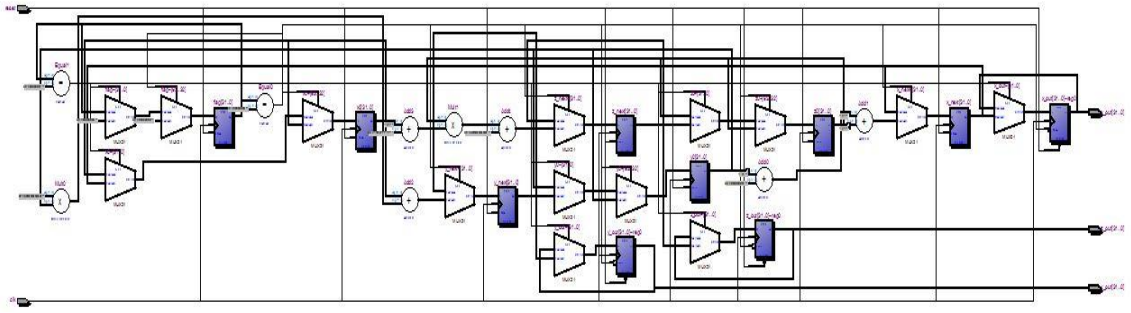


Figure 4. RTL diagram of Rössler attractor.

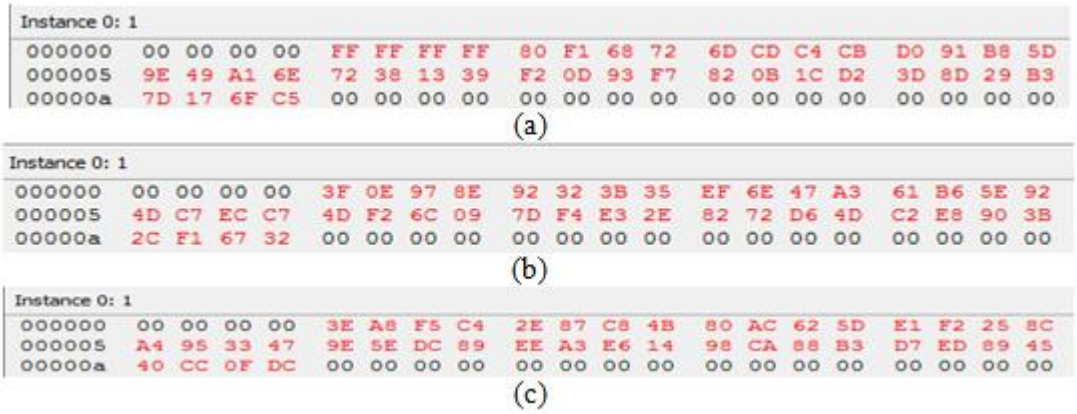


Figure 5. BRAM shots of Rössler attractor for Case-3 (a) X – Plane (b) Y – Plane and (c) Z – Plane.

4. RESULTS AND DISCUSSION

Statistical properties of the proposed PRNG were verified through NIST SP 800 – 22 batteries of test with three different sets of control parameters. In addition, entropy, correlation and bit distribution analyses were carried out to verify the randomness.

4.1. NIST SP 800 – 22 Batteries of Test

It is a statistical package consisting of many tests that have been developed to test the randomness of the binary sequences produced by random number generators [20]. Some tests are divided into many subtests. NIST tests were performed with 1,00,000 of random bits for all the three cases of control parameters with the following constraints.

Block frequency Test – Block length (M) = 128
Non-overlapping Template – Block length (m) = 9
Overlapping Template – Block length (m) = 9
Approximate Entropy Test – Block length (m) = 8
Serial Test – Block length (m) = 10
Linear Complexity Test – Block length (M) = 500

Table 2, 3 and 4 present the results for NIST SP 800 – 22 tests for Case 1, 2 and 3 of control parameters wherein case – 3 yields better results because of its sensitivity and stochasticity.

Table 2. NIST Results of random numbers generated using Case -1 control parameters.

Tests	Case – 1 (a = 0.2, b =0.1, c = 14, x_0 = 1, y_0 =1 & z_0 = 0)					
	X	Statu	Y	Status	Z	Status
Frequency	0.00000	Failed	0.21330	Passed	0.21330	Passed
Block Frequency	0.21330	Passed	0.35048	Passed	0.35048	Passed
Cumulative Sums – I	0.00000	Failed	0.74991	Passed	0.74981	Passed
Cumulative sums – II	0.00000	Failed	0.21330	Passed	0.213330	Passed
Runs	0.00000	Failed	0.12232	Passed	0.12232	Passed
Longest Runs	0.00232	Failed	0.73991	Passed	0.73991	Passed
Rank	0.01430	Passed	0.53414	Passed	0.53414	Passed
FFT	0.35048	Passed	0.78591	Passed	0.73991	Passed
Non Overlapping Template	0.00001	Failed	0.92341	Passed	0.91141	Passed
Overlapping Template	0.00887	Passed	0.03517	Passed	0.00004	Failed
Approximate Entropy	0.35048	Passed	0.73991	Passed	0.73991	Passed
Serial - I	0.00138	Failed	0.00001	Failed	0.73991	Passed
Serial - II	0.21330	Passed	0.00018	Failed	0.35048	Passed
Linear Complexity	0.73991	Passed	0.35048	Passed	0.35048	Passed

Table 3. NIST Results of random numbers generated using Case -2 control parameters

Tests	Case –2 (a = 0.2, b = 0.2, c = 5.7, x_0 = 1, y_0 =1 & z_0 = 0)					
	X	Status	Y	Status	Z	Status
Frequency	0.00000	Failed	0.00000	Failed	0.00000	Failed
Block Frequency	0.02365	Passed	0.21330	Passed	0.91141	Passed
Cumulative Sums – I	0.00000	Failed	0.00000	Failed	0.00000	Failed
Cumulative Sums – II	0.00000	Failed	0.00000	Failed	0.00000	Failed
Runs	0.00000	Failed	0.00000	Failed	0.00887	Passed
Longest Runs	0.06688	Passed	0.00000	Failed	0.00000	Failed
Rank	0.00000	Failed	0.00000	Failed	0.00000	Failed

FFT	0.00000	Failed	0.00000	Failed	0.00887	Passed
Non Overlapping Template	0.00000	Failed	0.00000	Failed	0.91141	Passed
Overlapping Template	0.35048	Passed	0.91141	Passed	0.02431	Passed
Approximate Entropy	0.00000	Failed	0.00000	Failed	0.00000	Failed
Serial - I	0.00000	Failed	0.00000	Failed	0.00000	Failed
Serial - II	0.00001	Failed	0.06688	Passed	0.00887	Passed
Linear Complexity	0.21330	Passed	0.03517	Passed	0.73991	Passed

Table 4. NIST Results of random numbers generated using Case -3 control parameters.

Tests	**Case –3 (a = 0.15, b =0.20, c = 5.7, x_0 = 0.1, y_0 =5.0000000001 & z_0 = 25)**					
	X	**Statu**	**Y**	**Status**	**Z**	**Status**
Frequency	0.19921	Passed	0.73991	Passed	0.73991	Passed
Block Frequency	0.21330	Passed	0.21330	Passed	0.21330	Passed
Cumulative Sums – I	0.44512	Passed	0.53414	Passed	0.73991	Passed
Cumulative Sums – II	0.12526	Passed	0.99146	Passed	0.21330	Passed
Runs	0.03887	Passed	0.53414	Passed	0.00887	Passed
Longest Runs	0.06688	Passed	0.73991	Passed	0.73991	Passed
Rank	0.01430	Passed	0.53414	Passed	0.53414	Passed
FFT	0.12232	Passed	0.02791	Passed	0.35048	Passed
Non Overlapping Template	0.99146	Passed	0.91141	Passed	0.91141	Passed
Overlapping Template	0.21330	Passed	0.99146	Passed	0.91141	Passed
Approximate Entropy	0.12232	Passed	0.06688	Passed	0.73991	Passed
Serial - I	0.35048	Passed	0.73991	Passed	0.73991	Passed
Serial - II	0.73991	Passed	0.53414	Passed	0.06688	Passed
Linear Complexity	0.91141	Passed	0.35048	Passed	0.91141	Passed

From the above results, it was inferred that the Case – 3 passed all the tests in NIST SP 800 – 22 which ensured its strength of randomness.

4.2. Entropy Analysis

Entropy is a fundamental measure of uncertainty which describes the amount of probability of 0's and 1's in a random sequence [21]. It is used to determine the equi - distribution property of random numbers. For a strong set of random numbers, the entropy value must be close to 1. To analyze the equi – distribution property, 32 – bit random numbers from Rössler attractor were divided as 8, 16 and 32 – bits with respect to the LSB and MSB positions. The results of entropy analysis are listed in Table 5. From the Table 5, it is observed that the 32-bit random numbers possess near 1 entropy when compared to 16-bit and 8-bit segments of all the cases.

Table 5. Entropy analysis.

Bits	*Case 1(X)*	*Case 1(Y)*	*Case 1(Z)*	*Case 2(X)*	*Case 2(Y)*	*Case 2(Z)*	*Case 3(X)*	*Case 3(Y)*	*Case 3(Z)*
32	0.999788	0.999636	0.999953	0.999304	0.999304	0.999306	0.999901	0.999998	0.999981
0 – 16	0.993846	0.999925	0.999915	0.999791	0.997365	0.997114	0.999439	0.999924	0.999945
17 –31	0.999845	0.999947	0.999965	0.997915	0.997385	0.997224	0.999479	0.999984	0.999947
9 – 24	0.999876	0.999998	0.999998	0.997925	0.997686	0.997254	0.999785	0.999995	0.999993
0 – 7	0.999876	0.999998	0.999998	0.997925	0.997686	0.997254	0.999785	0.999995	0.999993
8 – 15	0.988025	0.999998	0.99991	0.974932	0.988897	0.988543	0.989123	0.999432	0.999763
16 –23	0.988032	0.999993	0.99997	0.974923	0.988843	0.988345	0.989345	0.999561	0.999761
24 –31	0.988024	0.999994	0.99993	0.974943	0.988854	0.988567	0.989321	0.999287	0.999376

4.3. Correlation Analysis

This metric determines the data dependencies between the random numbers. To become a cryptographically strong PRNG, the correlation must be very low. This analysis was performed for Rössler attractor generated random numbers with Case – 3 control parameters and the results are depicted in Fig. 6 (a – c). The figures convey no existence of correlation among the generated numbers. The data distribution of random sequences generated by Rössler attractor are presented in Fig. 7 (a – c) to ensure the presence of randomness.

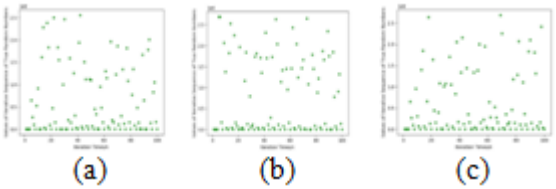


Figure 6. Correlation analysis: (a) X – Plane (b) Y – Plane and (c) Z – Plane.

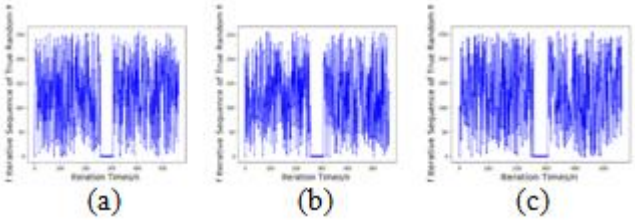


Figure 7. Data distribution analysis: (a) X – Plane (b) Y – plane and(c) Z – Plane.

4.4. Hardware Analysis

As the attractor is implemented on FPGA, it is necessary to evaluate the hardware efficiency in terms of the utility of standard measures such as Look Up Tables (LUTs), combinational logics, dedicated logic registers, on – chip memory bits and power dissipation. The proposed implementation consumes only 2% of total logic elements of Cyclone II FPGA EP2C20F484C7 to construct the Rössler attractor where the total power dissipation is 78.48 mW obtained through Power Play Power Analyzer in Quartus II 13.0 EDA tool for 12.5% toggling rate. Table 6 presents the hardware analyses of the proposed design.

Table 6. Hardware analysis.

Target FPGA	Cyclone II EP2C20F484C7 FPGA
Total Logic Elements	201/18,752 (1%)
Total Combinational Functions	289/18,752 (2%)
Dedicated logic registers	289
Total registers	98/315 (31%)
Total memory bits	131072
Embedded Multiplier 9-bit elements	12/52 (23%)
Total power dissipation (mW)	78.48mW
Time taken for 1024 × 32 bits	4.0 µS

To analyze the performance efficiency, the proposed work has been compared with other earlier works of attractor designs on various FPGAs which are presented in Table 7. From the comparison, this design is superior in terms of logic elements consumption and throughput.

Table 7. Performance comparison.

Criteria	Proposed work	Ref. [14]	Ref. [15]	Ref. [16]	Ref. [17]	Ref. [18]
Attractor	Rössler	Lorenz	Lorenz	Rössler	Lorenz	Lorenz + Lu
Number of Equations	3	3	3	3	3	4
Random Number Size	32 Bits	32 Bits	32 Bits	32 Bits	32 Bits	32 Bits
Target FPGA	Cyclone II	Virtex II	Virtex IV	ZYNQ 7000	ZYNQ 7020	Virtex V
LUTs	201	2718	287	433	868	276
Registers	289	791	96	96	96	96
DSP Blocks	12(Embedded multiplier)	-	8	12	8	8
Frequency(MHz)	50	15.59	53.53	70.9	36.3	78.149
NIST SP 800 - 22	PASS	-	-	-	-	PASS

5. CONCLUSION

The Rössler attractor based 32 – bit PRNG has been implemented on Cyclone II FPGA using Verilog HDL and Quartus II 13.0 EDA tool. This proposed design was realized through Euler's method which is the best way to represent differential equations in time domain. This work consumes 201 LUTs to accommodate the Rössler attractor design which requires only 4.0 µS to generate 32,768 random bits. Statistical characteristics of the proposed design have been verified through NIST SP 800 – 22 tests, entropy and correlation analyses. Future work will be on developing an image security system using the Rössler attractors.

ACKNOWLEDGEMENTS

The authors would like to thank SASTRA Deemed University for providing infrastructure through the Research & Modernization Fund (Ref. No: R&M / 0026 / SEEE – 010 / 2012 – 13) to carry out the research work.

REFERENCES

[1] Y. Hardy and W.-H. Steeb, "Cryptography," in Classical and Quantum Computing: with C++ and Java Simulations, Basel: Birkhäuser Basel, 2001, pp. 215–228.

[2] A. THESEN, "Chapter IX - Random Number Generators," in Computer Methods in Operations Research, A. THESEN, Ed. Academic Press, 1978, pp. 194–213.

[3] S. Z. Li and A. Jain, Eds., "Pseudo-Random Number Generator," in Encyclopedia of Biometrics, Boston, MA: Springer US, 2009, p. 1100.

[4] A. J. Elbirt, W. Yip, B. Chetwynd, and C. Paar, "An FPGA-based performance evaluation of the AES block cipher candidate algorithm finalists," IEEE Trans. Very Large Scale Integr. Syst., vol. 9, no. 4, pp. 545–557, 2001.

[5] S. Tezuka, “Linear Congruential Generators,” in Uniform Random Numbers: Theory and Practice, Boston, MA: Springer US, 1995, pp. 57–82.

[6] S. Strandt, “Quadratic Congruential Generators With Odd Composite Modulus,” in Monte Carlo and Quasi-Monte Carlo Methods 1996, 1998, pp. 415–426.

[7] M. H. Weik, “Linear-Feedback Shift Register,” in Computer Science and Communications Dictionary, Boston, MA: Springer US, 2001, p. 896.

[8] L. Petrica, “FPGA optimized cellular automaton random number generator,” J. Parallel Distrib. Comput., vol. 111, pp. 251–259, 2018.

[9] J. Pejaś and A. Skrobek, “Chaos-Based Information Security,” in Handbook of Information and Communication Security, P. Stavroulakis and M. Stamp, Eds. Berlin, Heidelberg: Springer Berlin Heidelberg, 2010, pp. 91–128.

[10] S. L. Chen, T. Hwang, and W. W. Lin, “Randomness enhancement using digitalized modified logistic map,” IEEE Trans. Circuits Syst. II Express Briefs, vol. 57, no. 12, pp. 996–1000, 2010.

[11] A. Ilyas, A. Luca, and A. Vlad, “A study on binary sequences generated by tent map having cryptographic view,” 2012 9th Int. Conf. Commun. COMM 2012 - Conf. Proc., pp. 23–26, 2012.

[12] M. Suneel, “Cryptographic pseudo-random sequences from the chaotic Hénon map,” Sadhana, vol. 34, no. 5, pp. 689–701, Oct. 2009.

[13] D. J. Driebe, “The Bernoulli Map,” in Fully Chaotic Maps and Broken Time Symmetry, Dordrecht: Springer Netherlands, 1999, pp. 19–43.

[14] M. A. Zidan, A. G. Radwan, and K. N. Salama, “The effect of numerical techniques on differential equation based chaotic generators,” Proc. Int. Conf. Microelectron. ICM, pp. 1–4, 2011.

[15] M. S. Azzaz, C. Tanougast, S. Sadoudi, and A. Dandache, “Real-time FPGA implementation of Lorenz’s chaotic generator for ciphering telecommunications,” in IEEE North-East Workshop on Circuits and Systems and TAISA Conference, NEWCAS-TAISA ’09, 2009, pp. 1–4.

[16] J. Schmitz and Z. Lei, “Rössler-based chaotic communication system implemented on FPGA,” Can. Conf. Electr. Comput. Eng., pp. 1–4, 2017.

[17] L. Zhang, “System generator model-based FPGA design optimization and hardware co-simulation for Lorenz chaotic generator,” 2017 2nd Asia-Pacific Conf. Intell. Robot Syst. ACIRS 2017, no. 2, pp. 170–174, 2017.

[18] A. A. Rezk, A. H. Madian, A. G. Radwan, and A. M. Soliman, “Reconfigurable chaotic pseudo random number generator based on FPGA,” AEU - Int. J. Electron. Commun., vol. 98, pp. 174–180, 2019.

[19] D. T. Maris and D. A. Goussis, “The ‘hidden’ dynamics of the Rössler attractor,” Phys. D Nonlinear Phenom., vol. 295–296, no. M, pp. 66–90, 2015.

[20] L. E. Bassham et al., “A statistical test suite for random and pseudorandom number generators for cryptographic applications,” Natl. Inst. Stand. Technol., Gaithersburg, MD, USA, Tech. Rep., no. April, 2010.

[21] R. Sivaraman, S. Rajagopalan, A. Sridevi, J. B. B. Rayappan, M. P. V. Annamalai, and A. Rengarajan, “Metastability-Induced TRNG Architecture on FPGA,” Iran. J. Sci. Technol. Trans. Electr. Eng., vol. 2, 2019.

AUTHORS

Hemanth Kumar Nalajala is currently pursuing his B. Tech (Electronics and Communication Engineering) in SASTRA Deemed to be University, Thanjavur. His research areas include information security and FPGA implementations of cryptographic algorithms.

Rajesh B is currently pursuing his B. Tech (Electronics and Communication Engineering) in SASTRA Deemed to be University, Thanjavur. His research areas include information security and FPGA implementations of cryptographic algorithms.

Sivaraman R received his B.Tech (Electronics and Communication Engineering) in 2014, from SRC, SASTRA University, Kumbakonam and M.Tech in VLSI Design from SASTRA University, Thanjavur in 2016. He is currently working as research scholar in school of electrical and electronics engineering, SASTRA University, India. His research areas include information security, digital system design of hardware peripherals and embedded system. He has published 16 research articles in the national and international journals.

Sridevi A completed her B. Tech in Electronics & Communication Engg. and M. Tech in Communication& Networking in the years 2009 and 2015 respectively. She has one year of industrial experience and two years of teaching experience. She is currently pursuing her Ph.D. in the domain of Multimedia information security at SASTRA Deemed University, Thanjavur. Her research areas include information security, Multimedia communication, Machine Learning and embedded system. She has published 13 research articles in the national and international journals.

Dr. R. Amirtharajan was born in Thanjavur, Tamil Nadu province India, in 1975. He received B.E. degree in Electronics and Communication Engineering from P.S.G. College of Technology, Bharathiyar University, Coimbatore, India in 1997. M.Tech. and Ph. D. from SASTRA University Thanjavur, India in 2007 and 2012 respectively. He joined SASTRA University, Thanjavur, Tamil Nadu, India (Previously Shanmugha College of Engineering) as a Lecturer in the Department of Electronics and Communication Engineering since 1997 and is now Associate Professor, His research interests include Image Processing, Information Hiding, Computer Communication and Network Security. So far, he filed one international patent; he has published more than 125+ research articles in national and international journals and 28 IEEE conference papers with 4 Best Paper Awards. He also holds the Certificate of Appreciation from IBM in 2009 for Great Mind Challenge, Mentor IBM Academic Initiative Program. Recently, he received the Founder Chancellor Award for the best Ph.D. thesis for 2013 from SASTRA University and he received the SASTRA Anukul Puraskar for Higher Involvement in Research and Education Award for 2011-2012 and 2013-2014. He serves as a Life Member in CRSI, SSI, IAENG, and IACSIT. He also served as the TPC Member and Review Member for more than 30+ IEEE and Springer supported international conferences apart from more than 10 peer reviewed journals. He had been working on funded project in the field of steganography supported by DRDO, Government of India, New Delhi, India.

Sundararaman Rajagopalan completed his B.Tech in Electronics & Instrumentation Engg., M.Tech in Advanced Communication Systems and Ph.D thesis in Steganography System on Reconfigurable Hardware in the years 2005, 2007 and 2016 respectively. He is currently working as Asst. Professor in the Dept. of ECE, SASTRA University. Presently he is carrying out a DRDO, Govt. of India funded project on True Random Key Generation. He carried out a funded project by DRDO on steganography as a Co-Principal Investigator between the years 2010 - 2013. He has published 15 articles on information security. Also he was a WIPRO ULK faculty resource guide team Contributor for FPGA based experiments with Unified Technology Learning Platform (UTLP). He was also a faculty guide for IBM Remote Mentoring Projects for the years 2011 and 2012.

MACHINE LEARNING MODEL TO PREDICT BIRTH WEIGHT OF NEW BORN USING TENSORFLOW

S.Karthiga, K.Indira and C.V.Nisha Angeline

Assistant Professors, Department of Information Technology, Thiagrajar College of Engineering,Madurai

ABSTRACT

Low Birth Weight is the major problem for the new born. Low birth weight is a term used to describe babies who are born weighing less than 5 pounds, 8 ounces (2,500 grams). Low-birth weight babies are more likely than babies with normal weight to have health problems as a newborn. Almost 40 percent of the new born suffer from underweight. Predicting birth weight before the birth of the baby is the best way to help the baby get special care as early as possible. It helps us to arrange for doctors and special facilities before the baby is born. There are several factors that affect the birth weight. Through past studies, it has been observed that the factors which affect the child birth range from biological characteristics like the baby's sex, race, age of mother and father, weight gained by the mother during pregnancy to behavioral characteristics like smoking and drinking habits of the mother, the education and living conditions of the parents. This project focuses on developing a web application that predicts baby weight taking baby's gender, plurality, gestation weeks and mothers age as inputs. Machine learning is one of the domains that plays important role in medical industry. Many machine learning models have been developed to predict diseases at the early stage. In this project wide and deep neural network model is developed using TensorFlow library in Google cloud environment. Wide and Deep Neural Network combines wide linear model and deep neural network. It provides both memorization and generalization. Pre-processing and training is done in the distributed environment using cloud Dataflow and Cloud ML Engine. The model is then deployed as REST API.A web application is developed to invoke the API with the user inputs and show the predicted baby weight to the users. It is scalable and provides high performance.

1. INTRODUCTION

The aim of the project is to predict the baby weight so that the baby can get better care. It is done using machine learning model and in cloud environment. Machine learning plays a major role in medical diagnostics. Machine learning in medicine has recently made headlines. Google hasdeveloped a machine learning algorithm tohelp identifycancerous tumours on mammograms. Algorithms can provide immediate benefit to disciplines with processes that are reproducible or standardized. Machine learning can offer an objective opinion to improve efficiency, reliability, and accuracy. We'll be able to incorporate bigger sets of data that can be analyzed and compared in real time to provide all kinds of information to the provider and patient. This project uses Wide and Deep Neural Network model which provide both generalisation and memorization. Cloud augments machine learning by enabling process in distributed environment providing benefits of

N. Ramasubramanian et al.(Eds) : SRAIC-2019
pp. 71-90, 2019. © CS & IT-CSCP 2019 DOI: 10.5121/csit.2019.91506

scalability,high performance, availability, maintainability, repeatability, abstraction and testability.

Problem Statement

A survey says almost 40 percent of new born suffer from underweight. An underweight baby is more likely susceptible to many health problems than a baby with normal weight. Special care and facilities are to be given to them when they born so that their health condition will be improved. Predicting the weight before the birth of the baby and arranging doctors and facilities if the weight of the baby is less than 5 pounds and 8 ounces helps the baby get better treatment. The solution is to create a machine learning model that predicts the baby weight from major factors like gestation weeks, mother's age, gender and plurality of baby. The model should be deployed as REST API so that it can be invoked using a web application to get predicted birth weight. The process should be carried in cloud environment so that it will be auto scalable and provides high performance.

Objectives

To collect and analyze the natality dataset from big query.

- To launch a preprocessing pipeline using cloud Dataflow to create training and evaluation datasets.
- To create Wide and Deep Neural Network Modelusing TensorFlow and train model in AI Platform.
- To deploy model as REST API.
- To create a web application that invokes API to predict the birth weight.

The scope of the project is to develop a web application that takes mother age, gestation weeks, plurality and gender of the baby as input and give birth weight as output. The application is highly helpful to mother and hospital to make facilities to care of the baby before its birth. If a mother is on the way to the hospital, she calls the nurse. This work is implemented in Deep netural network because of the following reasons: Deep Learning is the next generation of machine learning algorithms that use multiple layers to progressively extract higher level features (or understanding) from raw input. Deep learning algorithms are now used by computer vision systems, speech recognition systems, natural language processing systems, audio recognition systems, bioinformatics systems and medical image analysis systems and the special features of Deep learning is

- No need for feature Engineering
- Best results with unstructured data
- No need for Labeling Data

2. RELATED WORK

2.1. Wide and Deep Learning for Recommendation System

This paper presents Wide & Deep learning jointly trained wide linear models and deep neural networks to combine the benefits of memorization and generalization for recommender systems. It productionized and evaluated the system on Google Play, a commercial mobile app store with over one billion active users and over one million apps. Online experiment results show that Wide & Deep significantly increased app acquisitions compared with wide-only and deep-only models. A recommender system can be viewed as a search ranking system, where the input query is a set of user and contextual information, and the output is a ranked list of items. Given a query, the recommendation task is to find the relevant items in a database and then rank the items based on certain objectives, such as clicks or purchases. During training, input layer takes in training data and vocabularies and generate sparse and dense features together with a label. The wide component consists of the cross-product transformation of user installed apps and impression apps. For the deep part of the model, A 32 dimensional embedding vector is learned for each categorical feature. They concatenate all the embeddings together with the dense features, resulting in a dense vector of approximately 1200 dimensions. The concatenated vector is then fed into 3 ReLU layers, and finally the logistic output unit. The Wide & Deep models are trained on over 500 billion examples. Every time a new set of training data arrives, the model needs to be re-trained. However, retraining from scratch every time is computationally expensive and delays the time from data arrival to serving an updated model. To tackle this challenge, we implemented a warm-starting system which initializes a new model with the embeddings and the linear model weights from the previous model. Before loading the models into the model servers, a dry run of the model is done to make sure that it does not cause problems in serving live traffic. We empirically validate the model quality against the previous model as a sanity check.

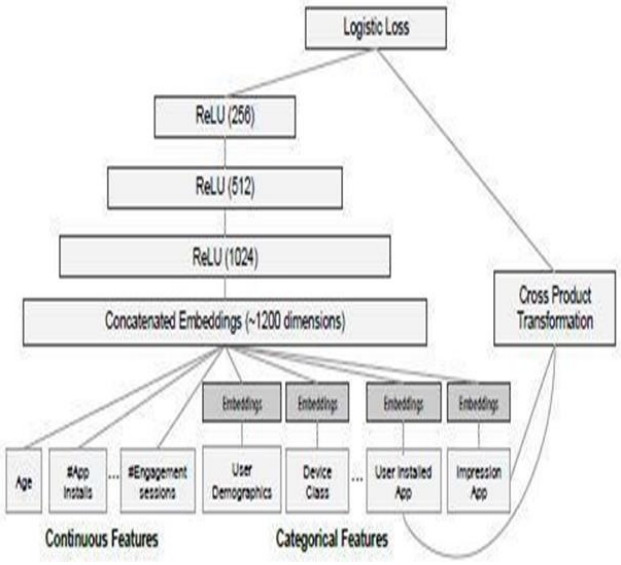


Fig: 1 Wide and Deep model structure for apps recommendation

2.2. Prediction and Classification of Low Birth Weight Data using Machine Techniques

The objective of this research was to apply one of the ML techniques on the low birth weight (LBW) data in Indonesia. This research conducts two ML tasks, including prediction and classification. The binary logistic regression model wasfirstly employed on the train and the test data. Then, the random approach was also applied to the data set. The results showed that the bi-nary logistic regression had a good performance for prediction, but it was a poor approach for classification. On the other hand, random forest approach has a very good performance for both prediction and classification of the LBW data set. Binary logistic regression is a type of logistic regression, which has only two categories of outcomes. It is the simplest type of logistic regression. The main goal of binary logistic regression is to find the formula of the relationship between dependent variable *Y* and predictor *X*. Random forests are defined as the combination of tree predictors such that each tree depends on the values of a random vector sampled independently and with the same distribution for all trees in the forest. In this research, the LBW data were obtained from the result of 2012 IDHS. In the beginning, the raw data consists of 45607 women aged 15-49 years as the respondents. After data cleaning process, the amount data reduced to 12055 women aged 15-49 years who give birth from 2007 up to 2012. The dependent variable is Low Birth Weight with two categories. The independent variables are Place of Residence, Time Zone, Wealth Index, Mother's and Father's Education, Age of the mother, Job of the mother, Number of children.

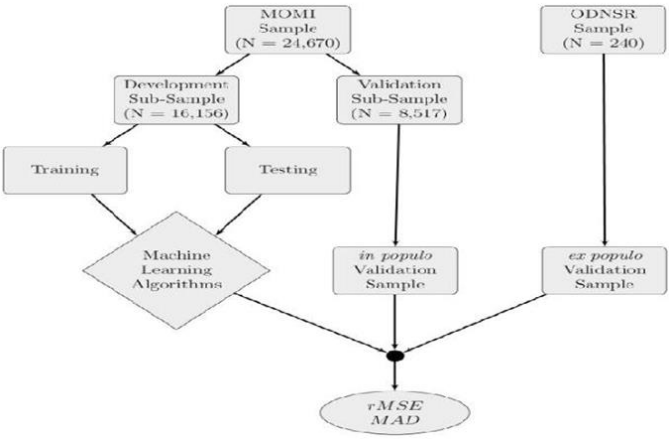


Fig:2 Strategy to predict fetal growth

rMSE is root Mean Squared Error, MAD is median absolute deviation, MOMI is Magee Obstetrics Maternal and Infant Database, ODNSR is Obstetrical Determinants of Neonatal Survival Study Data.

2.3. Prediction of Birth Weight of a Baby

The Dataset used in this research is NC VITAL STATISTICS BIRTHS Dataset.For the year 2008, it had 133422 rows with 125 columns. They trimmed it down by removing the features

which are not relevant. We have also refined the dataset by splitting the categorical variables into several binary variables. After all the cleansing, the final dataset has 69051 rows and 52 columns. The dataset was divided into training and test data in a random manner. The training set comprises of 85% of the data. Whereas, the test dataset comprises of the remaining 15%. It is observed that Boys are found to weigh slightly more than girls at birth, birth weight of a baby born to a smoker mother is less than that born to a non-smoker mother. Whereas, the mortality rate for LBW babies born to a smoker mother is less, babies born to black parents weigh more than those born to white parents. Also, babies born to black father and white mother are a little heavier compared to one born to a white father and black mother, birth weight of a baby born to a drinker mother is less than that born to a non-drinker, the risk of preterm delivery and Low Birth Weight increases in proportion of the severity of anaemia in an anaemic mother. The machine learning models used for training were Multivariate Linear Regression, Multivariate Ridge Regression, K Nearest Neighbours, Decision Trees, Ada-Boost Regressor, and Random Forest Regressor. The machine learning model selected for the final prediction was Random Forest Regressor as the Root Mean Square Error was the least among the models.

3. PROPOSED SYSTEM

The Proposed System is having the following steps to implement Machine learning process.

3.1. Description

In the proposed work, the dataset has to collect from different dataset which includes the major attributes of mother age, gestation weeks, gender and pluralrity of baby from the user. The collected dataset to be analyzed

1.Dataset collection from BigQuery.
2.Analyze the dataset features using Pandas and BigQuery.
-Ensure that dataset have enough examples of each data value, and to verify that the parameter has predictive value.
3.Preprocessing the dataset
-Create training and evaluation dataset.
-Replace missing values with default values.
-Modify plurality field to string.
-Create extra rows to simulate lack of ultrasound

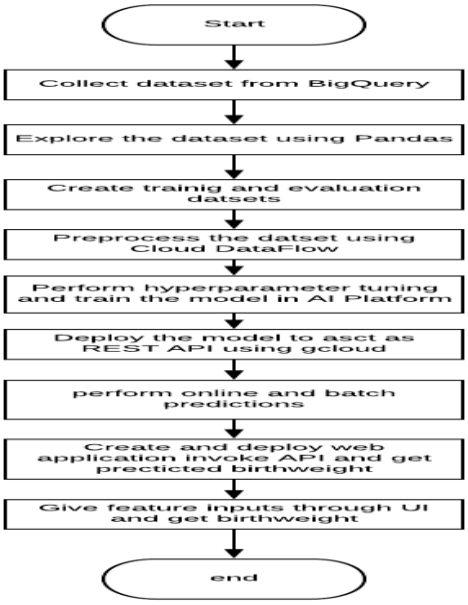


Fig:3 Proposed System

4. Train the model
-Create an input function reading a file using the Dataset API
-Define feature columns
-Create serving input function to be able to serve predictions
-Create metric for hyperparameter tuning
-Create estimator to train and evaluate
-Perform hyperparameter tuning.
-Create python package and submit it to cloud ML engine.

5. Deploy the model as REST API.
-Use model to predict (online and batch prediction)
Develop web application to collect user input and use the API to predict.
-Use model to predict (online and batch prediction)

3.2. Tensorflow

TensorFlow makes it easy to create machine learning models. TensorFlow is an open-source machine learning library for research and production. Estimator is high level API provided by TensorFlow Estimators can train large models on multiple machines in a production environment. TensorFlow provides a collection of pre-made Estimators to implement common ML algorithms. It encapsulates training,evaluation,prediction and export for serving. All Estimators whether pre-made or custom are classes based on the tf.estimator.Estimator class. Pre-made Estimators enable us to work at a much higher conceptual level than the base TensorFlow APIs. Pre-made Estimators create and manage tf.Graph and tf.Session objects. Cloud ML Engine is orthogonal to all APIs in TensorFlow Library. This project uses TensorFlow Version 1.8.0

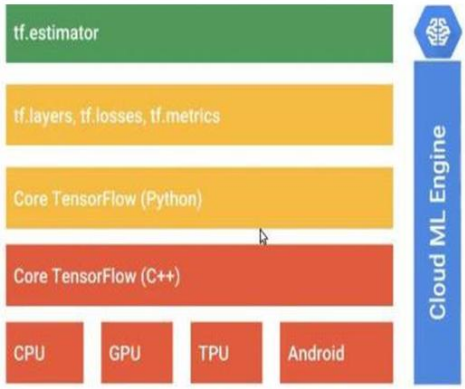


Fig: 4 TensorFlow Architecture

3.2.1. Premade Estimators

Tasks in these estimators include creating input function,defining feature columns,initiating estimator,training,evaluating the model and making predictions from the trained model. The premade estimator we are going to use is DNNLinearCombinedRegressor. It is a regression model since birthweight we are going to predict is a continuous value.Pre-made Estimators are an effective way toquickly create standard models. It also creates checkpoints so that training can be resumed at any time from previous checkpoint.

3.2.2. Checkpoints

Estimators automatically write Checkpoints and event files to disk.Checkpointsare versions of the model created during training. Event filescontain information that TensorBoarduses to create visualizations. The argument named model_dir specifies the directory in which estimators' stores information. If model _dir is not specified in an Estimator's constructor, the Estimator writes checkpoint files to a temporary directory chosen by Python's tempfile.mkdtempfunction. This function picks a secure, temporary directory appropriate for your operating system. By default, it writes a checkpoint every 10 minutes,writes a checkpoint when the train method starts (first iteration) and completes (final iteration) and retains only the 5 most recent checkpoints in the directory. The default schedule can be altered by tf.estimator.RunConfig. Each subsequent call to the Estimator's train, evaluate and predict method builds the model's graphby running the model_fn() and initializes the weights of the new model from the data stored in the most recent checkpoint.

3.2.3. Feature Columns

Feature columns are very rich, enabling you to transform a diverse range of raw data into formats that Estimators can use, allowing easy experimentation. We specify the input to the model through the feature_columns argument. Feature Columns bridge input data with your model. Feature columns are createdusing tf.feature_column module. This module has nine functions. They are Numeric column, Bucketized_column, Categorical identity column, Categorical vocabulary column, Hashed Column, Crossed column,Indicator and embeddingcolumns.The linear_feature_columns argumentacceptsanyfeature column type. The dnn_feature_columns

argument only accepts dense columns. The function categorical_column_with_vocabulary_list maps string to an integer based on an explicit vocabulary list. The function bucketized_column splits column values into different categories based on numerical ranges. The function crossed column combines features into a single feature, better known as feature crosses, enables the model to learn separate weights for each combination of features. The function embedding column never work on features directly, but instead take categorical columns as input. It represents that data as a lower-dimensional, ordinary vector in which each cell can contain any number, not just 0 or 1. By permitting a richer palette of numbers for every cell, an embedding column contains far fewer cells than an indicator column.

3.2.4. Datasets for Estimators

The tf.data module contains a collection of classes thatallows us to easily load data, manipulate it, and pipe it into our model. It enables reading in-memory data from numpy arrays and reading lines from a csv files. The tf.data.TextLineDataset reads the file one line at a time. The Dataset would iterate over the data once, in a fixed order, and only produce a single element at a time. It needs further processing before it can be used for training. Fortunately, the tf.data.Dataset class provides methods to better prepare the data for training. The tf.data.Dataset.shufflemethoduses a fixed- size buffer to shuffle the items as they pass through. In this case the buffer_size is greater than the number of examples in the Dataset, ensuring that the data is completely shuffled. The tf.data.Dataset.repeatmethod restarts the Dataset when it reaches the end. To limit the number of epochs, set the count argument. The tf.data.Dataset.batch method collects a number of examples and stacks them, to create batches. This adds a dimension to their shape. The new dimension is added as the first dimension.Datasets have many methods for manipulating the data while it is being piped to a model. The most heavily-used method is tf.data.Dataset.map, which applies a transformation to each element of the Dataset.The map method takes a map_func argument that describes how each item in the Dataset should be transformed.

3.3. Wide and Deep Neural Network

Generalized linear models with nonlinear feature transformations are widely used for large-scale regression and classification problems with sparse inputs. Memorization of feature interactions through a wide set of cross-product feature transformations are effective and interpretable, while generalization requires more feature engineering effort. With fewer features engineering, deep neural networks can generalize better to unseen feature combinations through low-dimensional dense embeddings learned for the sparse features. However, deep neural networks with embedding can over-generalize and recommend less relevant items when the user-item interactions are sparse and high-rank. Wide & Deep learning jointly trained wide linear models and deep neural networks to combine the benefits of memorization and generalization for recommender systems. Memorization can be loosely defined as learning the frequent co-occurrence of items or features and exploiting the correlation available in the historical data.Generalization, on the other hand, is based on transitivity of correlation and explores new feature combinations thathave never or rarely occurred in the past. Compared with memorization, generalization tends to improve the diversity of the system. Embedding-based models, such as factorization machines or deep neural networks, can generalize to previously unseen query-item feature pairs by learning a low-dimensional dense embedding vector for each query and item feature, with less burden of feature engineering. On the other hand, linear models with cross-product feature transformations can memorize these exception rules" with much fewer

parameters. The wide component and deep component are combined using a weighted sum of their output log odds as the pre diction, which is then fed to one common logistic loss function for joint training. Note that there is a distinction between joint training and ensemble. In an ensemble, individual models are trained separately without knowing each other, and their predictions are combined only at inference time but not at training time. In contrast, joint training optimizes all parameters simultaneously by taking both the wide and deep part as well as the weights of their sum into account at training time.

3.4. Dataset

This Project uses publicdata.samples.natality dataset available in BigQuery.The datasetdescribes all United States births registered in the 50 States, the District of Columbia, and New York City from 1969 .It has 137,826,763 rows.The table size is of 21.94 GB.The data location of table is US. It has 31 attributes. But we are interested in 7 main attributes .They are weight in pounds, gestation weeks, plurality, baby's gender, month and year.

Table:1 Schema of Natality table

Field Name	**Type**	**Description**
source_year	INTEGER	Four-digit year of the birth.
year	**INTEGER**	**Four-digit year of the birth.**
month	**INTEGER**	**Month index of the date of birth**
day	INTEGER	Day of birth, starting from 1.
wday	INTEGER	Day of the week from 1 to 7
state	STRING	The two character postal code for the state.
is_male	**BOOLEAN**	**TRUE if the child is male, FALSE if female.**
child_race	INTEGER	The race of the child.
weight_pounds	**FLOAT**	**Weight of the child, in pounds.**
plurality	**INTEGER**	**How many children were born as a result of this pregnancy.**
apgar_1min	INTEGER	Apgar scores measure the health of a new born child on a scale from 0-10.
apgar_5min	INTEGER	Apgar scores measure the health of a newborn child on a scale from 0-10. V
mother_residence_state	STRING	The two-letter postal code of the mother's state of residence when the child was born
mother_race	INTEGER	Race of the mother. Same values as child race.
mother_age	**INTEGER**	**Reported age of the mother when giving birth.**

gestation_weeks	**INTEGER**	**The number of weeks of the pregnancy.**
lmp	STRING	Date of the last menstrual period in the format MMDDYYYY.
mother_married	BOOLEAN	True if the mother was married when she gave birth.
mother_birth_state	STRING	The two-letter postal code of the mother's birth state.
cigarette_use	BOOLEAN	True if the mother smoked cigarettes. Available starting 2003.
cigarettes_per_day	INTEGER	Number of cigarettes smoked by the mother per day
alcohol_use	BOOLEAN	True if the mother used alcohol. Available starting 1989.
drinks_per_week	INTEGER	Number of drinks per week consumed by the mother
weight_gain_pounds	INTEGER	Number of pounds gained by the mother during pregnancy.

Note: Features of interest are highlighted.

The data collected after 2000 is used in this project. Month and year fields are concatenated and the hash is calculated to split the dataset into training and evaluation datasets. FARM_FINGERPRINT is used to find the hash value. The function computes the fingerprint of the STRING or BYTES input using the Fingerprint64 function from the open-source FarmHash library. The output of this function for a particular input will never change. The return type of this function is INT64.

3.5. Process Description

3.5.1.Exploring the Dataset

To train the model, we must explore the dataset, understand its structure, and examine relationships within the data. We then isolate and construct relevant features within the data. A feature is a piece of information that impacts the predictions our model will make. Features can be fields of data in our source dataset, or they can be formed using one or more of the original fields. Identifying the relevant features for our model is called featureengineering. It is done to ensure that dataset have enough examples of each data value, and to verify that the parameter has predictive value. It is also checked whether you have enough for each input value. Otherwise, the model prediction against input values that don’t have enough data may not be reliable.BigQuery python package is imported. Pandas is used to explore the dataset. Dataset is retrieved from BigQuery and stored in pandas Data frame. Then the data is visualised using plot function provided by Pandas. Data collected above 2000 is used for training.The number of records and the average weight for each value of the separate features is found.

From the exploration, it is interpreted the following:

-Male babies are heavier on average than female babies
-Teenaged and older moms tend to have lower-weight babies
-Twins, triplets, etc. are lower weight than single births.

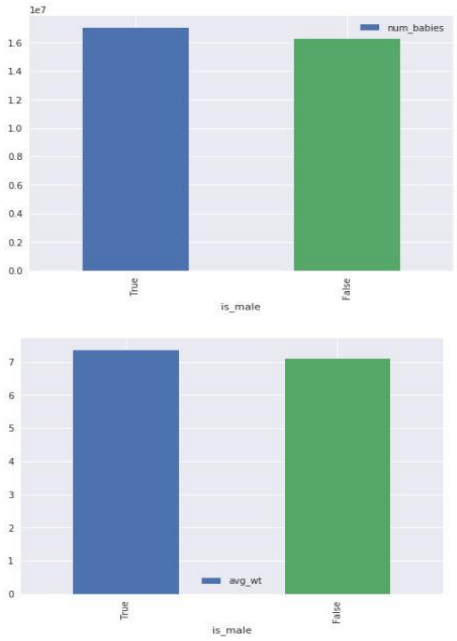


Fig: 5 Exploring is_male feature

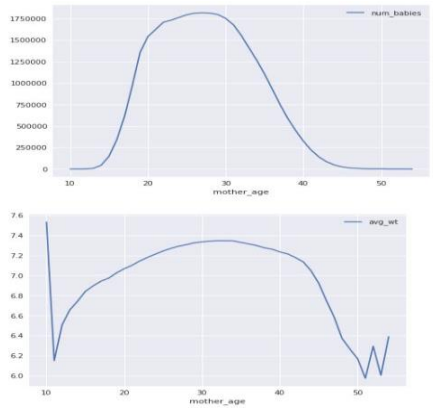


Fig:6 Exploring mother_age feature

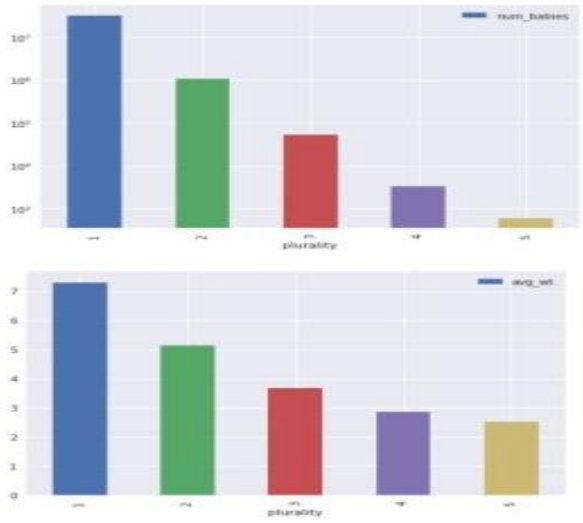


Fig:7 Exploring plurality feature

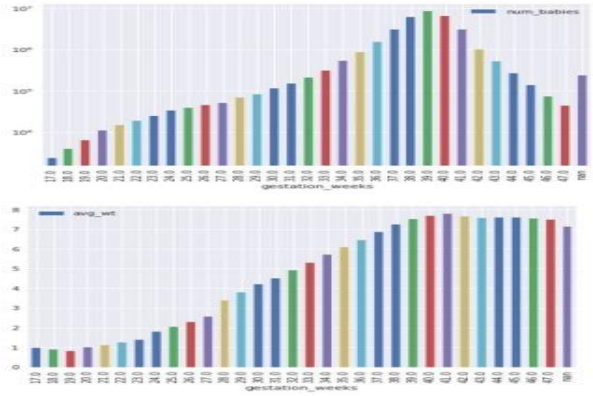


Fig:8 Exploring gestation weeks feature

3.5.2. Preprocessing the Dataset

Pre-processing is done to transform data into a format suitable for training. In this step, dataset is split into training and evaluation datasets. They are created using hash function and modulo function. The hash of the year-month is used so that twins born on the same day won't end up in different cuts of the data. The hash is calculated using FARM_FINGERPRINT function. The quarter of data is used for evaluation and remaining are used for training. Hence the remainder of dividing the hash by is used to define the two datasets. If the remainder is less than 3, that record belongs to training set and if it is equal to 3, that record belongs to evaluation set. This technique ensures that we get a random sampling of the source data in each dataset and reduces the risk of accidentally skewing the evaluation set. . It is important to guarantee that the evaluation set represents the general characteristics of the data so that you can evaluate the generalization performance of the trained model with it.The columns are pulled out of BigQuery and stored in a CSV file within a Cloud Storage bucket. Cloud Dataflow is used to generate synthetic data to make the model more robust to partial or unknown input values.

In the dataset, every row in the dataset contains the baby's gender, because this is known after the baby is born. However, we are building a model to predict the weight before the baby is born. We know the sex of the baby only if an ultrasound was performed during the pregnancy. If no ultrasound was performed, the doctor enters the baby's gender as "Unknown".So we generate artificial data by writing each historical data point twice, once with the original value for the is_male column and again after replacing the is_male column value by Unknown.

Also, it is difficult to count the number of babies without an ultrasound, so while doctors can tell whether there is one baby or multiple babies, they can't differentiate between twins and triplets.We replace the plurality numbers with string values when writing out the data to simulate the absence of an ultrasound.All these code are written with Apache Beam SDK.Apache Beam SDK is programming model for both batch and streaming use cases that implements data processing jobs that run on any execution engine and executes pipelines on multiple execution environments. The job is submitted to cloud dataflow using DataflowRunner which takes about 30 minutes to finish. Job details are showed in Cloud Dataflow page in Google cloud console.

Fig: 9 Cloud Dataflow data processing pipeline

3.5.3. Training the Model

The model is trained in cloud environment using AI Platform. The model code is created as python package and submitted to AI Platform using gcloud tool.The numerical features are mother_age and gestation_weeks.The categorical features are is_male and gestation_weeks.One hot encoding is applied to categorical columns.Wide model woks well on categorical features.Hence numeric features are Bucketized and passed to wide model.On the other hand deep model works well on numeric features. Wide features are crossed, embedded and passed as additional input to deep model. An input_fn is created to return batch of examples for training for each invocation. It identifies files that match the filename pattern and shuffles them before retrieving examples. After reading a batch of rows from a CSV file, tf.decode_csv converts column values into a list of TensorFlow constant objects. The DEFAULTS list is used to identify the value types and complement empty cells. The input_fnfunction returns the dictionary of features and the corresponding label values.Metrics for hyperparameter tuning is added with the parameter to be optimized as root mean squared error. Then serving input function is created to serve predictions using user inputs. Estimator object is initiated with

DNNLinearCombinedRegressor as model specifying model directory,features and hidden units. Training and evaluation specifications are specified. Training and evaluation of the model is done by calling tf.estimator.train_and_evaluate function. All these details are specified in model.py file. The python package contains 3 files-__init__.py to inform that it is a python package, model.py and trainer.py for handling command line arguments which reads value for parameters and sets them to the appropriate argument in model.py file. The arguments are bucket name,output directory,batch size,train examples,evaluation steps,file pattern,nembeds and neural network size.The training job is submitted to AI Platform using gcloud specifying package path, command line arguments etc.Once training is started,it can be visualized using tensor board tool.

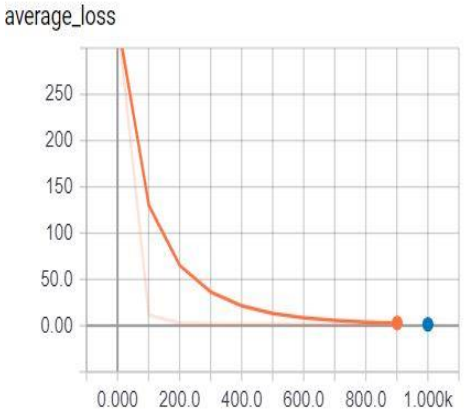


Fig:10 average loss during training

3.5.4. Deploying Model

The trained model is stored in exporter directory. This directory is given as option for gcloud command. The gcloud command is used for creating model and then version.The models are listed in AI Platform under the models tab. After that online and batch predictions are performed. For online prediction, json object is created with the features and sent with the request to the API.For batch predictions,an input file is created and outputpredictions are stored in cloud storage. Authentication is required for accessing the API.For that purpose access token is passed with the headers. Access token is generated using Google Credentials module.

3.5.5. Creating a Web Application

GoogleAppEngine is used to deploy a web application. The file deploy.sh contains code for creating and deploying the app. The app is deployed in asia-south1 region. The main.py is a Python script that runs on App Engine. It provides an API service that returns a prediction for a baby's weight. To get this predicted value, it uses the prediction API service deployed on the Managed ML Service.It sends a request to the prediction API service hosted on Cloud ML Engine converting plurality and gender field to string.It also checks whether all the fields are set.It uses Google Credentials for authorization.The templates/form.html is an HTML file containing JavaScript code that renders the input form shown below. It sends a REST API request to the backend application that runs on App Engine and then displays the result. The application is autoscalable and provides high performance.It supports several queries in a second.

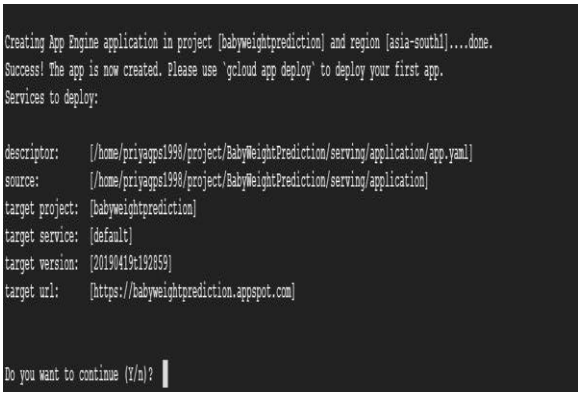


Fig:11 App Details

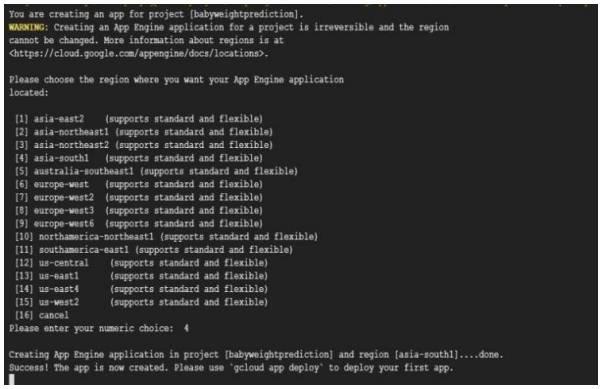


Fig:12 Regions available for deploying application

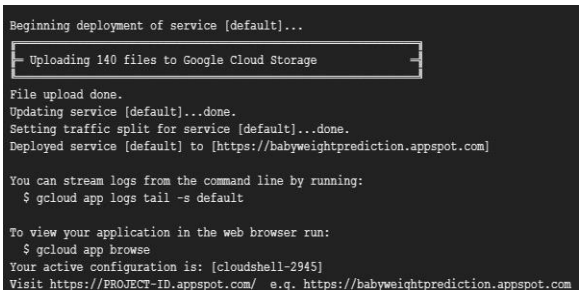


Fig:13 Deployment of application

3.6. Tools, Libraries and Apis Used

Bigquery

BigQuery is Google's serverless, highly scalable, enterprise data warehouse designed to make all our data analysts productive at an unmatched price-performance. There is no infrastructure to manage, we can focus on analysing data to find meaningful insights using familiar SQL without the need for a database administrator.We can analyse all our data by creating a logical data

warehouse over managed, columnar storage, as well as data from object storage and spreadsheets. It enables us to build and operationalize machine learning solutions with simple SQL. We can easily and securely share insights as datasets, queries, spreadsheets, and reports. BigQuery allows organizations to capture and analyze data in real time using its powerful streaming ingestion capability so that your insights are always current, and it's free for up to 1 TB of data analyzed each month and 10 GB of data stored. It enables us to save query, validate query, save view, schedule query, export table and get summary of query. It shows job history and explore in data studio.

BigQuery supports a standard SQL dialect which is ANSI: 2011 compliant, reducing the need for code rewrite and allowing us to take advantage of advanced SQL features. BigQuery provides free ODBC and JDBC drivers to ensure our current applications can interact with Big Query's powerful engine.BigQuery provides rich monitoring, logging, and alerting throughStackdriver Audit Logs. BigQuery resources can be monitored at a glance, and BigQuery can serve as a repository for logs from any application or service using Stackdriver Logging.

Public Dataset

A public dataset is any dataset that is stored in BigQuery and made available to the general public through the Google Cloud Public Dataset Program. The public datasets are datasets that BigQuery hosts for you to access and integrate into our applications. Google pays for the storage of these datasets and provides public access to the data via a project. Public datasets are available for you to analyze using either legacy SQL or standard SQL queries. You can access BigQuery public data sets by using the BigQuery web UI in the GCP Console, the classic BigQuery web UI, the command-line tool, or by making calls to the BigQuery REST API using a variety of client libraries such as Java, .NET, or Python.

In addition to the public datasets, BigQuery provides a limited number of sample tables that you can query. These tables are contained in the bigquery-public-data :samples dataset. It includes the following tables gsod,github_nested,githubtimeline,natality,Shakespeare,trigrams,Wikipedia.This project uses natality dataset for training the model.

Cloud Datalab

Cloud Datalab is a powerful interactive tool created to explore, analyze, transform and visualize data and build machine learning models on Google Cloud Platform. It runs on Google Compute Engine and connects to multiple cloud services easily so we can focus on our data science tasks. Cloud Datalab is built on Jupyter (formerly IPython), which boasts a thriving ecosystem of modules and a robust knowledge base. Cloud Datalab enables analysis of our data on Google BigQuery, Cloud Machine Learning Engine, Google Compute Engine, and Google Cloud Storage using Python, SQL, and JavaScript (for BigQuery user-defined functions). Whether we are analyzing megabytes or terabytes, Cloud Datalab has you covered. Query terabytes of data in BigQuery, run local analysis on sampled data and run training jobs on terabytes of data in Cloud Machine Learning Engine seamlessly.This project uses Cloud Datalab in asia-south1-a region to create notebooks and execute code.

Pandas

Pandas is an open source, BSD-licensed library providing high-performance, easy-to-use data structures and data analysis tools for the Python programming language. This project uses pandas to explore dataset.It supports three datastructures- Dataframe,series, and panel. A Data frame is a two-dimensional data structure.It supports columns of different types and can perform arithmetic operations on rows and columns.It helps data visualisation using matplotlib libraries plot() method .

Google Cloud Storage

Google Cloud Storage is a RESTful online file storage web service for storing and accessing data on Google Cloud Platform infrastructure. The service combines the performance and scalability of Google's cloud with advanced security and sharing capabilities. It is an Infrastructure as a Service, comparable to Amazon S3 online storage service. Contrary to Google Drive and according to different service specifications, Google Cloud Storage appears to be more suitable for enterprises. Google Storage (GS) stores objects that are organized into buckets identified within each bucket by a unique, user-assigned key. All requests are authorized using an access control list associated with each bucket and object. Bucket names and keys are chosen so that objects are addressable using HTTP URLs. Google Storage offers four storage classes, identical in throughput, latency and durability. The four classes, Multi-Regional Storage, Regional Storage, Near line Storage, and Cold line Storage, differ in their pricing, minimum storage durations, and availability. This project stores pre-processed dataset, trained model, hyperparameter tuning details, application in a Multi-regional bucket.

Compute Engine Api

It creates and runs virtual machines on Google Cloud Platform. Compute Engine’s tooling and workflow support enable scaling from single instances to global, load-balanced cloud computing. Compute Engine's VMs boot quickly, come with persistent disk storage, and deliver consistent performance. Our virtual servers are available in many configurations including predefined sizes or the option to create Custom Machine Types optimized for your specific needs. Flexible pricing and automatic sustained use discounts make Compute Engine the leader in price/performance. It is a billable component. It must be enabled to use Datalab. It enables us to resize our clusters, create machine images, virtualize our network, use Pre-emptible for batch workloads and create Custom Machine Types to optimize for our specific needs.

Cloud Dataflow

Cloud Dataflow is a fully-managed service for transforming and enriching data in stream (real time) and batch (historical) modes with equal reliability and expressiveness -- no more complex workarounds or compromises needed. And with its serverless approach to resource provisioning and management, you have access to virtually limitless capacity to solve your biggest data processing challenges, while paying only for what you use. Cloud Dataflow supports fast, simplified pipeline development via expressive SQL, Java, and Python APIs in the Apache Beam SDK, which provides a rich set of windowing and session analysis primitives as well as an ecosystem of source and sink connectors. Plus, Beam’s unique, unified development model lets you reuse more code across streaming and batch pipelines. GCP’s serverless approach removes

operational overhead with performance, scaling, availability, security and compliance handled automatically so users can focus on programming instead of managing server clusters. Integration with Stackdriver, GCP's unified logging and monitoring solution, lets you monitor and troubleshoot your pipelines as they are running. Rich visualization, logging, and advanced alerting help you identify and respond to potential issues. This project uses Dataflow runner to pre-process dataset in cloud Dataflow which stores the processed dataset in bucket.

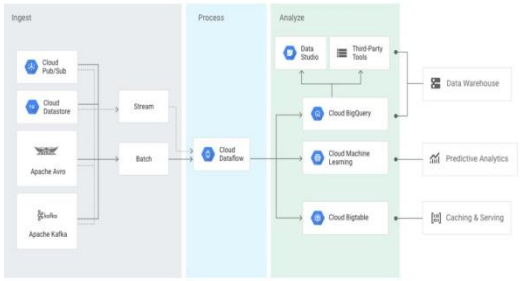


Fig: 14 Data transformation with cloud Dataflow

Cloud Ml Engine

Cloud Machine Learning Engine is a managed service that lets developers and data scientists build and run superior machine learning models in production. Cloud ML Engine offers training and prediction services, which can be used together or individually. We can scale up model training by using the Cloud ML Engine training service in a serverless environment within GCP. Cloud ML Engine supports popular ML frameworks or lets you run our application within a Docker image. It also provides built-in tools to help us understand our models and effectively explain them to business users. Cloud ML Engine automatically sets up an environment for XGBoost and TensorFlow to run on multiple machines, so you can get the speed you need by adding multiple GPUs to our training job or splitting it across multiple VMs. It helps us achieve better results faster by automatically tuning deep learning hyperparameters with HyperTune. HyperTune saves many hours of tedious and error-prone work.Once we have a trained model, Cloud ML Engine offers two types of predictions to apply what the computer learned to new examples.

Online Prediction deploys ML models with serverless, fully managed hosting that responds in real time with high availability. Our global prediction platform automatically scales to adjust to any throughput. It provides a secure web endpoint to integrate ML into your applications. Batch Prediction offers cost-effective inference with unparalleled throughput for asynchronous applications. It scales to perform inference on TBs of production data.

Cloud ML Engine has deep integration with our managed notebook service and our data services for machine learning: Cloud Dataflow for feature processing, BigQuery for dashboard support and analysis, and Cloud Storage for data storage. It is used for training and deploying model.

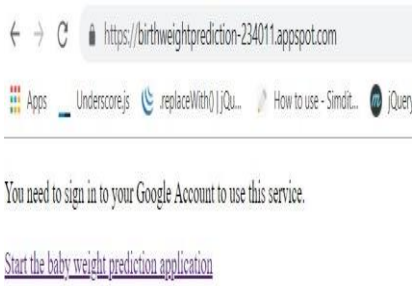


Fig:15 Index page

The users are redirected to the authorization server where the user provide their Google account credentials and authorized.

Fig: 14 Main Page

User needs to set all the fields otherwise it asks the user to set all items.

Fig: 15 Baby weight predictor

4. CONCLUSION AND FUTURE WORK

This application predicts the birthweight within a minute. It helps in making prior arrangement of doctors and facilities before baby birth. It is available all time since it is deployed in the cloud. This application is helpful mainly for hospitals, pregnant ladies. It is highly scalable and provides high performance and maintainability. This application currently depends on the four major factors mother's age, gestation weeks, plurality and gender of baby. In future, features will extended including several other factors like smoking mother, mother's race, country, etc. so that the algorithm will be improved to get the best results. Also, this web application will be extended as mobile application to improve portability and flexibility. It will be improved in such a way that it provides suggestions to prevent low birthweight and helps mother take special care during pregnancy.

REFERENCES

[1] Alfensi Faruk, Endro Setyo Cahyono, Ning Eliyati,IkaArifieni,(2018),"Prediction and Classification of LowBirth Weight DataUsing Machine LearningTechniques" Indonesian Journal of Science &Technology 3(1)18-28.

[2] Heng-Tze Cheng, Levent Koc, Jeremiah Harmsen, Tal Shaked, Tushar Chandra, Hrishi Aradhye, Glen Anderson, Greg Corrado, Wei Chai, Mustafa Ispir, Rohan Anil, Zakaria Haque, Lichan Hong, Vihan Jain, Xiaobing Liu, Hemal Shah,"Wide & Deep Learning for Recommender Systems" - arXiv: 1606.07792v1 [cs.LG]

[3] Stefan Kuhle, Bryan Maguire, Hongqun Zhang, David Hamilton, Alexander C. Allen, K.S.Joseph, Victoria M. Allen,,"Comparision of logistic regression with machine learning methods for the prediction of fetal growth abnormalities:a retrospective study ", BMC Pregnancy and Childbirth, 18(1):333. doi: 10.1186/s12884-018-1971-2.

[4] Dahlui, M., Azahar, N., Oche, O. C., and Aziz, N. A. "Risk factors for low birth weight in nigeria: evidence from the 2013 Nigeria demographic and health survey. Global Health Action",2016, 9, 28822.

[5] Firdaus, C., Wahyudin, W., & Nugroho, E. P. (2017)."Monitoring System with Two Central Facilities Protocol." Indonesian Journal of Science and Technology, 2(1), 8-25.

[6] https://codelabs.developers.google.com

[7] https://cloud.google.com/solutions/machinelearning/data-preprocessing-for-ml-with-tf-transform-pt2

[8] https://www3.cs.stonybrook.edu/~skiena/591/final_projects/baby_weight/

[9] https://cloud.google.com/mlengine/docs/tensorflow/hyperparameter-tuning-overview