

CLASS D POWER AMPLIFIER FOR MEDICAL APPLICATION

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ABSTRACT

The objective of this research was to design a 2.4 GHz class AB Power Amplifier (PA), with 0.18um Semiconductor Manufacturing International Corporation (SMIC) CMOS technology by using Cadence software, for health care applications. The ultimate goal for such application is to minimize the trade-offs between performance and cost, and between performance and low power consumption design. This paper introduces the design of a 2.4GHz class D power amplifier which consists of two stage amplifiers. This power amplifier can transmit 15dBm output power to a 50Ω load. The power added efficiency was 50% and the total power consumption was 90.4 mW. The performance of the power amplifier meets the specification requirements of the desired.

KEYWORDS

Two stage, Class D, Power amplifier, Healthcare

1. INTRODUCTION

Wireless medical sensor networks have offered significant improvements to the healthcare industry in the 21st century, technology changes our life at everywhere[1][2][3][4]. Devices are arranged on a patient's body and can be used to closely monitor the physiological condition of patients [5][6][7][8][9][10][11][12][13]. These medical sensors monitor the patient's vital body parameters, such as temperature, heart rate, blood pressure, oxygen saturation, and transmit the data to a doctor in real time [2]. When a doctor reviews the transmitted sensor readings, they can get a better understanding of a patient's health conditions. The benefit for the patients is that they do not need to frequently visit the hospital, thus patients could reap time and money savings. Such wireless medical sensors will continue to play a central role in the future of modern healthcare. People living in rural areas would especially benefit, since 9% of physicians work in rural areas while almost 20% of the US population lives there [2]. A shortage of physicians and specialist is a big issue in such areas, even today. But Wireless Medical Sensor Network technology has the potential to alleviate the problem. In a wireless sensor network, as seen in the figure 1 below, each device is capable of monitoring, sensing, and/or displaying information. A sensor node is capable of gathering sensory information, processing it in some manner, and communicating with other nodes in the network[2].

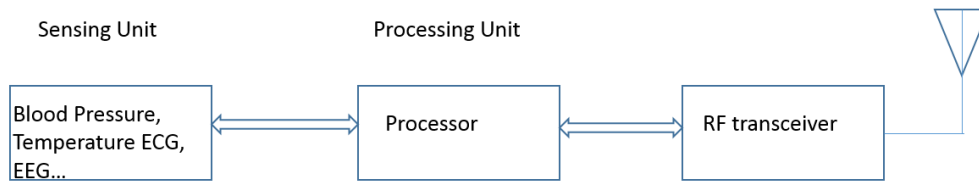


Figure 1. Block diagram of a typical sensor node

Figure 1 shows that the basic sensing node can collect the physiological signals (e.g.: such as EEG, ECG, body temperature, blood pressure, heart beat etc.), when attached to a human body [14]. The processing unit processes all the sensed signals, then sends out the data based on communication protocols. All the processed data will be transmitted through a wireless link to a portable, personal base-station. Doctors can then obtain all the patients' data through the network.

The main challenge for such sensor node is the high power consumption of portable devices. A solution to this challenge is the integration of the portable devices' digital and RF circuitry into one chip.

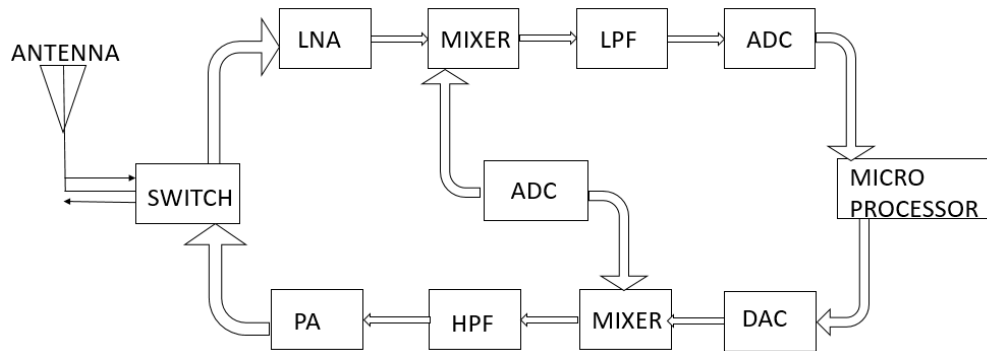


Figure 2. Block diagram of a transmitter

The receiver will receive the signal and will also perform DSP processing after the data is sent out by the transmitter [2]. Figure 2 is the transmitter diagram. It is desirable that the transmitter and receiver are low power devices. The direct-conversion transmitter is very popular for such applications, because it offers versatility, flexibility, spectral efficiency, and low complexity. These features make the transmitter simpler than the super-heterodyne transmitter. Small chip and circuit size, and low power consumption can be achieved with a direct-conversion transmitter architecture. For the front-end transmitter, the major objectives are 1) transmit RF signals and 2) recover the biosignal classification. This paper proposes a low power receiver design. This paper is mainly for the power amplifier design, since other portions of the circuit design are already discussed in the paper [14]. In order to meet the standards, the PA is designed as shown in table 1.

Table 1: PA design requirement.

| Parameter | Target(Unit) |
|--------------|--------------|
| Output Power | 10dBm |
| PAE | 40% |
| Stability | >1 |
| S11 | -10 dB |

2. METHODS

Over the past 30 years, research on CMOS radio-frequency (RF) front-end circuits has progressed extremely quickly. The ultimate goal for the wireless industry is to minimize the trade-offs between performance and cost, and between performance and low power consumption design [15].

The proposed Class D amplifier has low output power and good linearity based on the IEEE 802.11b communication protocol. The Class-D amplifier, whose basic form is seen in figure 3, consists primarily of two switches. During device operation, the switches will alternately turn on and off due to the driver stage, and the output voltage of the switch varies between ground and the supply voltage. Also within the device is a bandpass filter composed of a series LC resonator tuned to the desired frequency, providing nonzero conductance essentially only in the band of interest. Such filters allows the maximization of the current in the frequency band of interest, while minimizing the current flowing at the unwanted band. Hence, no power dissipation happens outside of the desired operational band[16].

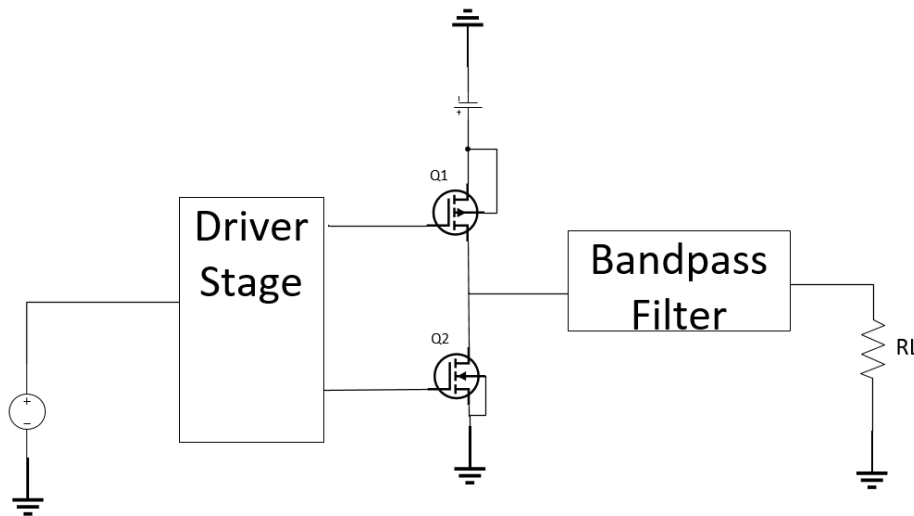


Figure 3. Block diagram of a class D power amplifier

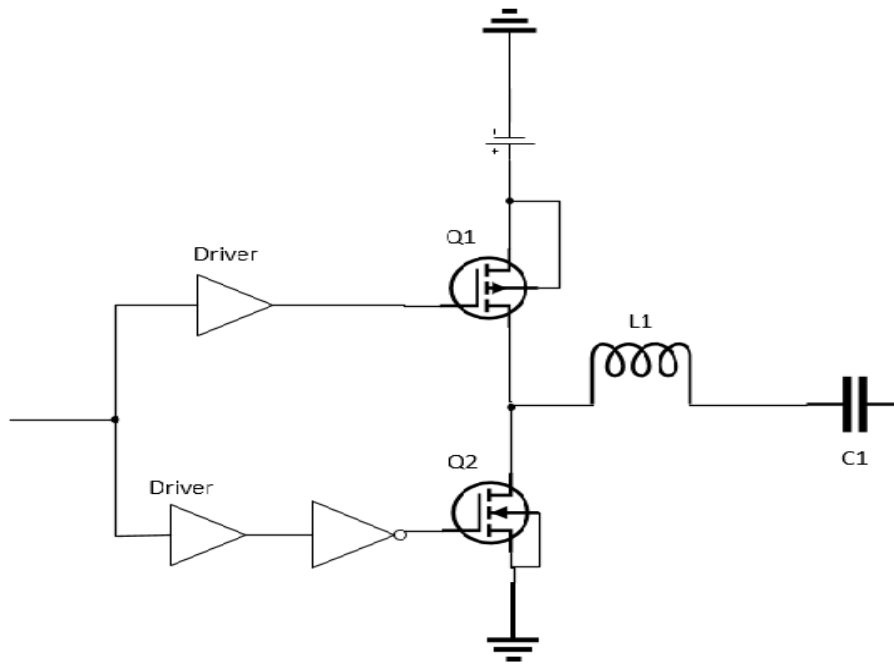


Figure 4. Schematic of PA design

To get the optimum bias, small-signal simulation and 1dB compression point simulation are completed by their power output capability. Resulting design values can be shown in Table 2.

Table 2: 2.4GHz PA driver stage component.

| Parameter | Size (Unit) |
|-----------|--------------------------|
| Q1 | W/L=1um/0.5um (f=8,m=18) |
| Q2 | W/L=1um/0.6um (f=2,m=12) |
| L1 | 2nH (Q=20) |
| C1 | 600fH |

3. RESULTS

As seen in figure 5(a), the output power was 16. As seen in figure 5(b), the frequency is at 2.4 GHz the S11 is less than -10 dB, also, the total power of the PA is 90.4 mW.

As seen in figure 6(a), Kf is larger than 1 for all frequencies from 1 to 3 GHz, so this circuit was totally stable. And the PAE could reach 50%.

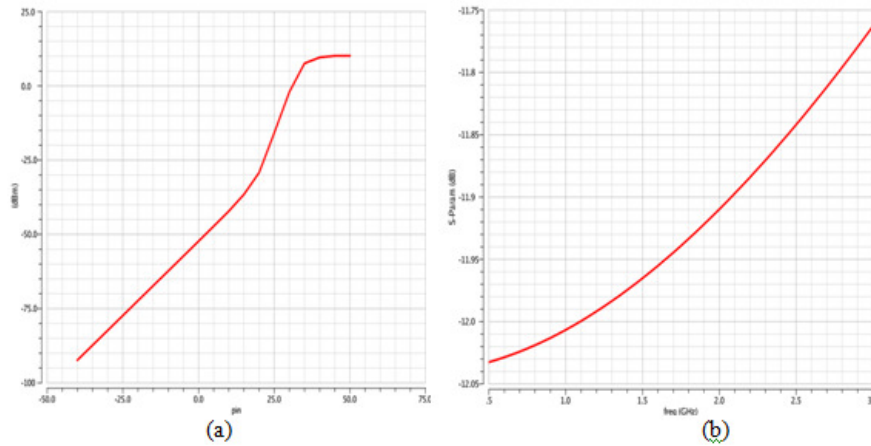


Figure 5. (a) Output power (b) S11

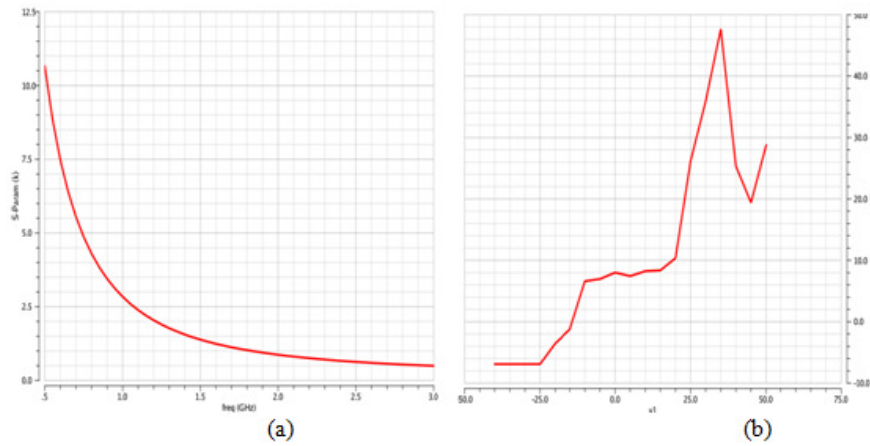


Figure 6. (a) Kf (b) PAE

4. CONCLUSION

This paper describes the method of designing and simulating power amplifier using cadence software based on SIMC CMOS process 180nm technology. This PA is used for sensor networks. This research is still in the early stages of development of a low cost and low power device. In order to reach the performance that is needed, the PA process uses group III and IV elements. This circuit meets the scheduled requirements for the CMOS process, but it still has room to improve performance metrics. When the sensor is coupled with communications technologies such as mobile phones and the Internet, the sensor network constant information flow between individuals and their doctors. Such low cost and low power device can save a lot of hospitalization resources. To realize this, future improvement is needed.

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