LOW POWER SI CLASS E POWER AMPLIFIER AND RF SWITCH FOR HEALTH CARE

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ABSTRACT

This research was to design a 2.4 GHz class E Power Amplifier (PA) for health care, with 0.18um Semiconductor Manufacturing International Corporation CMOS technology by using Cadence software. And also RF switch was designed at cadence software with power Jazz 180nm SOI process. The ultimate goal for such application is to reach high performance and low cost, and between high performance and low power consumption design. This paper introduces the design of a 2.4GHz class E power amplifier and RF switch design. PA consists of cascade stage with negative capacitance. This power amplifier can transmit 16dBm output power to a 50Ω load. The performance of the power amplifier and switch meet the specification requirements of the desired.

KEYWORDS

Cascode, Negative Capacitance, Class E, Power amplifier, Healthcare, RF switch

1. INTRODUCTION

Wireless Sensor Networks (WSN) can be widely applied to solve a vast array of problems, under varied conditions[1]. Such WSNs can provide near-real time, non-stop data over a large sampling area or population, by large distributing many devices to monitor the surrounding environment [2][3][4][5][6][7][8][9]. WSNs could deliver considerable efficiencies to otherwise with costly tasks [10][11][12]. For example, patient monitoring carries considerable cost, especially if used to a large section of the patient. Desirable solutions can be recognized leveraging WSNs and the present cellular communication. Academic and industry research is currently ongoing investigating such frameworks [13][14][15][16][17][18].

Due to current hardware components restrictions, healthcare application of WSNs are still in the early stages[19][20][21][22]. Such devices require Food and Drug Administration (FDA) approval, which can be challenging and costly due to the requirement that the devices pass a number of safety tests. Not so many companies and research institutions can successfully building such a heath care device under full FDA approval [23].

WSNs consist of a number of networked elements, which are individually called sensor nodes. Sensor nodes usually contain all kinds of hardware elements, such as batteries, sensors, antennas, memory, ADC, FPGA, etc [24][25][26][30]. A major design challenge for medical
applications is that - designs a cost effective device which would meet functional requirements [2][27][28][29]. In order to implement such networks with a massive amount of nodes, each node must be low cost. Typically, each device must provide long working cycles without battery recharging. This pushes most sensor node designs to be super ultra-low power. Achieving this low power performance at low cost are critical to making such sensor networks feasible[31][32].

The main design challenge for such WSN is the high power consumption of portable devices. One possible answer to this task is the integration of the digital, analog and RF circuitry into one chip. Thus, switch and power amplifiers have different and unique characteristics, which requires different processes to tape out each one. But switches and PAs can be integrated on a single SIP. A system in package (SiP) is a module that contains multiple integrated circuits. A SiP has the same function as an electronics system. They are often used in the smart phones and PCs. Dies could be connected via bondwires between packages. Alternatively, solder bumps may be utilized in a stacked architecture in the package.

Figure 2. Block diagram of a transmitter

The receiver will receive the signal and will also perform DSP processing after the data is sent out by the transmitter [32]. Figure 2 is the basic transmitter block. It is always desirable that the transmitter and receiver are low power consumption. In order to meet the standards, the PA and RF switch are designed as shown in table 1.

Table 1: PA design requirement.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Target(Unit)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Power</td>
<td>15 dBm</td>
</tr>
<tr>
<td>Power gain</td>
<td>50 dB</td>
</tr>
<tr>
<td>Stability</td>
<td>&gt;1</td>
</tr>
<tr>
<td>S11</td>
<td>-10 dB</td>
</tr>
<tr>
<td>Insertion</td>
<td>0-1.2 dB</td>
</tr>
<tr>
<td>Isolation</td>
<td>&gt;40 dB</td>
</tr>
<tr>
<td>IIP3</td>
<td>55 dB</td>
</tr>
</tbody>
</table>

2. METHODS

CMOS radio-frequency (RF) front-end circuits has developed extremely fast over the past 30 years. Getting the trade-offs between high performance and low cost, and between high performance and low power consumption design, people always try to achieve these target[34].
The cascode circuit with negative capacitance is shown in the figure 2. The advantage of this structure is that it provides less parasitic capacitance, since it allows the parasitic capacitance to be tuned at the driver stage. A shunt inductor instead of capacitor can also be inserted at the driver stage to filter out the unwanted parasitic capacitance, at the cost of wafer area [33].

As seen in figure 2, a negative capacitance can be implemented by a capacitor with a common gate amplifier. For class E power amplifiers, transistor M1 acts as a switch. Transistor M2 delivers high gain, when biased at saturation [35].

![Figure 2. Block diagram of a class E power amplifier](image)

To get the optimum bias, cadence simulation such as PSS are completed. Detailed design values can be seen in Table 2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Size (Unit)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q1</td>
<td>W/L=0.3um/0.6um (f=66, m=24)</td>
</tr>
<tr>
<td>Q2</td>
<td>W/L=0.3um/0.6um (f=66, m=24)</td>
</tr>
<tr>
<td>Q3</td>
<td>W/L=0.8um/0.6um (f=4, m=2)</td>
</tr>
<tr>
<td>L1</td>
<td>36nH (Q=20)</td>
</tr>
<tr>
<td>L2</td>
<td>20nH (Q=20)</td>
</tr>
<tr>
<td>L3</td>
<td>20nH (Q=20)</td>
</tr>
<tr>
<td>C1</td>
<td>240fH</td>
</tr>
<tr>
<td>C2</td>
<td>600fH</td>
</tr>
<tr>
<td>C3</td>
<td>11pF</td>
</tr>
<tr>
<td>R1</td>
<td>10.5ohm</td>
</tr>
<tr>
<td>R2</td>
<td>3.8Kohm</td>
</tr>
</tbody>
</table>

FET switches usually have three different topologies, such as series, shunt and combinatorial topology. Due to modern, complicated requirements, users for in health care usually require the
combinatorial topology to meet their stringent requirements, as seen in the Figure 3. When a control voltage is set high, the series FET would be on, which means a signal would pass to the following transistor, where a shunt FET would connect to the ground. When the control is set low, the series FET is off, so there will be no signal flow through the transistor, however the shunt FET will pass the signal.

In terms of RF switch performance, there are several key parameters, such as reflection coefficient \( S_{11} \), insertion loss \( S_{21} \) and isolation \( S_{31} \). \( S_{11} \) is the input reflection coefficient, which is voltage ratio of the reflected wave on the input port to the original wave. This parameter represents the power loss from impedance mismatches, also known as voltage standing wave ratio (VSWR). \( S_{21} \) represents the forward voltage gain. A low insertion loss between source and active switch is critical to increase the efficiency. \( S_{31} \) is also a very important switch parameter. When there is 3 ports, two ports are on, and another port is off, and this parameter is a measure of the transmission coefficient from the source to the off arm. This parameter represents how much power was leaked into the off arm. Besides the \( S_{11}, S_{21}, S_{31} \), a switch design’s value must also consider the intercept point (IP3). This parameter is a measure of the linearity of a device, which also known as intermediation distortion. The third order intercept point is where the intercept of the fundamental frequency and the third order of the fundamental frequency. There are many other parameters that can be considered, but the S-parameters and the IP3 are the critical ones that must often be considered. A good RF switch usually possesses: low insertion loss, high isolation, high power handling, and very high ESD immunity. A shunt FET would connect to the ground. When the control is set low, the series FET is off, so there will be no signal flow through the transistor, however the shunt FET will pass the signal.

FETs are three terminal devices are usually fabricated as SOI or GaAs. The basic function is shown in Fig. 3. When the gate is more positively biased then the source, a channel would be formed between the source and drain side, so the resistance is lowered, and a current can be flowed between source and drain terminals. However, if the gate voltage is equal or smaller than the source terminal, no channel will form, resistance will be much higher, and no current flows through channel.

![Figure 3. Modified series-shunt FET switch](image)
3. RESULTS

As seen in figure 4(a), the output power was 17 dBm. As seen in figure 4(b), the S11 is less than -10 dB at 2.4 GHz frequency, also, the total power consumption is 2.061 W.

As seen in figure 5(a), Kf is larger than 1 for all the simulated frequencies, so this design is completely stable. And the power gain could reach 94 dB.

As seen in figure 6(a), at 5 GHz, an insertion loss is 1.36 dB and an isolation is 58.5 dB.
4. CONCLUSION

This paper describes the method of designing and simulating power amplifier in SMIC CMOS 180 nm process and RF switch at SOI process 180nm technology. This PA and switch are used for sensor networks which can be integrated at SIP. Such kind research is still under developing, to realize this a low cost and low power device, future improvements are needed.

REFERENCES


Authors

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