FPGABASEDACQUISITIONANDTRANSMISSIONOFDATA INSONAR

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ABSTRACT

System development in FPG As allows considerable flexibility,during development and in production use. However, this flexibility comesat the cost of increased complexity. I have designed a modular development framework to help to overcome these issues of increased complexity. The development of the framework hasbeen divided into two phases. The first phase Is to interface preamplifier and ADC using SPI communication protocols while the second phase is to design the Ethernet interface. In this studies I developed the system in Virtex5 FPGA on ML505 evaluation platform, here IDEtool XilinxISE13.3i and Wireshark is used for control and communication.

Keywords

SONAR, Field Programmable Gate Array, Analog to digital convertor, Ethernet

1. INTRODUCTION

Underwater acoustics a key underpinning technology in off shoreoil and gas activities, is increasingly use dinoceanographic and environmental studies and continue stop lay a crucial role in defence. [1]Sound Navigation And Ranging (SONAR) uses sound propagation (usually under water, as in submarine navigation) to navigate, communicate or detect objects on or under the surface of the water, such as other vessels.

The challenge of SONAR signal processing is to detect/classify targets in anoisy environment. In signal processing literature, SONAR signal can be classified to wide range of applications according to the SONAR mode. The class of marine vessels is defined according to the application of surveillance system for example surface and sub.[2]For decades, the trained people classified and recognized the class of marine vessels by listening to the irradiated noise. Substituting these people with intelligent systems for classifying marine vessels based on their acoustic radiated noise is one of the hot topics in signal processing and artificial intelligence. Although intelligent methods outperformed classic methods in the signal processing using the same data[2] they need large amount of real data for learning, thus a considerable number of research papers are based on simulations of SONAR signals and environments. In addition, new

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Trends on mixing of classic and modern methods have been introduced. Infact, mixed methods strengthen advantages of each approach and reduce the irdis advantages. FPGA-based acquisition and transmission control systems are especially interesting because they allow parts of the system to be easily migrated between hard ware and software implementations[3]for optimal performance and resource use[4].

This project introduces a highly reliable system for realizing programmable gain amplifier(PGA)[3] based on digital potentiometers as opposed to multiple DAC.The choice of multiple DAC oradigipot involves a trade-off between resolution and speed. Although DACh as a higherre solution, digipot is better suited for multiple a coustic channel Sonar where speed is the most contributing factor.

2. SYSTEM DESIGN AND SPECIFICATION

An automatic gain circuit is provided which modifies the beam of signals based upon a history of the signal level present in previous returns. Design make suse of digitally controlled potentiometers (Digipot) programme dusing an automatic gain control algorithm to condition the transducer in put in the Programmable Gain Amplifier (PGA)as shown in the block diagram given in Fig.1

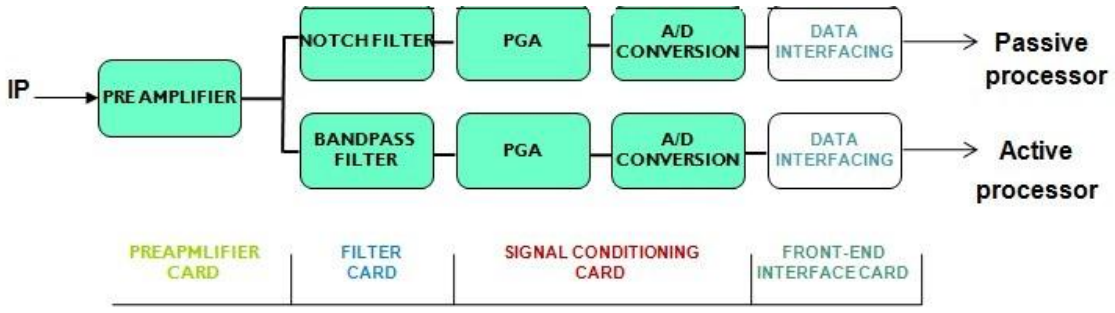

Fig.1. BlockDiagram

The basic functions of the Signal Conditioning Card are: Line Receiving the pre amplified signal from the signal conditioning PCB, High pass filter, Whitening, PGA, Anti- aliasing Filter and Analog to Digital Conversion of acoustic channels. The PCB is designed to cater for16 acoustic channels as shown in the input output diagram of signal conditioningcardinFig.2.

Specifications of the Signal Conditioning Card are Number of analog input channels: 16 Maximum, Maximum Signal Input:125mVpeak at preamplifier input2.5Vpeakat Line Receiver input, Programmable Gain : -10dB to +80dB in steps of 1dB , Signal Bandwidth:100Hzto12KHz, Sampling Frequency: 31.25K sample sperse cond, ADC Resolution:12bits.

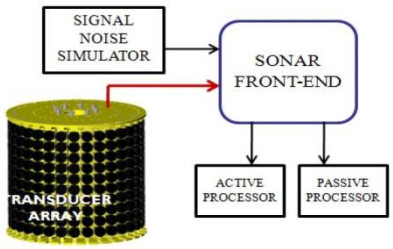

Fig.2. SignalConditioningCard

The platform is chosen to be FPGA over the conventional embedded environment. FPGAs are hard wired and the random attack of alpha ray scan not destroy/corrupt the memory are as hence collapse the device functionality. Life time of the FPGA based development is longer when they areopted in critical conditions. Micro controllers change too often. Hencelots of re-workre quired to do in order to keep pace with changing technology.

FPGAs can be easily adopted for advanced chip when situation demands. This is necessary to save the design from being obsolete. Hence the reconfigurable platform of FPGAs is preferred in real time military applications.

2.1 CIRCUITDESCRIPTION

A programmable-gain amplifier (PGA)is an amplifier (typically an op-amp) whose gain can be controlled by external digital or analog signals. The Programmable Gain Amplifier section of the PCB is realized using two independent gain stages both of them, programmable .The Programm able Gain Amplifier is realized as per the configuration shown in Fig.3.

Each of the Programmable gain stage is realized using digipot.The digipot is connected in the feed back path of the op-amp in order to vary the gain.U(x)8(AD5262) is a dual digital potentiometer with two independent 8bit register for storing the gain parameter.

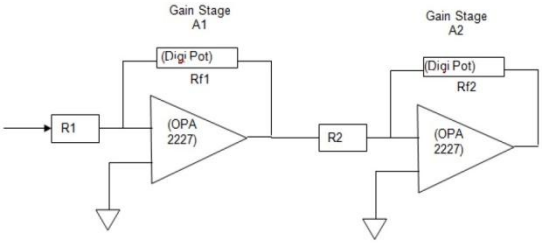

Fig.3. Programmable Gain Amplifier Configuration

The digital data interface for digipot is provided through the SPI interfacing. All the 16 devices required for 16 programmable gain amplifiers are cascaded so that only three serial lines are required for loading the gain parameter for all the Programmable gain amplifiers. The scheme for cascading the digital potentiometers is shown in Fig.4

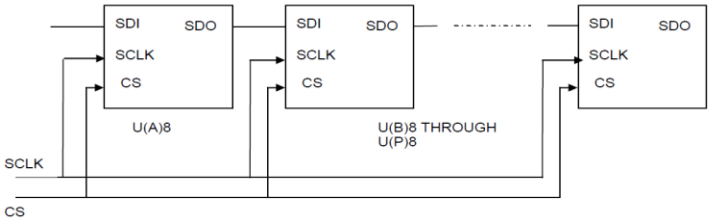

Fig.4 The scheme for cascading the digital potentiometers

3. A FRAMEWORK FOR PROTOTYPING

3.1 Interfacing of Digipot (AD5262)

The programmable gain amplifier section of the PCB is realised using two independent gain stages both of them are programmable. Each of the programmable gain stage is realised using digitally controlled potentiometers (digipot). The digital data interface for digipot is provided through the SPI interfacing. TheAD5262providesadual-channel,256-positiondigitally controlledvariableresistor(VR)deviceandoperateupto15Vmaximumvoltage[4]. Each VR has its own VR latch, which holds its programmed resistance value. These VR latches are updated from an internal serial-to-parallel shift register, which is loaded from a standard 3-wire serial-input digital interface. The AD5262 contains a 9-bit serial register. Each bit is clocked into the register on the positive edge of the CLK. The AD5262 address bit determines the corresponding VR latch to be loaded with the last 8 bits of the data word during the positive edging of CS strobe. Changing the programmed VR settings is accomplished by clocking a9-bit serial data word in to the SDI(SerialDataInput)p in.For this ADC, the format of this data word is one address bit.A represents the first bit of serial data B_8,then followed by eight data bits B_7-B_0 with MSB first. VR outputs can be changed one at a time in random sequence. TheAD5262 presets to amid-scale,simplifying fault condition recovery at power-up[3]. Mid-scale can also be achieved at anyt ime by asserting the PRp in.Both parts have an internal power ON preset[3] that places the wiper in mid-scale preset condition at power ON.Operation of the power ON preset function depends only on the state of the VLpin.TheAD5262 contains a power shutdown SHDNp in,which places the RDAC in an almost zero power consumption state,where terminals Axare opencircuited. And the wiper W is connected toB,result in g in only leakage currents being consume d in the VRstructure. In shutdown mode ,the V R l atch setting sare maintained so that,returning to operational mode from power shutdown. And the VR settings return to the irprevious resistance values. The functional block diagram of AD5262 is shown in the Fig.5.

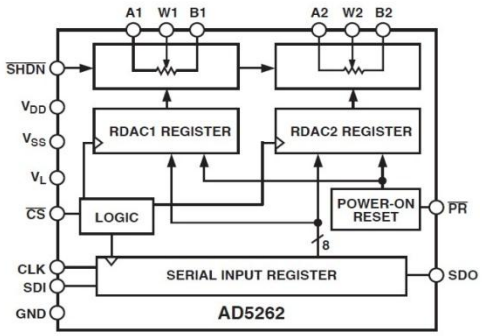

Fig.5. AD5262BlockDiagram

The AD5262 containsa4-wire SPI-compatible digital interface(SDI,SDO,CS,andCLK).For the AD5262,the 9-bit serial word loaded with address bit A0 first,then MSB of the data. The positive-edgesensitiveCLKinputrequirescleantransitionstoavoidclockingofincorrectdataintothe serial input register.When CS is low,the clock loads data in to the serial register one ach positive clock edge.For the AD5262 the last 9 bits of the serial data word entered into the serial data register are held when CS returns to high. Any extrabits are ignored. At the same time CS goe shigh,it gates the address decoder by enabling AD5262 one of two positive edge-triggered AD5262 RDA Clatches.The target RDA Clatch should be loaded with the last 8 bits of the serial data word completing one RDAC update.For theAD5262,two separate 9-bit serial data word smust be clocked into change both VR settings. During shutdown (SHDN)the SDO output pin is forced to the off to disable power dissipation in the pull-upresistor. Fig.6 shows the timing diagram of AD5262.

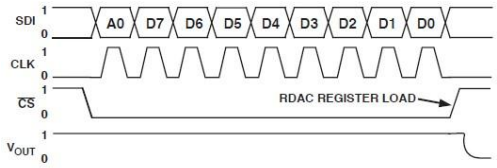

Fig.6. AD5262TimingDiagram

3.2 Interfacing of ADC (ADS1278)

This paper opted ADS1278for ADC interfacing.Based on the single-channel ADS1271,ADS1278(octal)is24-bit, delta-sigma analog-to-digital converter(ADCs)with data rates upto128ksamples per second(SPS),allowing simultaneous sampling of eight channels. The device is offered in identical packages,permitting drop-inexpandability. Industrial delta-sigma ADCs offers good drift performance use digital filters with large pass band droop. Hence they have limited bandwidth and are mostly suited for dc measurements.In audio applications high-resolution ADC sofferslargerus able band widths,but the offset and drift specifications are significantly weaker than respective industrial counter parts. This ADC combines these types of

converters, allowing high-precision industrial measurement with excellent dc and ac specifications.

Data ready for retrieval are indicated by the falling DRDY output and are shifted out on the falling edge of SCLK, MSB first. The device shifts in data on the falling edge and the user normally shifts this data in on the rising edge. On the application of the control signals, serial data bits will be available at the output pin of ADC along with DRDY signal. Timing diagram of ADS1278 is shown in Fig.7.

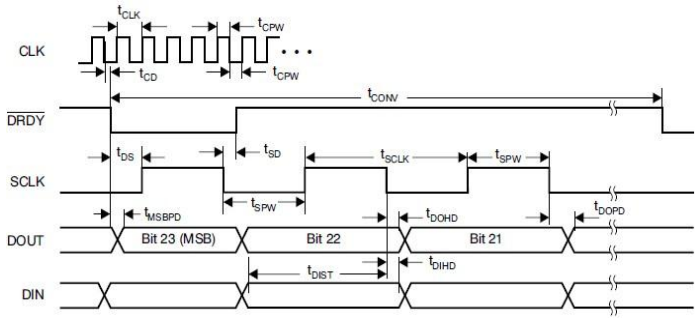

Fig.7. Timingdiagram of ADS1278

3.3 Design of Ethernet Interface

Ethernet interfacing is implemented VHDL making use of Virtex-5FPGA.Embedded Tri-Mode Ethernet MAC wrapper automates the generation of the HDL wrapper files for the Embedded Tri-ModeEthernet MAC(Ethernet MAC)inVirtex-5LXT,FXT,SXT and TXTFPGA susing the software Xilinx COREGenerator[5].Although, Verilog and VHDL instantiation templates are available in Libraries Guide for the FPGA Ethernet MAC primitive; how ever,due to the complexity and large number of ports CORE Generator software is preferred. It simplifies integration of the Ethernet MACby providing HDL examples based on user-selectable configurations.

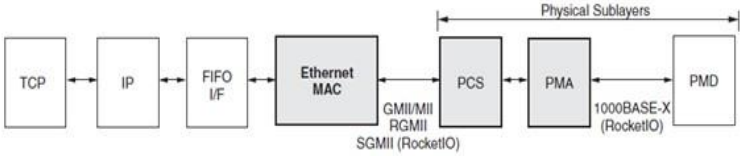

Fig.8. Typical Ethernet Architecture

Fig.8 displays Ethernet MAC architecture from the MAC to the right,as defined in the IEEE802.3specification, and it also illustrates where the supported physical interfaces fit into this architecture.TheSerial-GMII(SGMII) interface is an alternative to GMII/MII.It converts

the parallel interface of the GMII/MII in to a serial format using aRocket IOGTP or GTXtransceiver. It radically reduces the I/Ocount.For this reason,it is often the preferred interface of PCBdesigners. SGMIIcancarryEthernet traffic at10Mbps,100Mbps,and 1Gbps[6].The combination of the Physical Coding Sublayer (PCS),the Physical Medium Attachment (PMA),and the Physical Medium Dependent(PMD) sublayer comprise the physicallayersof the Ethernet protocol.

The Ethernet MAC wrapper file instantiates the full Ethernet MAC primitive. All unused input ports are tied to the appropriate logic level and all unused outputports are left unconnected. The Ethernet MAC attributes are set based on the options selected in the CORE Generator. Only usedports are connected to the ports of the wrapper file.This simplified wrapper is used as the instantiation template for the Ethernet MAC in the design.The designis downloaded on to the FPGA. All the clock management logic required to operate the Ethernet MAC and the designis provided. BUFGs, DCMs and so forth are instantiated as required.The design includes an Addresss wapping module and a FIFO[7]. Frames received by the Ethernet MAC are passed through the Receiveside of the FIFO. Data from the Receiveside of the FIFO is passed into the Address Swap Module and then onto the Transmitside of the FIFO using a Local Link interface.The Transmit FIFO queues frames for transmission and connects directly to the clientside Transmit interface of the Ethernet MAC.

The Address Swap Module switches the Destination Address and Source Address . The10Mbps,100Mbps,1Gbps Ethernet FIFO is a wrapper file around the Receive and Transmit FIFO components. The Receive(Rx) Client FIFO and theTransmit(Tx) Client FIFO,both4k-byte FIFO simplemented in block RAMS, is connected directlyt to the Rx Client Interface and the TxClient Interface of the Ethernet MAC respectively. The transmit and receive FIFO component simple menta Local Link user interface, through which the frame data is read and written. The FIFO is designed to work with the client clocks running at speeds in the range of 125MHz to 1.25MHz.

The data transferred from source to destination on the Local Link interface, with the flow governed by the four active low control signals of -n, src-rdy-n, e of-n, and dst-rdy-n. The flow of data is controlled by the src-rdy-nanddst-rdy-n signals. When these signals are asserted simultaneously,data is transferred from source to destination.The individual packet boundaries are marked by thes of-nande of-nsignals.

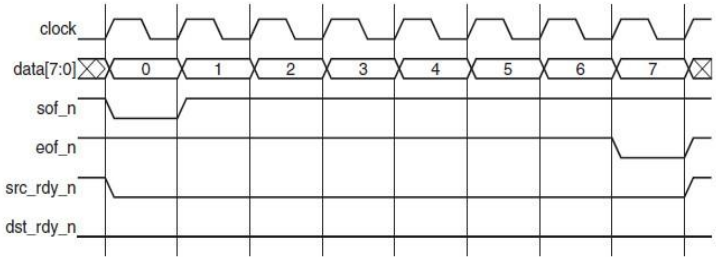

Fig.9 FrameTransferacrossLocalLinkInterface

The selected GMII/MII interface connects the physical interface of the Ethernet MAC block to the I/O of the FPGA. This component contains IOB flip-flops Input/Outputblock(IOB) buffers.

4. RESULT

Isim is a Xilinx simulation provides a complete, full featured hdl simulator which is integrated within the ISE tool. Xilinx Isim is a Hardware Description Language (HDL) simulator that helps to perform behavioral and timing simulations for VHDL. A test bench was created for the user logic module to initially simulate and verify its working.

The csbar signal is generated based on the clkout and timing at which control word is given to the digipot. The csbar signal is set low when the control word is available at the SDI pin of the digipot and made high when the control word is ready to be written on to the RDAC register. The sync pulse which is necessary to activate the ADC is set as an active low pulse of small duration. The simulation result for generating digipot and ADC control signals is shown in the figure fig10.

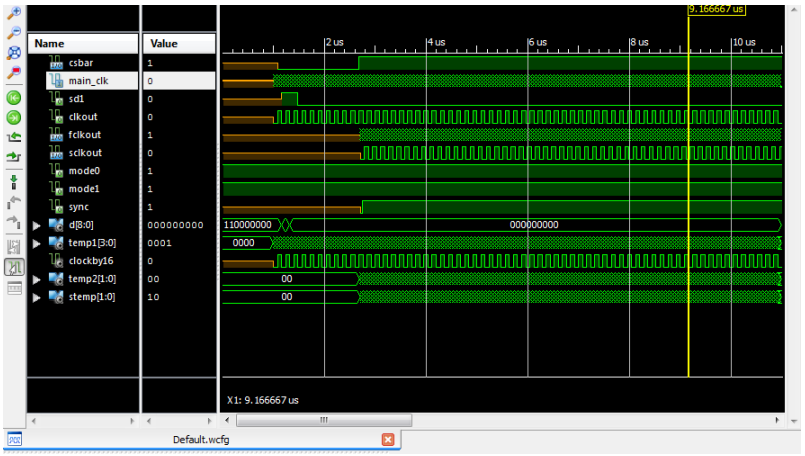

Fig 10: Generated Digipot and ADC control signals

On the application of the control signals, serial data bits were available at the output pin of ADC along with DRDY signal. The experimental results are shown in Fig11 and Fig12.

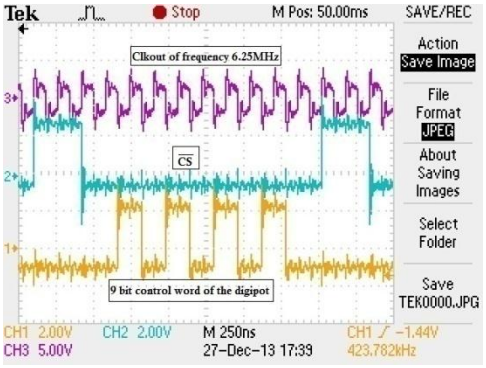

Fig.11: Generated control signals along with the required serial control word of AD5262

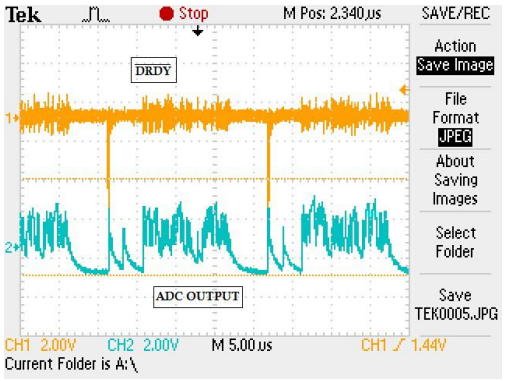

Fig.12: The output signals from ADS1278

It was observed that all the control signals namely sof_out_n, eof_out_n, src_rdy_out_n and dst_rdy_n were generated accurately, with initially the header information being transmitted through data[7:0] followed by the data field. Sof_out_n signals the beginning of frame transmission, eof_ot_n signals the end of a frame transmission, and src_rdy_out_n signals presence of valid data on data_out[7:0]. The simulation results are shown in Fig13.

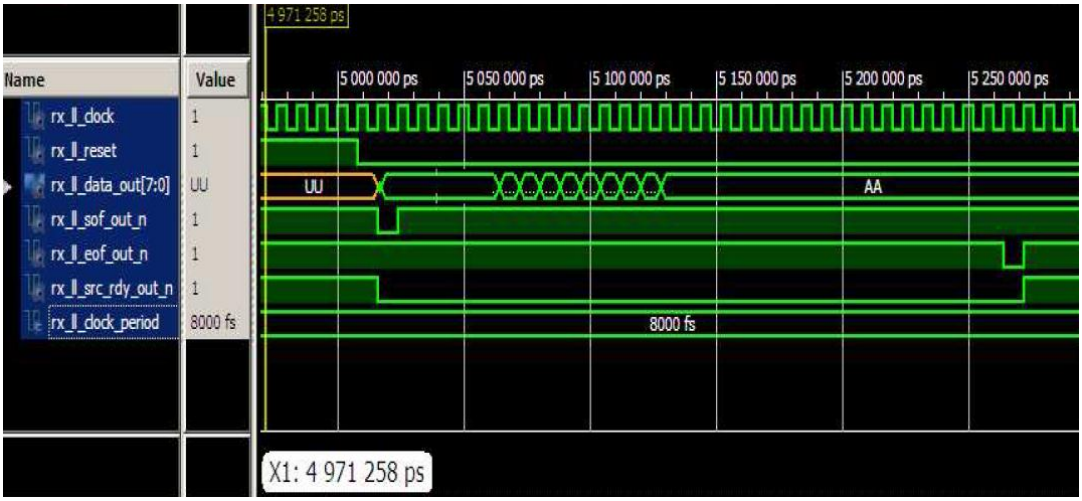

Fig13: User logic simulation results Expanded waveform

The serial data transmitted through Ethernet cable is captured using Wireshark software and the resultant data shown in Fig 14

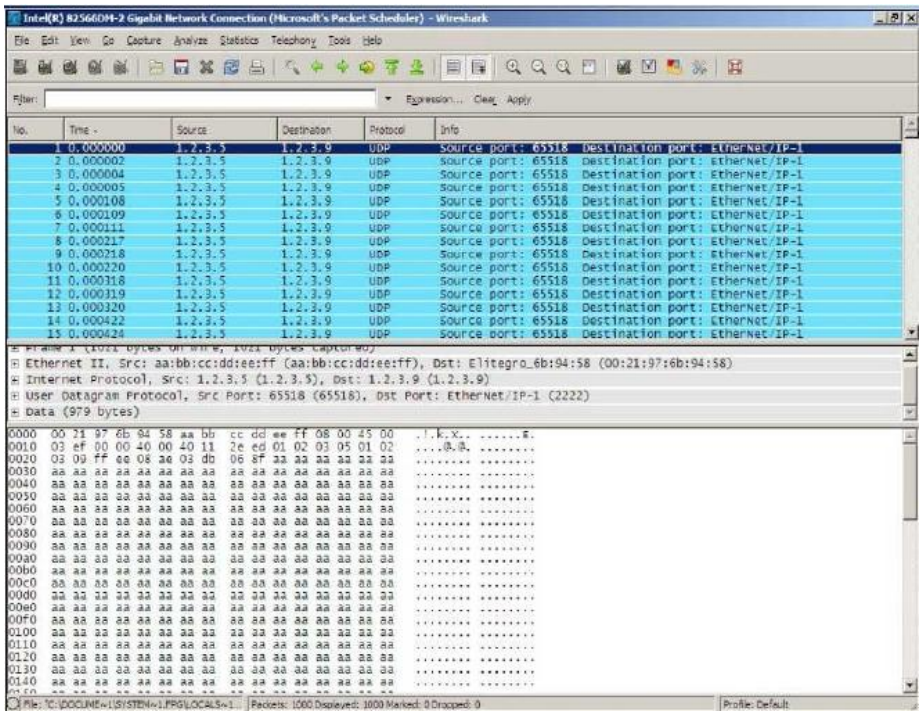

Fig14: Transmitted packets captured in Wireshark

5. CONCLUSION

The development of alow-costreal-time Data Acquisition System on FPGA and interfacing with Ethernet was studied. This paper presents an attractive combination of low cost and high performance,along with an apparent flexibility. A framework has been developed suitable for the development of an FPGA based DAQ using SPI and Ethernet protocols suitable for Sonar.This framework deceives many of the difficult issues associated with the existing DAQs, making it usable even by less-experienced developers. The potential interms off lexibility is of particular interest, asitis the key to developing large,scalable,independent data acquisition systems.

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