ERROR CORRECTION FOR PARALLEL FIR FILTERS USING HAMMING CODES

Ramya Nallagopula[1] and Murthy Raju Kommisetty[2]

[1]M.Tech-VLSID, SVECW (Autonomous), Bhimavaram,Andhra pradesh
[2] Associate Professor, SVECW (Autonomous), Bhimavaram,Andhra Pradesh

ABSTRACT

In this paper ,we propose a error correction for parallel FIR filters using Hamming code in which single parallel FIR filter is taken as a bit in ECC technique. In many complex circuits, reliability plays a crucial role and it requires fault tolerant filter implementations. Now a days, technology grows up, the complex system use many filters which operates simultaneously. Consider an example in which same parallel filter is applied to different inputs. To achieve fault tolerance, an ECC technique uses the presence of parallel filters are considered. The ECC technique provides protection where more number of parallel filters are used by using the case study, the effectiveness in error correction and circuit design cost is evaluated.

KEYWORDS

Soft Errors, FIR filters, Error Correction Codes.

1. INTRODUCTION

Digital filters plays a vital role in DSP systems. Now-a-days, complex circuits are rapidly increasing in many applications in which their reliability is critical.To meet the intrinsic reliability challenges like manufacturing variations and soft errors,fault tolerance is introduced. If redundancy is added at the logic level the faults occurred in the circuit can be reduced and its system functionality will not be affected by those errors. The common technique i.e. ,Triple Modular Redundancy (TMR) is used to add redundancy.TMR triples the input block and to correct errors it adds voting logic.The disadvantage of TMR is the area and power of the circuit is increased and it doesnot acceptable to some applications.

The block diagram for TMR is shown in figure 1,

DOI: 10.5121/ijci.2016.5403

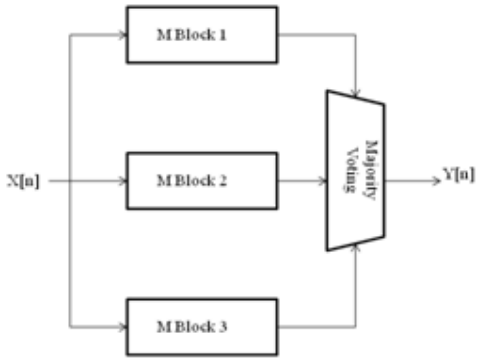

Fig 1:Triple Modular Redundancy

RPR is used to reduce the circuit design cost.The FIR filters protection is done by using residue number system and arithmetic codes are proposed.The Error Correction Codes(ECC's) with hamming protection is presented.when the parallel FIR filters are larger in number,then it enables efficient implementations.By using advanced ECC's can correct failures in multiple modules and powerful protection is also provided.

2.PARALLEL FILTERS WITH SAME RESPONSE

The parallel FIR filter implementations are used for high performance applications.FIR filters are mostly used because they have good stability and they are easily designed to match a given response.
The general FIR filter equation is summerized as,

$$y[n] = \sum_{i=0}^{N-1} x[n-i].h[i] \qquad \text{……..(1)}$$

Consider input data and parallel filters with same response .The diagram for parallel filters are shown in figure 2.

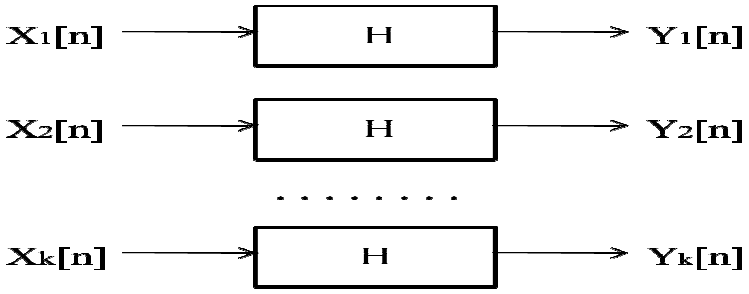

Fig 2:Parallel Filter With Same Response

Hamming codes are used to protect FIR filter to achieve an optimal design and to reduce resource consumption.Hamming codes are also called as block codes and the Hamming Rule is determined as,

$$2^{P} \geq x+p+1 \qquad \text{.....(2)}$$

Where, X : Number of data bits,

P : Number of parity bits.

3.PROPOSED METHOD

By using ECC scheme,the parallel FIR filter with hamming code is designed.Consider an ECC with 4 data bits and 3 parity check bits to produce 7 bits.For example,take a simple Hamming code of K=4 and n=7.By using data bits d1,d2,d3,d4 the parity check bits p1,p2,p3,p4 are computed as a function of,

p1=d1 xor d2 xor d3

p2=d1 xor d2 xor d4

p3=d1 xor d3 xor d4

.....(3)

If there are any errors in one of the bits,the total bits are stored and recovered later.The parity bits are calculated again and by using stored values the results are compared.The Hamming code with generating G matrix and parity check H matrix are,

$$G = \begin{bmatrix} 1 & 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 1 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 0 & 1 & 1 \end{bmatrix} \qquad H = \begin{bmatrix} 1 & 1 & 1 & 0 & 1 & 0 & 0 \\ 1 & 1 & 0 & 1 & 0 & 1 & 0 \\ 1 & 0 & 1 & 1 & 0 & 0 & 1 \end{bmatrix}$$

From above example,

The error in d1 causes errors on p1,p2,p3 check bits and the error in d2 causes errors on p1 and p2 and an error in d3 causes on p1 and p3 and finally error in d4 causes on p2 and p3.
The error bit position is shown in table 1 as,

S_1 S_2 S_3	Error Bit Position	Action
0 0 0	No Error	None
1 1 1	d1	Correct d1
1 1 0	d2	Correct d2
1 0 1	d3	Correct d3
0 1 1	d4	Correct d4
1 0 0	p1	Correct p1
0 1 0	p2	Correct p2
0 0 1	p3	Correct p3

Fig 3:Error Location In Hamming Code

The architecture for 4 parallel FIR filters & hamming code is given in figure 4,

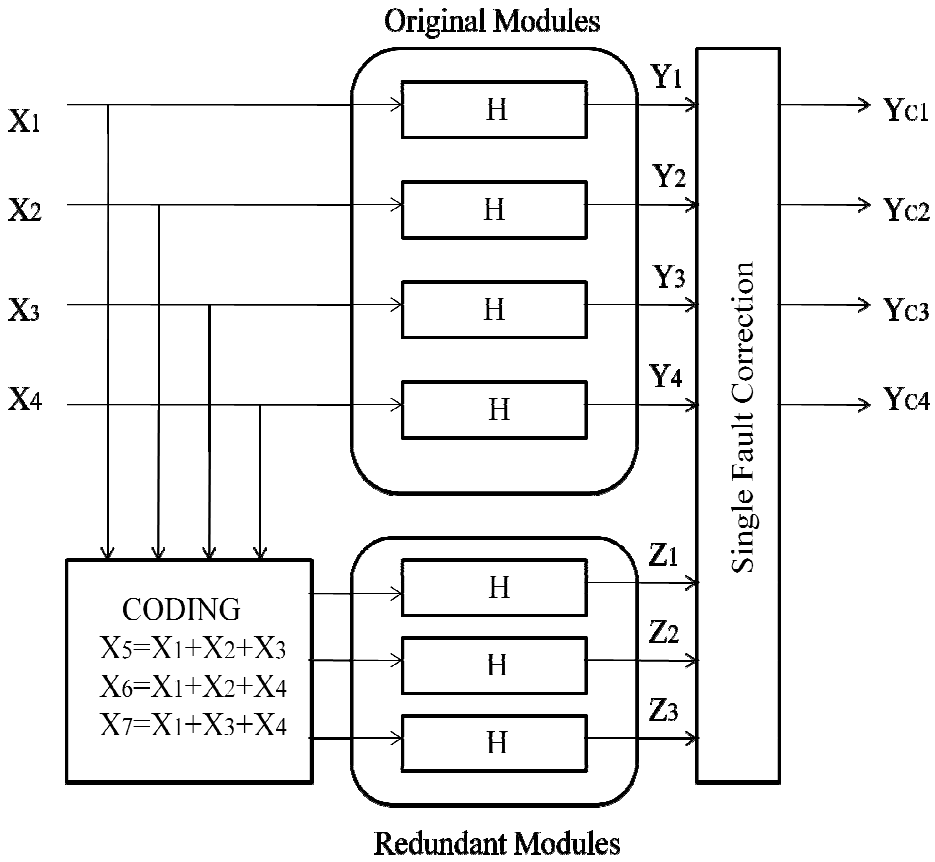

Fig 4:ECC Based Scheme For 4 Filters & Hamming Code

The calculations are, Encoding is calculated as, $y = x \bullet G$ ……..(4)
Where syndrome is calculated as,

$$S = y \bullet H^{T} \quad \text{……..(5)}$$

where • denotes XOR and multiplication operation .To identify the bits in error the syndrome is used for correction.when the error bit is found,it can be corrected by inverting the bit.
The check filters Zj is calculted as,

$$Z_1[n] = \sum_{l=0}^{\infty} (X_1[n-l]+X_2[n-l]+X_3[n-l]) \cdot h[l]$$
$$Z_2[n] = \sum_{l=0}^{\infty} (X_1[n-l]+X_2[n-l]+X_4[n-l]) \cdot h[l]$$
$$Z_3[n] = \sum_{l=0}^{\infty} (X_1[n-l]+X_3[n-l]+X_4[n-l]) \cdot h[l]$$

…….(6)

Checking is done by,

$$Z1[n] = Y1[n]+Y2[n]+Y3[n]$$

$$Z2[n] = Y1[n]+Y2[n]+Y4[n]$$

$$Z3[n] = Y1[n]+Y3[n]+Y4[n]$$

…….(7)

Consider an example ,if an error Y1 is detected the error is corrected by,

$$Yc1[n] = Z1[n] – Z2[n] – Z3[n] \quad \text{……(8)}$$

Consider eleven parallel FIR filters with hamming code of total 15 bits including four redundant bits .The reductions for eleven parallel filters are large only when number of filters are larger.By using the traditional ECC's if number of filter increases,the overheads decreases.There is a trade off between area and delay i.e., if area is increased the delay is reduced in 11 parallel filters.Finally the circuit complexity is less when compared with 4 parallel filters and the circuit cost is also low.The above results are confirmed by using a case study.

By using a case study consider 16 coefficients with input bits and filter coefficients . Two evaluations are implemented for a block of parallel filters with data bits k=4 & k=11 and total bits n=7 & n=15 bits. These techniques are synthesized and simulated by using a Xilinx tool.

The fault injection experiments and effectiveness in terms of error correction is done by using eleven parallel filters.For input filters and the coefficients the errors are injected randomly and in all these cases the single errors can be injected & it can be detected and corrected.So, by using

case study the effectiveness is confirmed to correct the single errors and system cost is determined.

4. SYNTHESIS & SIMULATION RESULTS

The RTL Synthesis and Simulation results for proposed system are given below.

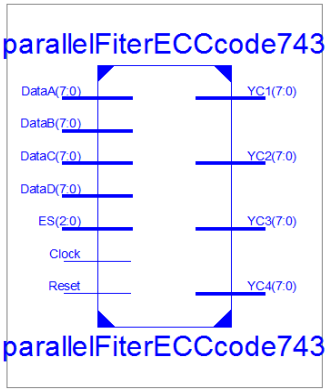

Fig 5:RTL Schematic For 4 Parallel Filters

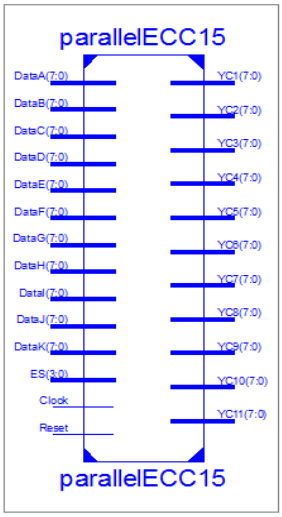

Fig 6:RTL Schematic For 11 Parallel Filters

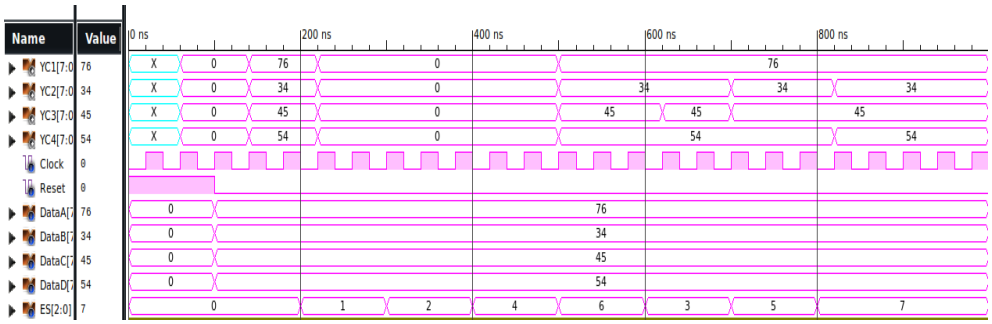

Fig 7:Simulation Result For 4 Parallel Filters

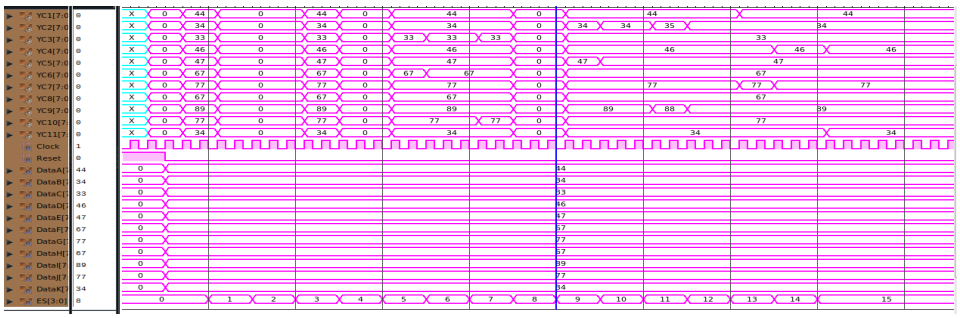

Fig 8 : Simulation Result For 11 Parallel Filters

4.1.Timing Report

For 4 Parallel Filters:

```
Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 2.027ns (Maximum Frequency: 493.340MHz)
   Minimum input arrival time before clock: 3.399ns
   Maximum output required time after clock: 12.031ns
   Maximum combinational path delay: No path found
```

For 11 Parallel Filters**:**

```
Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 2.058ns (Maximum Frequency: 485.909MHz)
   Minimum input arrival time before clock: 4.804ns
   Maximum output required time after clock: 4.368ns
   Maximum combinational path delay: No path found
```

5. CONCLUSION

By using the proposed scheme the protection of parallel FIR filter can be done in DSP systems. The error detection and correction is done by applying ECC's to parallel filter outputs.The effectiveness i.e., circuit overheads and single fault correction is discussed by using case study.The performance is improved in terms of delay is reduced.

The future scope is the scheme is also done for IIR filters instead of FIR filters. Another extension is instead of using hamming codes another error correction codes can be used.

REFERENCES

[1] .S.Ranjani "Multi fault detection and correction using error correction codes and parsevel checks,"IEEE trans.VLSI systems vol .5,special issue 4,march 2016.
[2]. T.Saranya " Highly reliable parallel filter design based on reduced precision error correction codes, "IEEE trans.VLSI syst.,vol.5,issue 1,ver 3, feb 2015,pp.45-48.
[3]. R.Mamatha Rani," Design of low power efficient FIR digital filter,"IEEE trans.VLSI syst.,vol 4,issue 10,October 2014.
[4]. Dhiraj.k.pradhan,"Fault tolerant single error correction encoders," IEEE transactions,springer,30 march 2011.
[5]. L.Jessy,"Design and analysis of algorithm based error detect-corrections of parallel FFT,"vol5,issue3,pp:134-138,march 2016.
[6]. P.Jeevitha,"Application of error correction code for pipelined filter with efficient addition structure,"IJSETR,vol 3,issue 11,Nov 2014.
[7]. P.Sneha ,"FPGA implementation of RPR protected parallel FIR filters," IEEE trans.,vol 10,issue 3,pp:57-64,june 2015.