NOISE IMMUNE CONVOLUTIONAL ENCODER DESIGN AND ITS IMPLEMENTATIONIN TANNER

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ABSTRACT

With the rapid advances in integrated circuit(IC) technologies, number of functions on a chip was increasing at a very fast rate, with which interconnect density is increasing especially in functional logic chips. The on-chip noise affects are increasing and needs to be addressed. In this paper we have implemented a convolution encoder using a technique that provides higher noise immunity. The encoder circuit is simulated in Tanner 15.0 with data rate of 25Mbps and a clock frequency of 250MHz

KEY WORDS

Noise immune design, Convolutional encoder design.

1. INTRODUCTION

Due to the rapid advances in integrated circuit technologies,with the advent of VLSI,The electronics industry has achieved a phenomenal growth over the last few decades,The number of applications of been rising steadily, and at a very fast pace. Typically, the required computational power (or, in other words, the intelligence) of these applications is the driving force for the fast development of this field.

The design complexity of logic chips increases almost exponentially with the number of transistors to be integrated. As the technology aggressively scales down, the density on the chip have increased and hence the interconnection density, leading to increased interaction among the connections and thereby increasing crosstalk and system failures.

On the other hand with the decrease in supply, the gate threshold is decreased to preserve system throughput and so leakage currents have increased. And therefore the noise margins have greatly reduced. The noise immunity is of more concern in high fan-in circuits as they have larger leakage due to more parallel evaluation paths. As the number of parallel paths(fan-in) increase in the design, the noise immunity of the design decreases. The circuits with wide fan-in include coding and decoding circuits in communications, address decoding and encoding, data sequencing and timing control in computational applications.

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PROBLEM STATEMENT

The basic digital communication system employs various encoding and decoding circuits as shown in Fig. 1. Forward error correction schemes are generally used in transmitter to encode the data or information and in receiver to detect and correct errors.

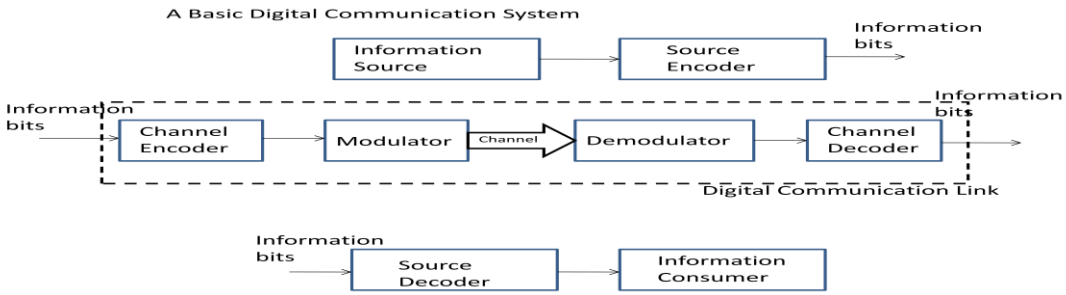


Fig.1 Basic Digital Communication System

Forward Error Correction (FEC) in digital communication system improves the error detection as well as error correction capability of the system at the cost of increased bandwidth and system complexity. Using FEC the need for retransmission of data can be avoided hence it is applied in situations where retransmissions are relatively costly or impossible. FEC codes can be classified in two categories namely block codes and convolution codes. Block codes operate on fixed size data blockswhere as convolution codes operate on arbitrary length data blocks. A convolution coder is often used in digital communication systems where the signal to noise ratio is very low. Error detection and correction or error control arethe techniques that enable reliable delivery of digital data over an unreliable (noisy) communication channel. Many communication channels are subject to channel noise, and thus errors may be introduced during transmission from the source to a receiver. Error detection techniques allow detecting such errors, where aserror correction techniques allow for the reconstruction of the original data.

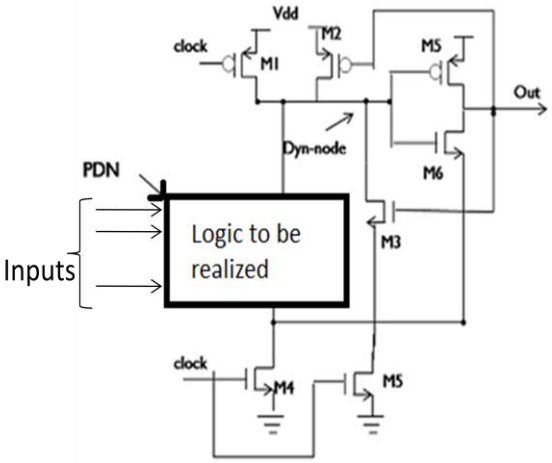
As the encoder circuits comprise of high fan-in gates, when implemented in nano-metric technologies, are prone to noise effects. In the chips which realize logic, most of the chip area is used in providing interconnections and because of their high density; interaction among them would be more. This large inter coupling among the wires introduces noise in the nearby wires which in turn may result in errors in function realization, especially when the encoder input gets corrupted, it results in unrecoverable error at the output of the encoder. Thus we have designed a convolution encoder with a technique which is more noise immune and simulated the design.
In section II we discussed the noise immune technique, Section III deals with Convolution encoder design ,in section IV, simulation results and in section V conclusion were presented.

2. NOISE IMMUNE GATE DESIGN

Dynamic logiccircuits find their wide application in high speed, low power areas such as microprocessors, digital signal processing, dynamic memories etc., because of their low device count, high speed, short circuit power free and glitch free operation [2]. On the other hand it is also possible to design a dynamic logic unit that is smaller than its static counterpart. Dynamic logic consists of pull down network realizing the logic.

From the basic theory of dynamic logic, large amount of noise gets induced and power consumption increases. Dynamic logic suffers from charge sharing and cascading. To overcome these problems domino logic was proposed. When a dynamic gate is cascaded by a static inverter, it is called Domino logic. For the same output current and a lower switching threshold, aDomino gate runs faster thanits static counterpart as they present much lower input capacitance.

The proposed domino circuit is shown in the Fig.2 [3]. Transistor M3 and M5 are connected between the dynamic- node and ground, gate ofM3 transistor is connected to the OUT terminal and M3 is stacked with M5. During evaluation phase when PDN is on with one or more inputs connected to logic one, the transistor M4 discharges the dynamic-node and the Out terminal goes to logic '1' and M3 becomes on which aids in faster discharge of any accumulated charge on dyn_node along with PDN and M4. The rate of discharge can be controlled by varying the W/L ratio of M4. When all the inputs are at logic '0', output stay at logic '0' and M3 remains off and thus dyn_node retains its charge. If any input changes from logic '0' to logic '1' , PDN becomes conducting and during evaluation phase when clock is high, dyn_node discharges below V_t of the inverter turning its output to logic '1'. When output becomes logic '1', M3 turns on providing a path to discharge dyn_node quickly as M5 is also ON during evaluation phase. At the same time as the source node of M6 being connected to N-foot, effect of noise in the circuit can also be reduced. An Ex-or gate of the proposed technique is implemented and simulated.



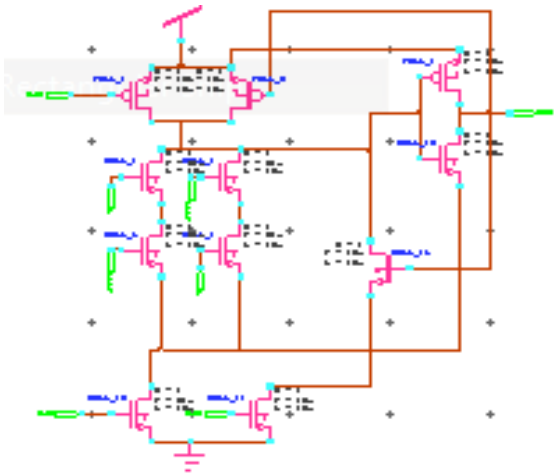


Fig.2 Proposed noise immune technique. Fig.3 Two inputs Ex-OR gate of the proposed technique.

3. CONVOLUTIONAL ENCODER DESIGN:

Convolution codes operate on arbitrary length data blocks. The convolution coder is often used in digital communication systems where the signal to noise ratio is very low. In this, the encoding operation may be viewed as discrete time convolution of input sequence with the impulse response of the encoder.

Convolutional codes are commonly specified by three parameters, (n,k,and m),Where n represents the number of output bits,krepresents number of input bits andm, the number of registers. [4] Code rate k/n is measure of efficiency of the code. Generally k and n range from 1 to 8, m from 2 to 10 and code rate from 1/8 to 7/8 except for deep space applications where code rates as low as 1/100 or even longer will be used[4]. Convolutional code chip manufacturers often specify the code by parameters (n,k,L), where L is constraint length, defined by L = k(m-1), and

represents the number of bits in the encoder memory that effect the generation of the n output bits[4].

As a bit is shifted along the register it becomes part of other output symbols sent. Thus the present output bit that is observed has information about previous input bits. A convolution encoder used shown in Fig.4. It is assumed here that the shift register shifts in one bit at a time and outputs three bits, though other combinations of input to output bits are also possible.

Input[S1]	[S2 S3]	[O1 O2 O3]
0	0 0	0 0 0
1	0 0	1 1 0
0	1 0	1 1 0
1	1 0	0 1 1
0	1 1	0 1 1
1	1 1	1 1 0
0	0 1	1 0 1
1	0 1	0 0 0

Table 1. Encoder Transition table

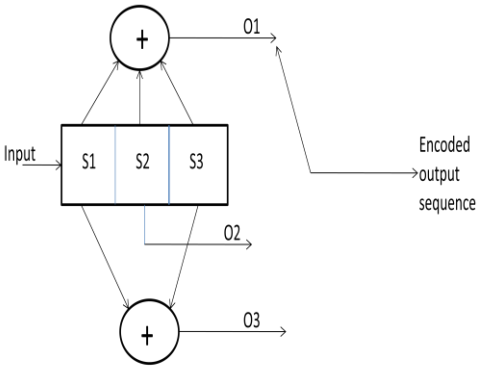


Fig.4. Convolutional Encoder

Here the present input bit is shifted intoS1,S2 and S3 holds the previous bits thus defining the state of the encoder. For every input bit there are three output bits (O1, O2,O3), thus code rate is 1/3. The transition tabledefines the output of the encoder for given state and input (Table.1).
It is the code generation polynomial which gives a unique error detection quality for a generator.For example a list of Generator polynomials found by Busgang for good rate 1 /2 codes is shown in Table.2, as can be seen from the table that fan-in of summing circuit (here EX-OR) is increasing with constraint length. Thus as the fan-in increases the effect of on chip noise at will be more and thus can cause errors in the coded output, and cannot be recovered at the receiver as the encoder output itself is erroneous. Thus to eliminate such type of error, Ex-or gate should have high noise immunity.

Constraint Length	G1	G2
3	110	111
4	1101	1110
5	11010	11101
6	110101	111011
7	110101	110101
8	110111	1110011
9	110111	111001101
10	110111001	1110011001

Table.2 Generator Polynomials found by Busgang for good rate ½ codes

The encoder circuit is thus implemented with a gate having high noise immunity as reported in [4]. Two input and three input ex-or gates were implemented and simulated with the proposed technique.

4. SIMULATION AND RESULTS

Simulations were done on Tanner T-spice 15.0 with 16nm technology PTM files with 1V supply. The encoder circuit is implemented in three design techniques namely footless domino gate with keeper (FLDG Keeper), Scheme [8] technique and Noise immune proposed technique. All the circuits were simulated with 250MHz clock and data rate of 25Mbps.

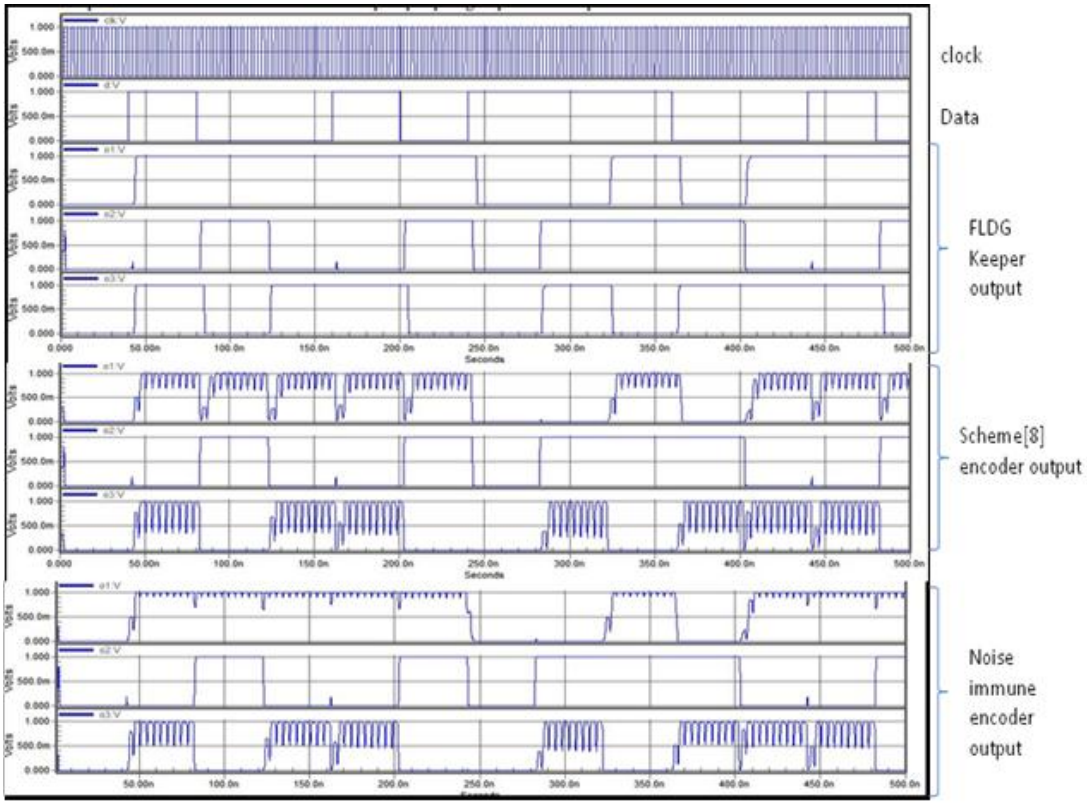


Fig.5. Simulation results of convolutional encoder using three different techniques

From the simulation result we have observed that the proposed technique has less- ripple in the output and more noise immune as EX-OR gates are implemented with noise immune design technique.

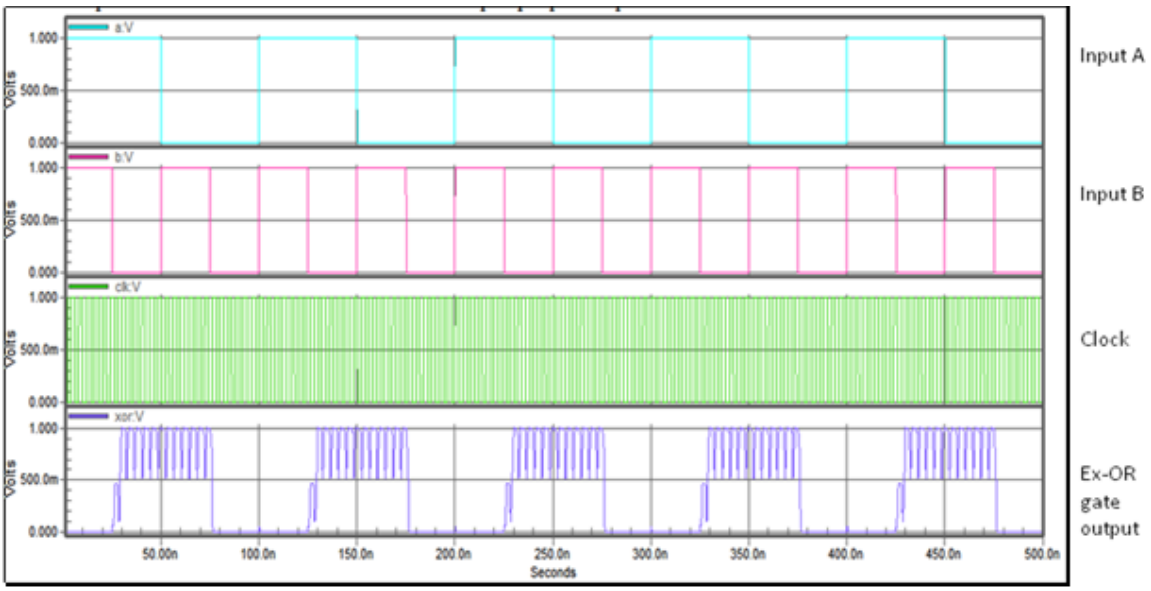


Fig.6. Simulation result of two input Ex-OR gate.

Fig. 6 shows the simulation output of two inputs Ex-OR gate with noise immune technique.

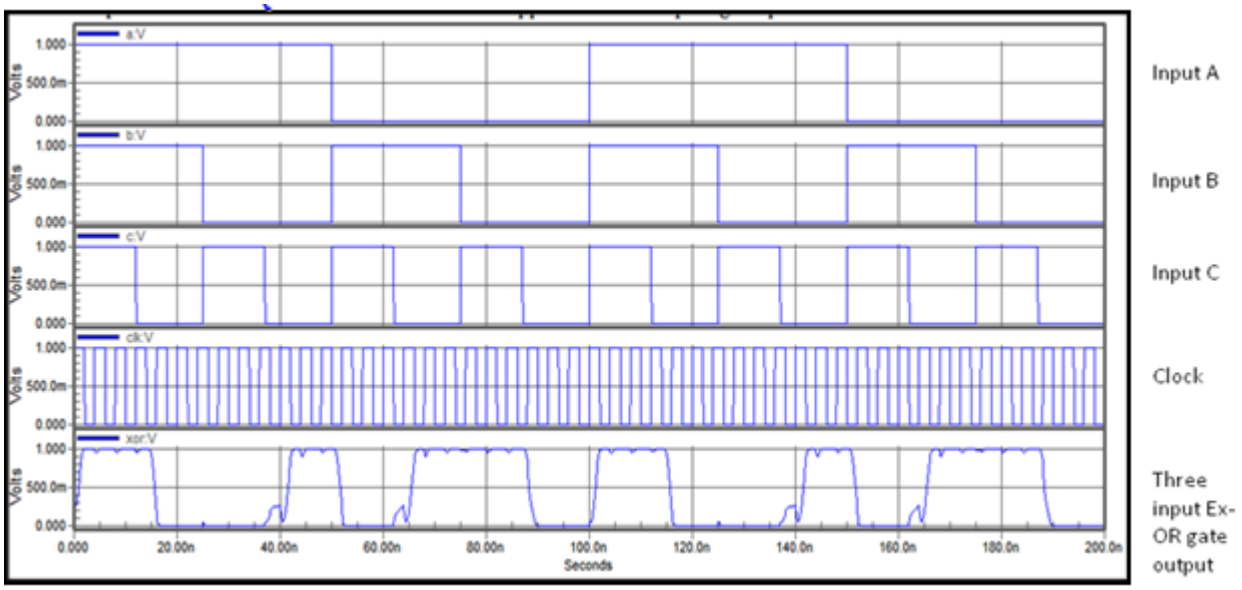


Fig.7 Simulation result of three input Ex-OR gate.

Fig. 7 shows the simulation output of a three input Ex-OR gate with noise immune technique.

CONCLUSION

In this paper we have presented theimplementation results of a rate 1/3 convolutional encoder with input data rate of 25Mbps and Clock rate of 250MHz. The circuit is implemented in three different techniques and their simulation results were presented, and found that the proposed technique has fewer ripples in the output and is more noise immune.

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