DESIGN ANDIMPLEMENTATION OF EFFICIENT TERNARY CONTENT ADDRESSABLE MEMORY

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ABSTRACT

A CAM is used for store and search data and using comparison logic circuitry implements the table lookupfunction in a single clock cycle. CAMs are main application of packet forwarding and packet classification in Network routers. A Ternary content addressable memory(TCAM) has three type of states '0','1' and 'X'(don't care) and which is like as binary CAM and has extra feature of searching and storing. The 'X' option may be used as '0' and '1'. TCAM performs high-speed search operation in a deterministic time. In this work a TCAM circuit is designed by using current race sensing scheme and butterfly matchline (ML) scheme. The speed and power measures of both the TCAM designs are analysed separately. A Novel technique is developed which is obtained by combining these two techniques which results in significant power and speed efficiencies.

KEYWORDS

Content Addressable Memory (CAM) Circuit, XOR-based conditional keeper, Ternary Content Addressable Memory (TCAM)Circuit,Pseudo-Footless Clock Data Pre-charge Dynamic Match line (PF-CDPD)Architecture.

1. INTRODUCTION

Ternary Content Addressable Memory (TCAM) is the useful for search and store ternary values and used for partial data matching. TCAMs are composition of conventionaltype semiconductor memory with addition of comparison circuitry. The most common application of TCAMs arepacket forwarding and packet classification.

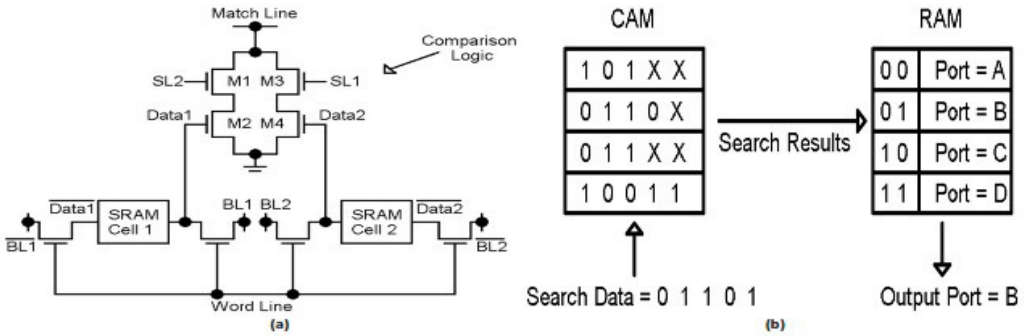

Fig 1(a) Conventional TCAM (b) Address lookup with TCAM/RAM

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A TCAM contains two parts.Static RAM cells and a comparison logic circuit. These are shown in Fig.1.Both NOR and NAND versions are used to design TCAMs. But NOR type is used to design TCAM because higher speed. The stored data (D1, D2) is referred as three type of states such as '1', '0' and don't care(X).Search data (SL1, SL2) is present and it is provided through search line pair. In case of a mismatch the ML is connected to ground through one of the paths M1,M2 or M3,M4.In the case of a match (D1D2=SL1SL2) there is no connection to ground. So, reduction ofpower consumption is reduced to design TCAM.

Fig1 (b) shows TCAM system as a complete implementation of an address lookup function. The match address output of the CAM is in fact a pointer used to retrieve associated data from RAM. In this case the associated data is the output. The TCAM search can be viewed as a dictionary lookup where the search data is word to be queried.

2. MATCH LINE TECHNIQUES

2.1.1 Current Race Scheme

The Current Race Scheme is the one of the matchline techniques. The scheme achieves the 50% of power saving. The scheme starts with the precharges the matchline (ML) low and evaluatesmatchline (ML) state is the chargewith the current I_{ML} is placed by a current source. The precharge signal of the matchline low when it starts the prechrging search cycle. thematchline is precharging low, then scheme charges the search lines/match lines to their search data values, eliminating the need for a separate SL precharge phase required by the precharge-high scheme. After the Search Line/Match Line precharge phase completes, current source to matchline is connected to enable signal. In match state the matchline (ML) is in high voltage, while in the miss state it is in low voltage. thevoltage of only I_{ML} x R_{ML}/M. The ML is connected to nMOS transistor, M_{sense}. The output of nMOS transistor M_{sense} is stored by half latch. The main reason of the ML is precharged low because of the scheme allow changing the CAM cell configuration. Hence there is no charge sharing problem when precharge low in the CAM cell configuration.

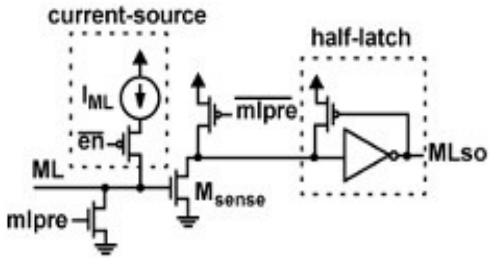

Fig 2(a) current race scheme

2.2.1 Butterfly ML TCAM

The butterfly match-line (ML) TCAM scheme is proposed using pseudo-footless clock data pre-charge dynamic (PF-CDPD) structure. It is associatedthe each pipelined stage is in the butterfly associationstructure which is utilized for diminish thepower consumption and search time. The powerutilization on the search line is reduced without any search time overhead. A noise-tolerant

match-line (ML) scheme with XOR-based conditional keeper is introduced to diminish the power consumption and search time. With the specific end of the goal to reduce the search time overhead caused by butterfly connection style the XOR-based conditional keeper system can decrease delay of critical path of the match-line. Figure 2(b) shows the butterfly connection structure. Thetwo CAM segments are associated in the butterfly connection structure. The two CAM segments are connected using two input NOR-gate, and controlled signal of next stage is generated by the two input NOR-gate output. The proposed four segment butterfly match-line scheme with XOR-based conditional keeper gives the power saving and high performance.

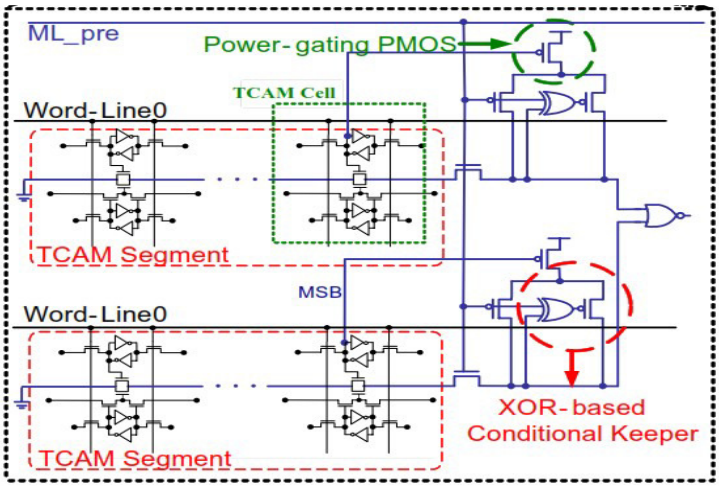

Fig 2(b) butterfly ML TCAM

2.3.1 Novel Technique

The novel technique is designed by using combining the current race scheme and butterfly match-line (ML) scheme. In the current race scheme the Match Lines are pre-discharged to ground.Match Line (ML) enable signal initiates the search operation. During the search operation MLs are charged towards high. Search Lines are need not to be precharged to ground in the technique. This reduced search line switching activity compared to the conventional scheme saves around 50% power. And Current Race scheme reduces the search time also.

In the butterfly match-line (ML) in order to reduce search time overhead caused by butterfly connection, a XOR-based conditional keeper technique is applied. The XOR-based conditional keeper is the turned off and it is used for to reduce the search time and power consumption.

Due to this butterfly connection style, this circuit has got high-degree of parallelism since it can do search operation of all TCAM cells at a time. Hence, because of this power of this circuit has been reduced considerably when compared to that of conventional TCAM cell.

2.3.2 Advantages of Novel Technique

The butterfly ML scheme could reduce about 82.2% of match-line power. And current race scheme reduce the delay of 41.2% of match-line power. So, we design a novel technique by combine these two techniques reduce the both power as well as delay of the circuit.

3. SIMULATION RESULTS

The Design and the implementation of the power reduction techniques have been carried out in Tanner tool 13.0 version software tool of 0.18µm CMOS technology. The specifications that are followed in the simulation results are shown in the table 3.1. The most power consuming task is the search operation in the TCAM access. The different techniques have been used to reduce power reduction and how far power and delay savings compare to traditional TCAM.

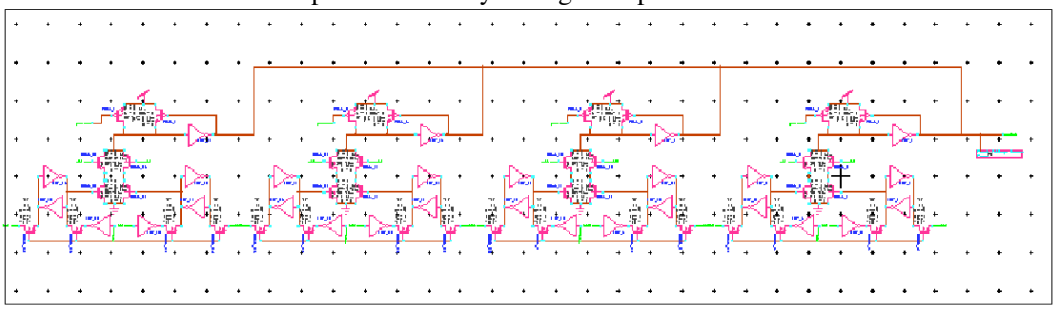

Fig 3.1(a) Circuit schematic conventional 4-bit TCAM cell with comparison and storage parts

Figure 3.1(a) shows the Schematic conventional 4-bit TCAM cell. Here four TCAM cells are connected in series. Each TCAM cell has comparison logic and storage parts.

Fig 3.1(b) Speed analysis of Conventional TCAM

Figure 3.1(b) shows the Conventional TCAM Speed analysis. The speed obtained is 2.47 Seconds.

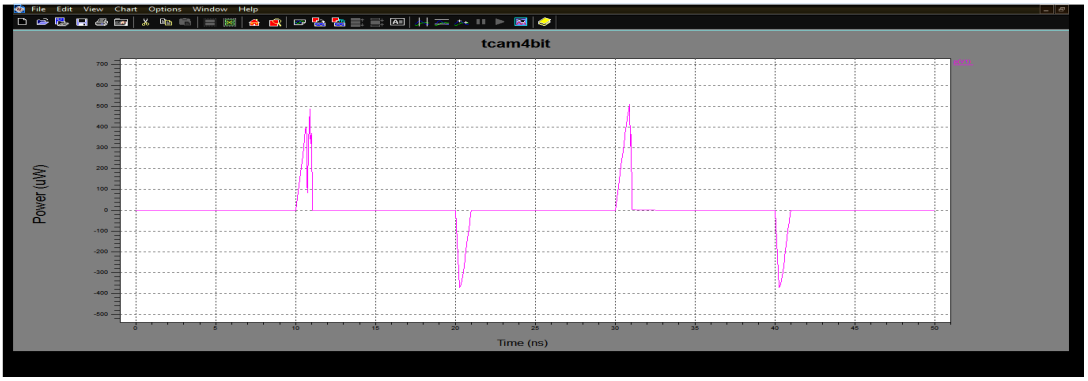

Fig 3.1(c) power analysis of Conventional TCAM

The figure 3.1(c) shows the power analysis conventional TCAM cell, which is used to compare the power reduced value to that of various implemented power reduction techniques. Here the power consumption obtained is 508µW.

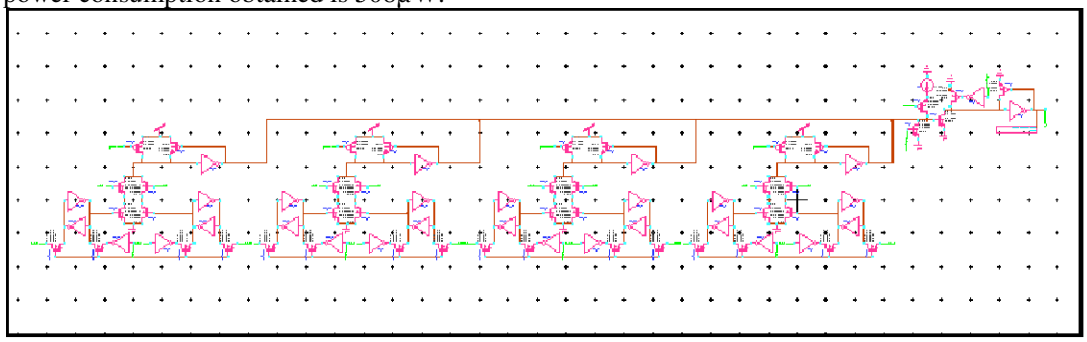

Fig 3.2(a) Circuit schematic of the proposed current race technique

Figure 3.2(a) shows the 4-bit TCAM with proposed current race scheme. The current race scheme is designed by connecting the conventional TCAM with current race scheme part. This is designed in Tanner tools software.

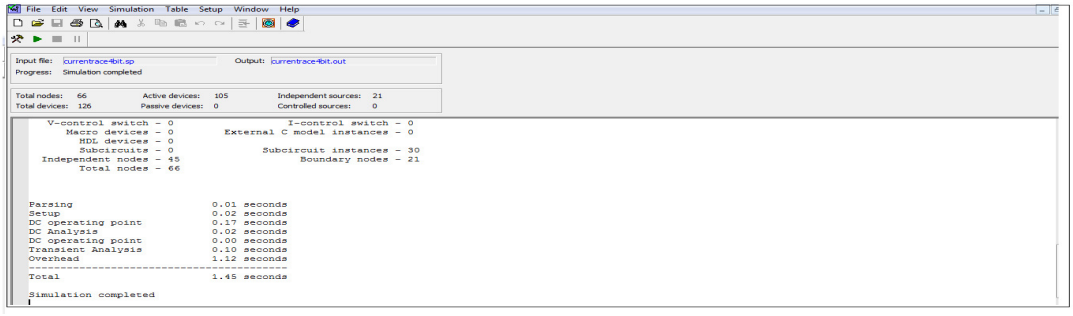

Fig 3.2(b) Speed analysis of the proposed current race technique

A figure 3.2(b) show the proposed current race scheme speed analysis and obtained the speed is 1.45 Seconds. The speed is better compared to conventional TCAM.

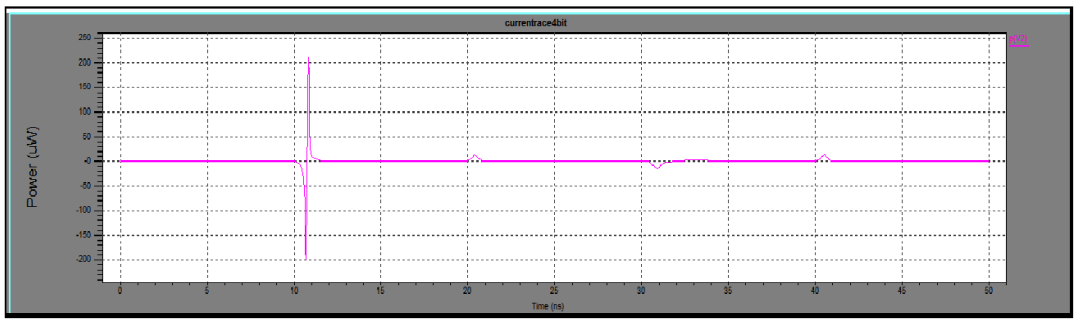

Fig 3.2(c) power analysis of the proposed current race technique

Figure 3.2(c) shows power analysis of the proposed 4-bit TCAM with the current race technique. During the ML charging phase Current race scheme passes similar currents to both matched and mismatched MLs. So, here in large number of mismatched MLs large amount of energy wasted. Hence the CR scheme is reduce the currents to the mismatched MLs. The obtained power consumption is 212µW.The current race scheme is reduce power is 58% and delay is 41% compared to Conventional TCAM.

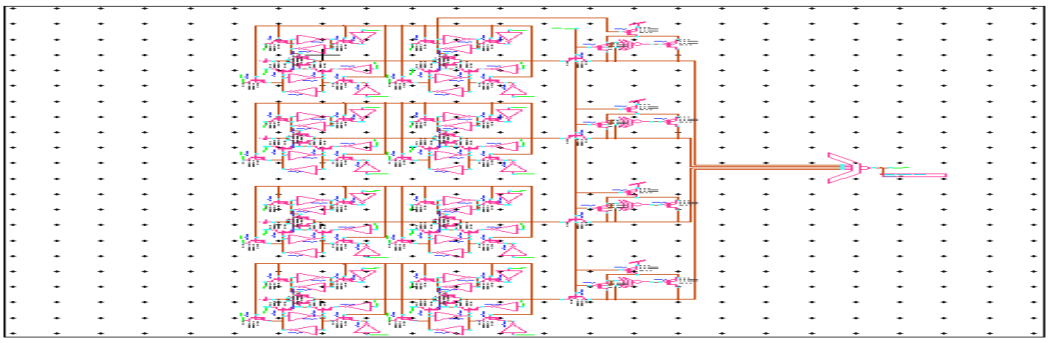

Fig 3.3(a) Circuit schematic of the 4-segment butterfly ML scheme

Figure 3.3(a) shows the 4-segment butterfly match line scheme which is connected the TCAM segments are in pipelined architecture. Four TCAM segments are connected with NOR gate.

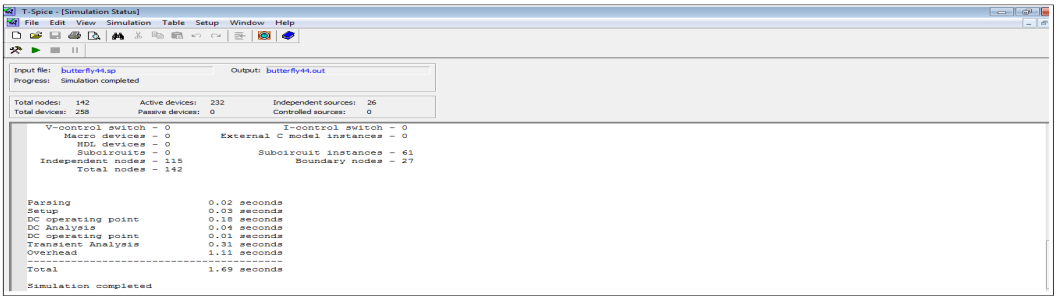

Fig 3.3(b) speed analysis of the butterfly ML scheme

Figure 3.3(b) shows the speed analysis of butterfly match line scheme and obtained speed is 1.69 Seconds.

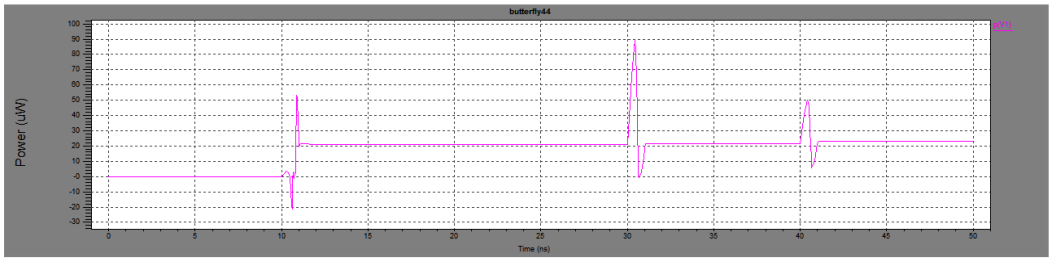

Fig 3.3(c) power analysis of butterfly ML scheme

Figure 3.3(c) shows the power analysis of 4-segment butterfly ML TCAM employing TCAM structure of Asymmetric TCAM cell model. Due to this butterfly connection style, the circuit has got high degree of parallelism since it can do search operation of all TCAM cells at a time. Hence because of this power of this circuit has been reducedwhen compared to the conventional TCAM cell. And obtained power is 90µW.and butterfly ML technique is reduce power is 82% and delay is 31% compared to conventional TCAM.

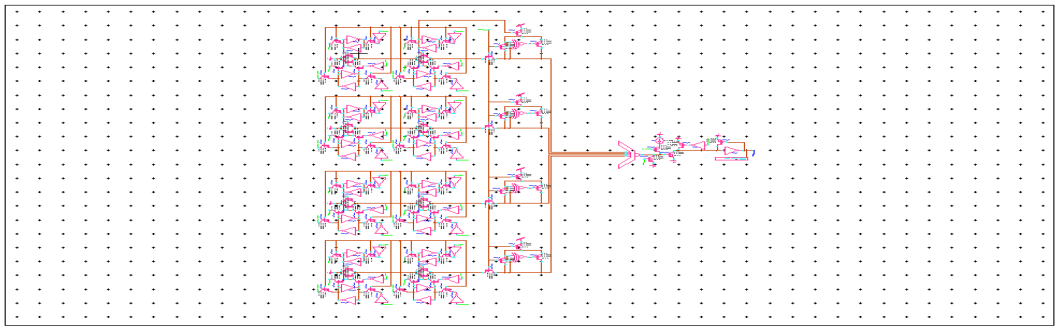

Fig 3.4(a) Schematic implementation of Proposed Novel technique

Figure 3.4(a) shows of the schematic implementation of proposed novel technique which is designed by combining the butterfly match line scheme and current race scheme.

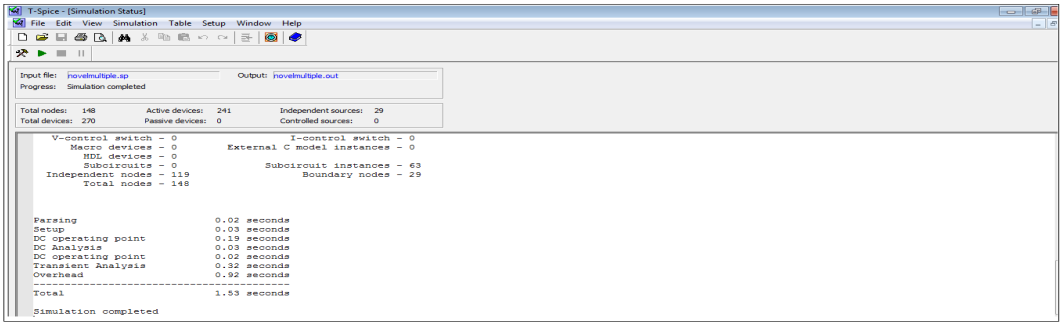

Fig 3.4 (b) speed analysis of Proposed Novel technique

Figure 3.4(b) shows the Speed analysis of proposed novel technique and obtained speed is 1.53Seconds.

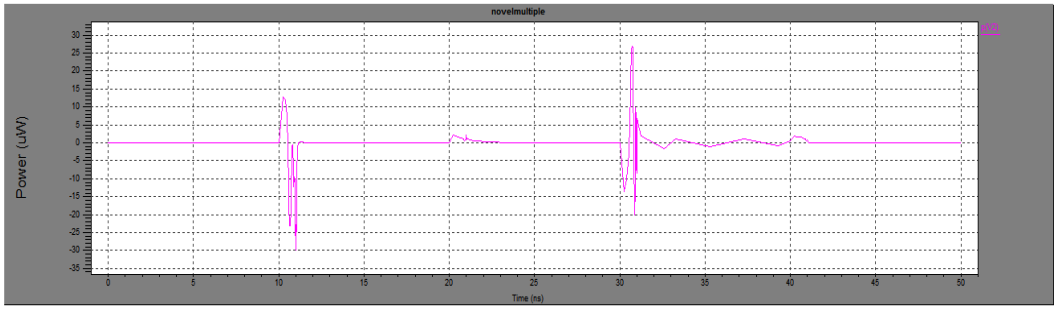

Fig 3.4(c) power analysis of Proposed Novel technique

Figure 3.4(c) shows the power analysis of the Proposed Novel technique and obtained power is 27µW. The Proposed novel technique is designed by combine the current race technique and butterfly ML technique. So combine the both techniques we obtain the power is reduced by 94% and delay is 38% compared to conventional TCAM.

Table 3.1: Tabulated Results

Proposed Configuration	**Power (µW)**	**Speed(Secs)**	**Power reduced compare to TCAM**	**Speed increased compare to TCAM**
Conventional TCAM Circuit	508	2.47		
Proposed Current Race Scheme	212	1.45	58.26%	41.29%
Butterfly Match Line Scheme	90	1.69	82.28%	31.57%
Proposed Novel Technique	27	1.53	94.68%	38.05%

CONCLUSIONS

An energy efficient Novel ternary content addressable Memory design is proposed in this paper. The reduction of high power consumption and delay which are the limiting factors of TCAM has been achieved by various power reduction techniques which are implemented in 0.18µm CMOS technology. The Novel technique is designed which is reduced power up to 94% and increased speed up to 38.05% compared to Conventional TCAM.

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