WAVELET BASED ON THE FINDING OF HARD AND SOFT FAULTS IN ANALOG AND DIGITAL SIGNAL CIRCUITS

[1]Gurunadha.Ravva [2]k.Babulu and [3]p.srinivasa rao

[1]Department of ECE, JNTUK-UCEV, Vizianagaram, Andhra pradesh, India
[2]Department of ECE, JNTUK-, vizianagaram, Andhra pradesh, India
[3] Department of ECE, JNTUK-UCEV, Vizianagaram, Andhra Pradesh, India

ABSTRACT

In this paper methods for testing both software and hardware faults are implemented in analog and digital signal circuits are presented. They are based on the wavelet transform (WT). The limit which affected by faults detect ability, for the reference circuits is set by statistical processing data obtained from a set of faults free circuits .In wavelet analysis it has two algorithm one is based on a discrimination factor using Euclidean distances and the other mahalanobis distances, are introduced both methods on wavelet energy calculation. Simulation result from proposed test methods in the testing known analog and digital signal circuit benchmark are given. The results shows that effectiveness of existing methods two test metrics against three other test methods, namely a test method based on rms value of the measured signal, a test method utilizing the harmonic magnitude component of the measured signal waveform.

.KEYWORDS

Faults dectection, simulation distance measurement eudiean distance and mahanolobis distance,

1. INTRODUCTION

A software simulator is a computer program; an emulator is a hardware simulator. Simulation is used for design verification that is validating assumptions, verify logic, verify performance (timing). Types of simulation are logic or switch level simulation, timing simulation, circuit simulation; fault simulation.Fault models are analyzable approximations of defects and are essential for a test methodology [1]. For digital logic circuits, single stuck-at fault model offers best advantage of tools and experience. Many other faults (bridging, stuck-open and multiple stuck-at) are largely covered by stuck-at fault tests. Stuck-short and delay faults and technology-dependent faults require special tests. Memory and analog circuits need other specialized fault models and tests.

Ladder Filters circuits are popular for realizing analog integrated circuits and also popular for designing analog circuits in modern mixed signal IC [2]. So it can be most easily realized with Z-transform techniques and typically require anti aliasing filter, smoothing filter. Accuracies of key parameters clock frequency, as well as the capacitor ratios and remain accurate with temperature. In single stage operational amplifier doubling of the load capacitance halves the unity gain frequency and improves the phase margin. The finite slew rate may limit the upper clock speed. on-zero DC offset can result in a high output dc offset, depending on the topology chosen, especially if correlated double sampling is not used.

DOI: 10.5121/ijci.2016.5431

.Simple faults are for the most part characterized into two indexes hard and parametric shortcomings. A hard blame that progressions the circuit netlistv, for example, a stuck at 0 and struck at 1(short or open wire)[3]. Hard blames for the most part result in an emotional change of the circuit under test (CUT) exchange capacity. In delicate deficiencies speak to parameter movements of the parts in the CUT, for example, varieties of , trans-conductance resistance Sudan changes of the coefficients in the exchange capacity of the CUT. The considerable achievement of the stuck-at shortcoming model of advanced circuits roused looks into to extend its applications to simple circuits.

Delicate faults are hard to test in labs. The fundamental issue of testing delicate flaws is shortcoming rundown of a solitary parameter comprises of interminable number of qualities The unbounded delicate issue list makes the deficiency reproduction time illogically long. To address this issue, proposed receiving the auxiliary data of the CUT to lessen the span of the shortcoming set. Another way to deal with rate

1.1 Objective Of The Paper:

This paper is to verify and design the fault model that can be applied for analog circuits. In general, the fault simulation time for analog circuits is large and no exact method has been proposed yet. The fault simulation time of analog circuits is complex from the fact that multiple kinds of faults arises in analog circuits like catastrophic faults, which relates to the creation of net list, short or open wires and parametric faults which are major in number relating to change in the value of the components in the circuit.

This work includes:

(i) Design of a static linear behaviour analog fault model for ladder circuits.
(ii) Design of a test procedure, which can estimate all the parameters
(iii) In the parameter set so that the circuit under test can be tested with
(iv) Multiple parametric faults.
(iii) Finding out the component which is responsible for the error.
(iv) Calculating the percentage of the error present in the value of the component.

2. Fault Model

Testing of analog and digital signal circuits has become a challenge and gained more interest in the last decade for many reasons including increasing the applications of the analog circuits, integrating the whole system on one chip, and the high cost of analog testing compared with digital testing counterpart. This measure is called ‘fault coverage ‘and is defined as:

Fault coverage= Number of detected faults/ Total number of faults

When a product is, fabricated designed and tested and it fails the test, then there must be cause for the failure. Either the test was wrong, or the fabrication process was faulty, or the design was incorrect, or the specification had a problem. Anything can go wrong. The role of testing is to detect whether something went wrong and the role of diagnosis is to determine exactly what went wrong, and where the process needs to be altered. Therefore, correctness and effectiveness of testing is most important for quality products. However, electronic tests are not perfect either. They may not cover certain faults and some bad chips will pass.

Many integrated circuits contain fabrication defects upon manufacture. A defect is a physical flaw in the device, i.e. a shorted transistor or an open inter connect. A fault is the logic level manifestation of the Defect, i.e. a line permanently stuck at a low logic level .An error occurs when a fault causes an incorrect logic value at a functional output. A logic gate may generate a wrong output signal because of fault in the circuitry that implements the gate. Dealing with the many different types of faults is cumbersome. Fortunately, it is possible to restrict the testing process to simple faults, and obtain generally satisfactory results. A circuit is said to be faulty if it gives output transfer function out of design specifications. Faults can occur both in analog and digital circuits and based on the fault model, efficient tests can be generated to ensure the quality of the circuits with low test cost. Generally a practical fault model helps to simplify testing problems. A fault model helps to simplify the problem by targeting only Logical Faults.

NEED FOR FAULT MODELS

i. A fault model identifies targets for testing and is essential for a testing methodology
ii Real defects often mechanical too numerous and often not analysable.
iii .A fault model identifies a fault model and targets for testing makes analysis possible.

2.1 CLASSIFICATION OF FAULTS

The diversity of VLSI defects, it is difficult to generate tests for real defects. Fault models are necessary for generating and evaluating a set of test vectors. Generally, a good fault model should satisfy two criteria:

i. It should accurately reflect the behavior of defects, and
ii It should be computationally efficient in terms of and test pattern and generation

Many fault models have been proposed but, unfortunately, no single fault model accurately reflects the behaviour of all possible defects that can occur. As a result, a combination of different fault models is often used in the evaluation and generation of testing approaches and test vectors developed for VLSI devices. When there is only one fault in the circuit, then the total number of possible single faults, referred to as the single-fault model. In reality of course, multiple faults may occur in the circuit. The total number of possible combinations of multiple faults, referred to as the multiple-fault model [3] Coming to classification of faults they are of different types and mainly they are partitioned to

I. Analog Faults II. Digital Faults

Analog faults are generally classified into two catalogs: hard and soft faults[3]. A hard fault is a fault that changes the circuit net list such as a short or an open wire. hard faults result in a dramatic change of the CUT’s transfer function. On the other hand, soft faults represent parameter shifts of the component

3. WAVELET BASED ALGORITHM

A circuit test involves three major steps: signal response measurement, circuit stimulate and analysis of the results. Here, the CUT is stimulated in normal operation by an generated signal, and the *I*PS or *V*OUT signal is measured and stored. A *wavelet* algorithm is performed to stored the *I*PS or *V*OUT signal is to calculate the necessary distance values. The WTis utilized better approximation of a transient signal waveform than the Fourier transform for a fixed limiting

frequency of the measured signal[4]. Moreover, it allows the selection (in terms of minimization of the approximation error) of the appropriate basis function according to the measured signal encountered in the CUT.

For the wavelet based algorithm, the *discrete wavelet* is used. The Wavelet energy divide a discrete signal of length *n* into two sub signals [4]. One sub signal is a trend or average; the other sub signal is a fluctuation or difference. Two energy values are computed, $EF1$and ETi. For the computation of ETi (i = 1, 2 . . .), the trend coefficients Tij (j = 1 . . . n) of the i decomposition

$$E_{Ti} = \sum_{j=i}^{k} E_{ij}^{2} \tag{1}$$

And for $EF1$, the fluctuation or detail coefficients $F1j$ of the first level of decomposition are taken into account

$$E_{f1} = \sum_{j=i}^{k} E_{f1}^{2} \tag{2}$$

3.1 Test Algorithm Utilizing A Discrimination Factor Of Euclidean Distance Metric Function

In this algorithm, the discrimination factor Df test metric is introduced which is actually a normalized Euclidean test metric that depends on the energy values $ET2$and $EF1$ of the WT of the measured waveform (IPS, VOUT).For the wavelet energy computation, the trend coefficients of the second-level decomposition and detail coefficients of the first-level decomposition are considered[5]. The proposed test algorithm A is a two-phase process. At the first phase (*Training Phase*), statistical processing of the fault free circuit data takes place in order to compute the wavelet energy values $ET2,0(z)$ and $EF1,0(z)$ for the reference circuit and the discrimination factor limit Dflim In the second phase(*Main Test Phase*), algorithm phases are described in the following.

Training Phase (steps)

Step 1:each fault-free circuit $i = 1, \ldots, n$
Step 2:Measuring the waveform $z = \{I$PS, VOUT$\}$.
Step 3:Compute the values and store $ET2,0-i(z)$, $EF1,0-i(z)$.

$$E_{T2,0(Z)} = 1/n \sum_{j=i}^{k} E_{T2,0-i(z)} \tag{3}$$

$$E_{f1,0(Z)} = 1/n \sum_{j=i}^{k} E_{f1,0-i(z)} \tag{4}$$

$$Df_{i2,0(Z)} = \sqrt{(E_{T2,0-i(z)} - E_{T2,0(Z)}} / E_{T2,0(Z)})^2 + (E_{f1,0-i(z)} - E_{F1,0(Z)}) / E_{f1,0(z)})^2 \tag{5}$$

The cut-off frequency is 1.4 kHz. It consists of 6 operational amplifiers (opamps), 4 capacitors, and 13 resistors. Each operational amplifier consists of capacitor and nine MOS transistor. All

catastrophic faults on passive components are taken into account, thus giving 51 faulty cases. For each opamp, internal hard faults are also considered: all opens and shorts in MOS transistors [gate open (GOP), drain open (DOP), source open (SOP), gate–drain short (GDS),gate–source short (GSS), and drain–source short (DSS)] and shorts and opens for the internal capacitor *C*1.

Each one of the *I*PS and *V*OUT signal waveforms and the tolerance limit *Df*lim0 (*z*)(for the test algorithm A with the *discrimination factor* metric)or *MD*lim0 (*z*) (for the test algorithm B with the Mahalanobis distance metric) are computed from the fault-free circuits

4. SIMULATED RESULTS

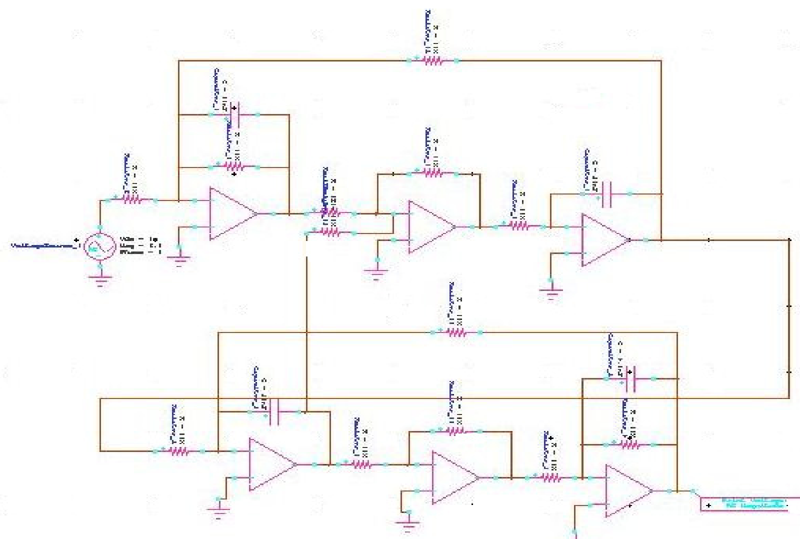

Fig 4 leaf frog filter circuit

In this circuit it can design the leaf frog filter it consists of operational amplifier resistor and capacitor it is to find out the faults of this circuits and to calculate the errors

4.1 INNER CIRCUIT DIAGRAM OF OPERATIONAL AMPLIFIER

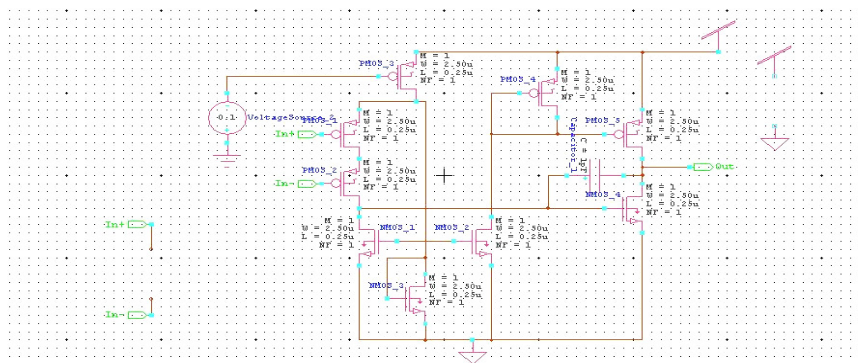

Fig 4.1 op-amp circuit of leaf frog circuit

In this op-amp circuits it consists of nmos and pmos transistor it is a internal circuit of leaf frog filter .it can be useful in to finding the faults in hardware and software faults it can estimate In which component the error has been detected to resolve the values and compare the previous values that values is to compare to existing values .in hard faults it can easily determine the

Values but soft faults it has some losses present in the circuit that has been detected

4.3 FREQUENCY RESPONSE OF FAULT FREE CIRCUIT

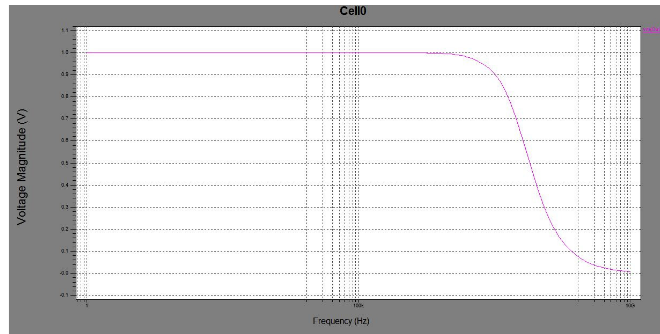

Fig 4.2 fault free of leaf frog circuit

4.4 OP AMP FAULT

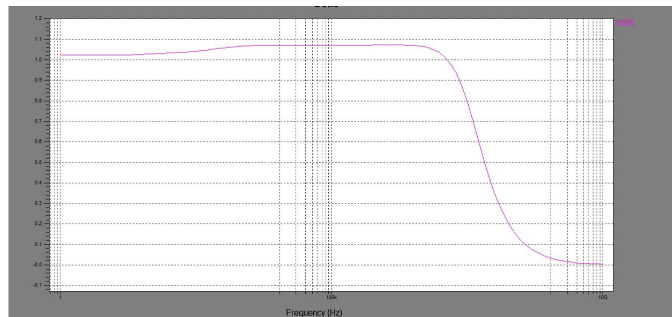

Fig 4.3soure open of leaf frog circuit

4.5 RESISTOR R4 FAULT

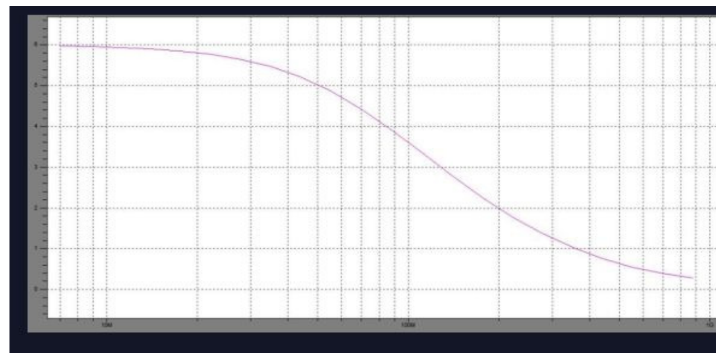

Fig 4.4 resistor r4 circuit of leaf frog circuit

4.6 BRIDGING RESISTANCE

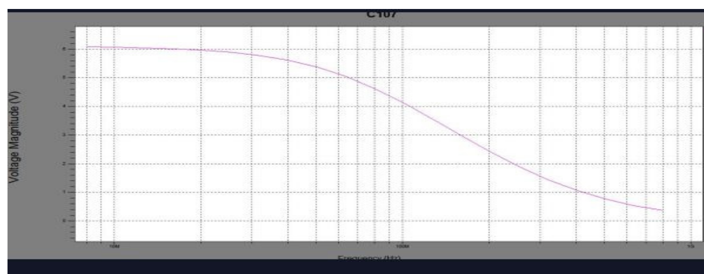

Fig 4.5 bridging resistance of leaf frog circuits

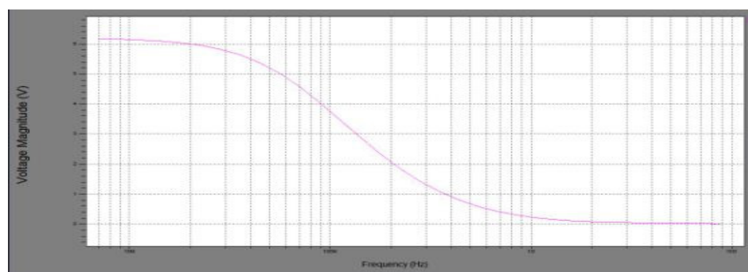

Fig 4.6 capacitor c4 leaf frog circuit

4.7 TABULAR FORM OF LEAF FROG CIRCUIT

Table 1 .distance measurement and eigen valuesof leaf frog circuit

	$Df_{(vout)}$	$Md_{(vout)}$	**Eigen value**				
			V_{maxi}	V_{min}	K_{min}, ,K_{maxi}	B_{min}, B_{maxi}	Error values
Fault free circuits	1.35	1.35	18.4649	-0.433	24.245, -5.846	24.7479, -23.687	0.222
gate open	**1.3272**	**2.56**	20.122	-0.33	24.345, -5.762	24.647, -23.58	0.233
Resistor r5	0.0715	**2.75**	16.6149	-0.33	24.101, -5.456	24.54, -23.45	0.56
Capacitor fault c3	1.285	0.915	19.8140	-0.077	41.673 2, -27.988	21.228, -20.168	0.56
Drain open	1..88	**1.157**	2.621	-0.413	41.345, -27.45	21.28, -20.145	0.98
Bridging resistance	0.5039	**0.265**	19.044	-0.07	41.256, -27.045	21.023, -20.145	0.69

It ensures that the matrix Eigen values varies with the change of matrix elements. In this way the Eigen values of matrix *A[6]* and the elements of the parametric fault set of CUT can be put one-to-one correspondence. So the proposed method is available to implement the faults diagnosis for analog circuits[7]. The algebraic theory guarantees the correctness of this approach.

The tolerance limits for the fault-free(reference) circuit are also given in Table I. It is observed that, according to steps of the Main Test Phase in the *Opamp1_M1-GOP* (gate-open fault at M1 internal toopamp1) fault is not detectable using the *V*OUT [*Dfk*(*V*OUT) 1.32 < 1.35 = *Df*lim0 (*V*OUT) and *MDT*1,*k*(*V*OUT) =1.32 < 2.56 = *MD*lim *T*1,0(*V*OUT)]

When the *V*OUT signal is utilized, the fault detect ability percentage is 70.99% for the test algorithm B and 70.74%for the test algorithm A. The fault delectability percentage for the test algorithm B (70.99%) is attributed to the energy values from the trend coefficients (70.99% for "MDT1"), whereas the information from the detail coefficients results in lower fault detection percentage (64.41% for "MDF1")

5. CONCLUSION

All the analysis was made on low pass leap frog using tanner tools. The required coefficients were successfully calculated and compared with that of the given in the base paper we have got a variation of about 1-2 percent in the final values and we have extended this method to two other components apart from what are mentioned in the paper .Finally, we are successful in finding out the faulty component and also the variation in the faulty component value from its nominal values

REFERENCES

[1] A. Singh, J. Plusquellic, D. Phatak, and C. Patel, "Defect simulation methodology for i(DDT) testing," J. Electron. Test. Theory Appl., vol. 22,no. 3, pp. 255–272, Jun. 2006.

[2] Plusquellic, A. Singh, C. Patel, and A. Gattiker, "Power supply Transient signal Analysis for defect-oriented test," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 22, no. 3, pp. 370–374,Mar. 2003.

[3] F. Liu, P. K. Nikolov, and S. Ozev, "Parametric fault diagnosis for analog Circuits using a Bayesian framework," in Proc. 24th IEEE VTS, Berkeley, A, Apr. 30–May 4, 2006, pp. 272–277

[4] S. Bhunia and K. Roy, "A novel wavelet transform-based transient current Analysis for fault detection and localization," IEEE Trans.Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 4, pp. 503–507,Apr. 2005

[5] M. G. Dimopoulos, A. D. Spyronasios, D. K. Papakostas, and A. A. Hatzopoulos, "Wavelet energy-based testing using supply current measurements," IET Sci.,Meas. Technol., vol. 4, no. 2, pp. 76–85,Mar. 2010.

[6] G. W Stewart and J. G. Sun, Matrix Perturbation Theory. Boston, MA,USA: Academic, 1990, pp. 166–167.

[7] J. H. Wilkinson, The Algebraic Eigen value Problem. Oxford, U.K.:Clarendon, 1988, pp. 62–64.

,