AN OPTIMIZED DEVICE SIZING OF TWO-STAGE CMOS OP-AMP USING MULTI-OBJECTIVE GENETIC ALGORITHM

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ABSTRACT

A novel approach for optimizing the transistor dimensions of two stage CMOS op-amp using Multi-Objective Genetic Algorithm (MOGA) is presented. The proposed approach is used to find the optimal dimensions of each transistor to improve op-amp performances for analog and mixed signal integrated circuit design. The aim is to automatically determine the device sizes to meet the given performance specifications while minimizing the cost function such as power dissipation and a weighted sum of the active area. This strongly suggests that the approach is capable of determining the globally optimal solutions to the problem. Exactness of performance prediction in the device sizing program (implemented in MATLAB) maintained. Here Six parameters are considered i.e., open loop gain, Phase Margin (PM), Area (A), Bandwidth of unity Gain (UGB), Power Consumption (P) and Slew Rate (SR). The circuit is simulated in cadence(Virtuoso Spectre) 0.18um CMOS technology.

KEYWORDS

Analog Design, complementary metal-oxide-semiconductor (CMOS), Optimization, Two-Stage Operational Amplifier, Multi-objective Genetic Algorithm (MOGA).

1. INTRODUCTION

The semiconductor industry is driven by the scaling of CMOS technology to improve the speed, performance and reduce the cost [1].the demand for mixed mode integrated circuits increases, the design of analog circuits such as operational amplifiers (op-amps) in CMOS technology becomes more critical [2]. The design process involves the two major steps, the first is the selection of the topology, and optimization of topology by obtaining the optimal dimensions of the transistors, by proposing suitable architecture to meet the given specifications and to do the hand calculations, Second step is to take the design, verify and optimize it. The hand calculations may take more design time as well as leads to mistakes but an automated optimization can save enormous design time. A new methodology is proposed to determine the transistor dimensions (i.e., Width and Length) for CMOS two-stage op-amps. This paper is planned into four sections. In section -II is

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about the Operational Amplifiers. In section-III and section-IV the Optimization Methodology and Result and Discussions are discussed. In section-V gives the conclusion of the paper.

2. OPERATIONAL AMPLIFIER

In this section, operational amplifier (op amp) design is discussed. Op-amp is used for several operations such as amplifying the signals, addition or subtraction, signal generators, and filters. In order to achieve these it must have high gain, high input resistance and it should function over a wide range of frequencies. Such op-amp can also be used in A/D converters, D/A converters, filters and sensing circuits.

2.1 Two-stage operational amplifier

This CMOS operational amplifier has four major blocks, first one is bias circuits (current mirror) is to establish the operating points of transistor in its saturation region, an input differential amplifier which provides a differential voltage or differential current as an output, improves the noise and offset performances. A compensation circuit for compensating the poles and to stabilize the circuit for example miller compensation. The second Gain circuit block is configured as a common-source amplifier to allow maximum output swings.

In this paper, for the two-stage operational amplifier, design parameters are considered. such as open loop DC gain, unity gain bandwidth (UGB), phase margin (PM), power consumption (Pc), area (A) and slew-rate (SR).



Fig.1 Two stage op-amp

2.1.1 Open loop DC Gain

$$A_{V} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} \cdot \frac{g_{m6}}{g_{ds7} + g_{ds6}}$$

2.1.2 UGB

The UGB is given as

$$GBW = \frac{g_{m1}}{C_c}$$

Where C_c is compensation capacitor

2.1.3 Phase Margin

The phase margin is given by the equation

PM=180-tan⁻¹(gain banwidth/pole1)- tan⁻¹(gain banwidth/pole2)- tan⁻¹(gain banwidth/zero)

2.1.4 Slew Rate

$$SR = \frac{I_5}{C_c}$$

2.1.5 Power Consumption

$$P = (V_{DD} - V_{ss})(I_5 + 2I_7)$$

3. OPTIMIZATION METHODLOGY

The op-amp design optimization employs genetic algorithms (GA's). Genetic Algorithm (GA) is concurrent evolution approach for optimization of transistor parameters, which follows the evolution of the living beings, In general The evolutionary algorithms uses three main principles: reproduction, selection and diversity of the species similar to natural evolution. Usually starts from and is an iterative process. The new generation solutions is then used in the next iteration of the algorithm then mutation, crossover operations are performed, until the satisfactory fitness level is reached for the population. After reaching the total number of generations the process is terminated. Optimal dimensions are represented as

[W1,L1,W3,L3,W5,L5,W6,L6,W7,L7,W8,L8].

The above process can be explained by using the flow chart shown in the Fig.2 below.



Fig.2 Genetic algorithm flowchart.



Fig.3 Op-amp design flow

4. SIMULATION AND DISCUSSION

The simulation results of an operational amplifier is measured in terms of open loop DC gain, unity gain bandwidth, phase margin(PM), slew rate(SR) and area(A). The optimization process involves the crossover, mutation, selection operations which are performed on each variable to improve the fitness score. This process will be iterated until the satisfactory fitness level is reached, if the total number of generations is generated then the process is terminated. Here the optimization method is implemented using MATLAB. The results of two-stage operational amplifier are the open loop DC gain is 85.14dB,unity gain bandwidth(UGB) is 66.5MHz,phase margin(PM) is 54^0 and slew rate(SR) is $50V/\mu$ s.



Fig.4 Schematic of 2 stage Op - amp

				0	1.4					
() 				Operational Amplifier			Specifications			
5							VDD	1.8 V	VSS	-1.8 V
1	·	72 .72		Design	Figure		S.R	50 V/us	UGB	50 MHZ
			P.c	She	w		P.M	>60 DEG	GAIN	86 DB
			, [Inp	outs		Max CMR	1 V	Min CMR	-1.5 V
				Enter	Inputs		Kn	0.000345306	Кр	5.43857e-005
					OUTPUT	'S				
PARAMETERS	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10
THOF	Р	р	N	N	Р	N	Р	Р	Р	Р
ITPE					h					
I(uA)	2.5e-006	2.5e-006	2.5e-006	2.5e-006	5e-006	4.39449e-005	4.39449e-005	3e-005	3e-005	3e-005
I(uA) W/L	2.5e-006 3.62581	2.5e-006 3.62581	2.5e-006 0.160888	2.5e-006 0.160888	5e-006 12.7689	4.39449e-005 2.82808	4.39449e-005 112.225	3e-005 136.201	3e-005 76.6133	3e-005 76.6133
I(uA) W/L	2.5e-006 3.62581 7.42645e-007	2.5e-006 3.62581 7.42645e-007	2.5e-006 0.160888 1.1896e-007	2.5e-006 0.160888 1.1896e-007	5e-006 12.7689 2.3884e-006	4.39449e-005 2.82808 5.99055e-007	4.39449e-005 112.225 2.02906e-005	3e-005 136.201 2.46063e-005	3e-005 76.6133 1.38804e-005	3e-005 76.6133 1.38804e-005

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Fig.5 output window with W/L values of the 2 stage op-amp

Table I:	optimized	parameters	of 2	stage	op-amp
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Transistor	W/L
M1	0.74u/0.18u
M2	0.74u/0.18u
M3	1u/0.18u
M4	1u/0.18u
M5	2.3u/0.18u
M6	0.59u/0.18u
M7	3.27u/0.18u
M8	24.6u/0.18u
M9	13.88u/0.18u
M10	13.88u/0.18u



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Fig.6 AC response for the 2 stage Op-amp



Fig.7 Phase response for the 2 stage Op-amp



Fig.8 positive slew rate



Fig.9 negative slew rate

Table II: The Optimized performance of 2-stage Op-Amp

Performance	Specifications	Simulation Results	
DC gain (in dB)	≥85	85.14	
Unity Gain	>50	66.5	
Bandwidth(in MHz)			
Phase Margin(in deg)	60	54	
Slew Rate(V/us)	50	48	
Area(m ²)	Min	550	
Power(uW)	Min	47	

3. CONCLUSION

In this paper, a multi objective optimization algorithm for mixed signal circuit design is implemented using Matlab. Circuit equations and genetic algorithm is combined and produced the tool in order to determine the optimal dimensions of a two-stage op-amp. The results balance the desired and obtained specifications this shows the efficient approach in the analog design where the design time is reduced in the proposed approach. It can be concluded that the proposed multi-objective genetic algorithm based approach is efficient and gives optimized results for circuits design and reduce the design time.

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