DESIGN VERIFICATION AND TEST VECTOR MINIMIZATION USING HEURISTIC METHOD OF A RIPPLE CARRY ADDER

K.L.V.Ramana Kumari [1] , M.Asha Rani [2]and N. Balaji [3]

[1]Department of ECE, VNRVJIET, Hyderabad, India
[2]Department of ECE, JNTUH, Hyderabad, India
[3]Department of ECE, JNTUK, Vizianagaram, India

ABSTRACT

The reduction in feature size increases the probability of manufacturing defect in the IC will result in a faulty chip. A very small defect can easily result in a faulty transistor or interconnecting wire when the feature size is less. Testing is required to guarantee fault-free products, regardless of whether the product is a VLSI device or an electronic system. Simulation is used to verify the correctness of the design. To test n input circuit we required 2^n test vectors. As the number inputs of a circuit are more, the exponential growth of the required number of vectors takes much time to test the circuit. It is necessary to find testing methods to reduce test vectors . So here designed an heuristic approach to test the ripple carry adder. Modelsim and Xilinx tools are used to verify and synthesize the design.

KEYWORDS

Ripple carry Adder, Test vectors, Modelsim Simulator

1. INTRODUCTION

The complexity of VLSI technology has reached the point where we are trying to put 100 million transistors on a single chip, and we are trying to increase the on-chip clock frequency to 1 *GHz.* Transistor feature sizes on a VLSI chip reduce roughly by 10.5% per year, resulting in a transistor density increase of roughly 22.1% every year. An almost equal amount of increase is provided by wafer and chip size increases and circuit design and process innovations. This is evident that, 44% increase in transistors on microprocessor chips every year. This amounts to little over doubling every two years[3]. The doubling of transistors on an integrated circuit every 18 to 24 months has been known as Moore's since the mid-1970s. Although many have predicted its end, it continues to hold, which leads to several results [1].

The reduction in feature size increases the probability that a manufacturing defect in the IC will result in a faulty chip[2]. A very small defect can easily result in a faulty transistor or interconnecting wire when the feature size is less than 100 nm. Furthermore, it takes only one faulty transistor or wire to make the entire chip fail to function properly or at the required operating frequency. Defects created during the manufacturing process are unavoidable, and, as a result, some number of ICs is expected to be faulty therefore, testing is required to guarantee fault free products, regardless of whether the product is a VLSI device or an electronic system

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composed of many VLSI devices. It is also necessary to test components at various stages during the manufacturing process. For example, in order to produce an electronic system, we must produce ICs, use these ICs to assemble printed circuit boards (PCBs), and then use the PCBs to assemble the system. There is general agreement with the rule of ten, which says that the cost of detecting a faulty IC increases by an order of magnitude as we move through each stage of manufacturing, from device level to board level to system level and finally to system operation in the field. Electronic testing includes IC testing, PCB testing, and system testing at the various manufacturing stages and, in some cases, during system operation. Testing is used not only to find the fault-free devices, PCBs, and systems but also to improve production yield at the various stages of manufacturing by analyzing the cause of defects when faults are encountered. In some systems, periodic testing is performed to ensure fault-free system operation and to initiate repair procedures when faults are detected. Hence, VLSI testing is important to designers, product engineers, test engineers, managers, manufacturers, and end-users [1].

Fig. 1 explains the basic principle of digital testing. Binary patterns (or *test vectors*) are applied to the inputs of the circuit. The response of the circuit is compared with the expected response [4, 5]. The circuit is considered good if the responses match. Otherwise the circuit is faulty. Obviously, the quality of the tested circuit will depend upon the thoroughness of the test vectors. Generation and evaluation of test vectors is one of the main objectives of this paper. VLSI chip testing is an important part of the manufacturing process.

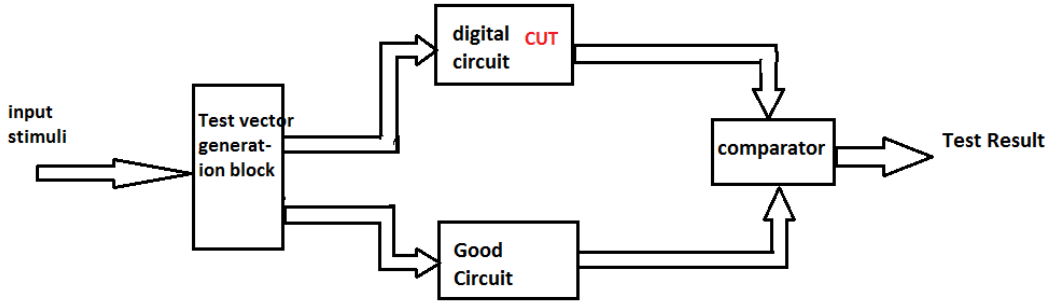

Fig.1. Principle of Testing

2. PROPOSED SYSTEM

Simulation serves two distinct purposes in electronic design. First, it is used to verify the correctness of the design and second, it verifies the tests. The simulation process is illustrated in Figure 2. The process of realizing an electronic system begins with its specification, which describes the input or output electrical behaviour (logical, analog, and timing) and other characteristics (physical, environmental, etc.)

The specification is the starting point for the design activity. The process of synthesis produces an interconnection of components called a net list. The design is verified by a true-value simulator. True-value means that the simulator will compute the response for given input stimuli without injecting any faults in the design. The input stimuli are also based on the specification.

Typically, these stimuli correspond to those input and output specifications that are either critical or considered risky by the synthesis procedures. A frequently used strategy is to exercise all functions with only critical data patterns. This is because the simulation of the exhaustive set of

data patterns can be too expensive. However, the definition of "critical" often depends on designer's heuristics.

The true-value simulator in Figure 2. Computes the responses that a circuit would have produced if the given input stimuli were applied. In a typical design verification scenario, the computed responses are analyzed (either automatically, or interactively, or manually) to verify that the designed net list performs according to the specification. If errors are found, suitable changes are made, until responses to all stimuli match the specification.

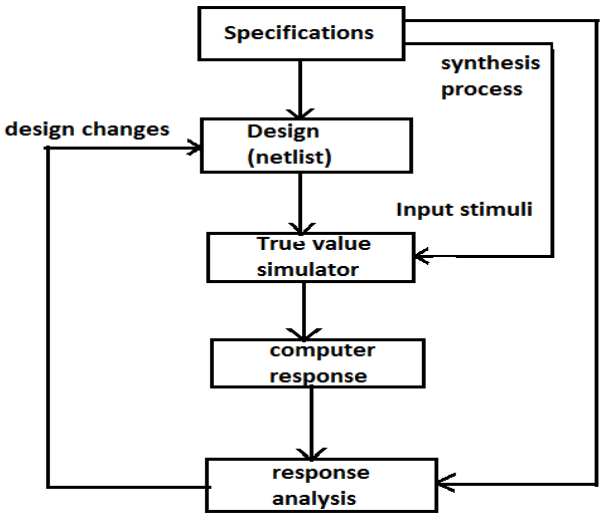

Fig. 2. Block diagram for Design Verification

2.1. Test vector Minimization method

A combinational logic circuit is designed to add two 4-bit binary numbers. This circuit has 9 binary inputs and 5 outputs. To verify the circuit the number inputs required to the circuit is 2^n ie., 512, to completely verify the correctness of the implemented logic, we must simulate input vectors and check that each produces the correct sum output.

This is clearly impractical. So, the designer must simulate some selected vectors. For example, one may add pairs of integers where both are non-zero, one is zero, and both are zero shown in Fig. 3. Then add a large number of randomly generated integer pairs. Such heuristic, though they seem arbitrary, can effectively find many possible errors in the designed logic. The next example illustrates a rather simple heuristic.

FA0			FA1			FA2			FA3			Cout
C_0	A_0	B_0	C_1	A_1	B_1	C_2	A_2	B_2	C_3	A_3	B_3	C_4
0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	1	0	0	1	0	0	1	0
0	1	0	0	1	0	0	1	0	0	1	0	0
0	1	1	1	0	0	0	1	1	1	0	0	0
1	0	0	0	1	1	1	0	0	0	1	1	1
1	0	1	1	0	1	1	0	1	1	0	1	1
1	1	0	1	1	0	1	1	0	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1

VECTOR NO.	BIT : $C_0 A_0 B_0 A_1 B_1 A_2 B_2 A_3 B_3$	Input $C_n A_n B_n$ to FAn
1	000000000	000 applied to all FAs
2	001010101	001 applied to all FAs
3	010101010	010 applied to all FAs
4	011001100	011 applied to FA0,FA2 & 100 applied to Fa1,FA3
5	100110011	100 applied to FA0,FA2 & 011 applied to FA1,Fa3
6	101010101	101 applied to all FAs
7	110101010	110 applied to all FAs
8	111111111	111 applied to all FAs

Fig.3. Binary values applied to the FA's

Design verification heuristic for a ripple-carry adder: Fig. 4. shows the logic design of an adder circuit. The basic building block in this design is a full-adder that adds two data bits, and one carry bit, to produce sum and carry outputs, and respectively. For logic verification, one possible strategy is to select a set of vectors that will apply all possible inputs to each full adder block. For example, if we set and apply all four combinations shown in Fig.3.

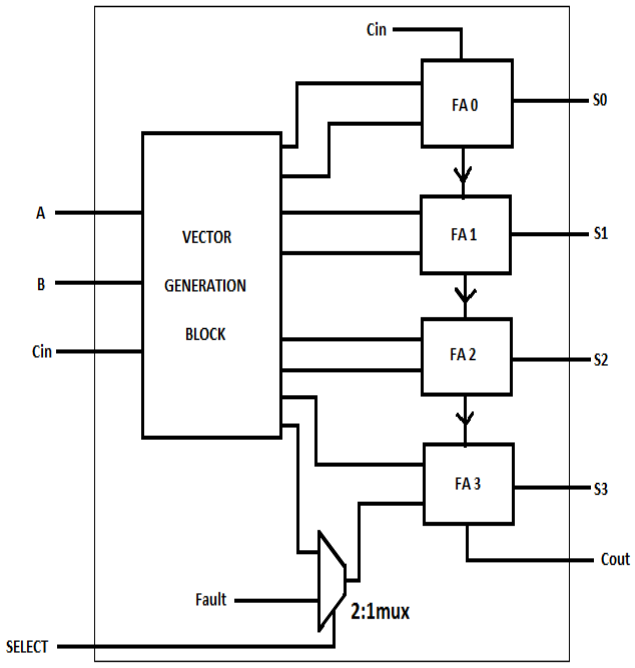

Fig.4. Heuristic method for test minimization

Test vectors are generated from the logic block. Inject the SA1 or SA0 to one input to the full adder through 2:1 Multiplexer. If the multiplexer input is 0, true bit will be selected and multiplexer input is 1, faulty input is selected at the input of the full adder. Associated carry will

be generated at the full adder and fault free and faulty outputs are compared. If the output is different fault will be detected. Depending on the input, carry will be propagated, that effects the next adder circuit also. 8 test vectors are sufficient to test the circuit. One significant advantage of simulation is that all internal signals of the circuit can be examined. This reduces the complexity of verification. The regular pattern in each vector allows us to expand the width of the vector without increasing the number of vectors to an adder of arbitrarily large size.

3. RESULTS AND DISCUSSIONS

SA1 fault is injected to the 3rd full adder of a circuit, Fault free output and faulty outputs are observed, if the two are different fault is identified and marked in the diagrams shown in Fig. 5. and Fig.6.

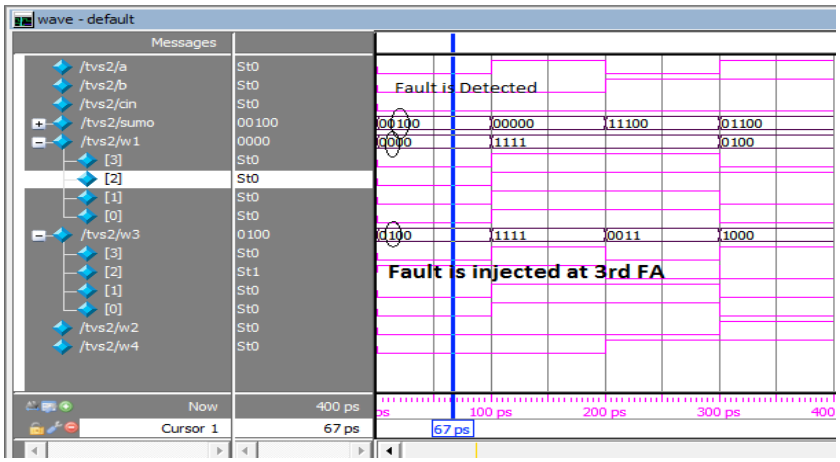

Fig. 5. Fault is detected at the output of the full adder.

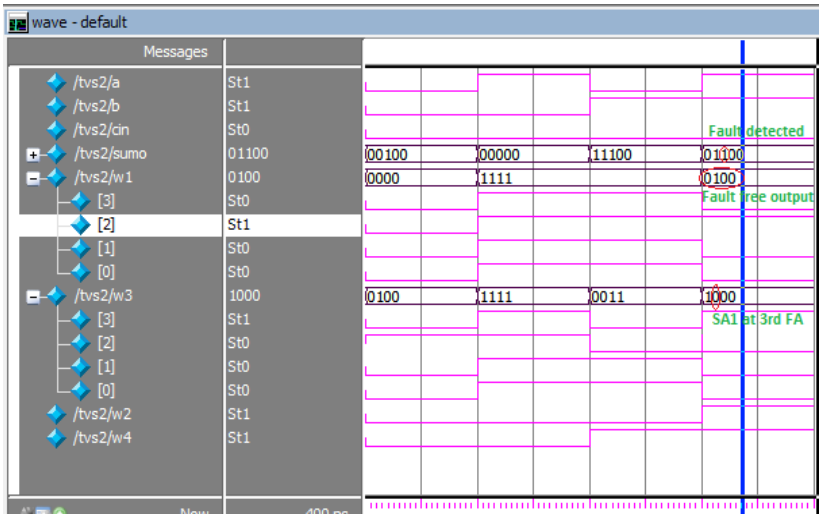

Fig.6. Fault is detected at the output of the full adder.

Output is analyzed at the output of the full adder, that fault is propagated to next full adder, with final carryout 0.

3.1. Register Transistor level diagram generated by tool shown in Fig.7.

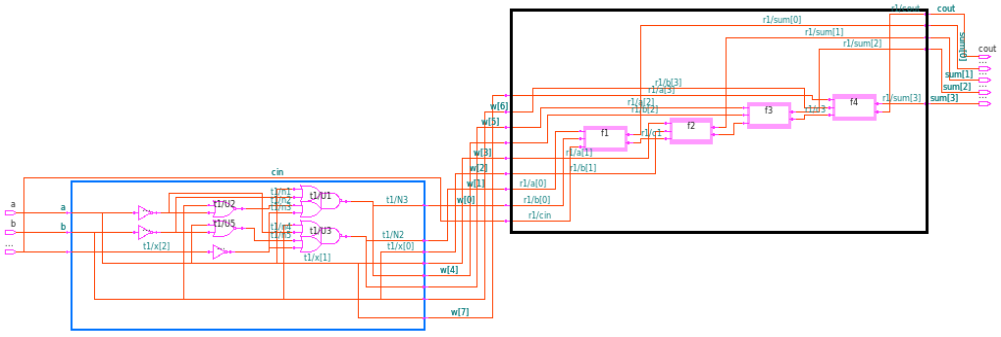

Fig.**7.** Register transistor level diagram of a Ripple Carry Adder

Dynamic power, Leakage power, Switching power given by the tool is shown in the report.

```
    Capacitance Units = 0.100000ff
    Time Units = 1ns
    Dynamic Power Units = 100nW    (derived from V,C,T units)
    Leakage Power Units = Unitless


  Cell Internal Power  =   0.0000 nW    (0%)
  Net Switching Power  =   9.4924 uW  (100%)
                         ---------
Total Dynamic Power    =   9.4924 uW  (100%)

Cell Leakage Power     =   0.0000

Error: Either dynamic power or leakage power, in the library, is unitless. Unable to display complete power group summary.
Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000             NA    (     N/A)
memory             0.0000           0.0000              0.0000             NA    (     N/A)
black_box          0.0000           0.0000              0.0000             NA    (     N/A)
clock_network      0.0000           0.0000              0.0000             NA    (     N/A)
register           0.0000           0.0000              0.0000             NA    (     N/A)
sequential         0.0000           0.0000              0.0000             NA    (     N/A)
combinational      0.0000        9.4924e+03             0.0000             NA    (     N/A)
--------------------------------------------------------------------------------------------------
Total              0.0000 nW     9.4924e+03 nW          0.0000             NA

***** End Of Report *****
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Dynamic power, Leakage power, Switching power Report.

4. CONCLUSIONS

Test vector minimization method is designed in this paper. A heuristic method is used to reduce the test vectors of a ripple carry adder. Testing operation of the ripple carry adder is performed. This method reduces the number of test vectors to detect the faults. The regular pattern allows us to expand the width of the vector without increasing the number of vectors to an adder of arbitrary large size. Design compiler, Modelsim and Xilinx tools are used to analyze the method.

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