DESIGN OF PROCESSING ELEMENT (PE3) FOR IMPLEMENTING PIPELINE FFT PROCESSOR

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ABSTRACT

Multiplexing is a method by which multiple analog message signals or digital data streams are combined into one signal over a shared medium. In communication, different multiplexing schemes are used. To achieve higher data rates, Orthogonal Frequency Division Multiplexing (OFDM) is used due to its high spectral efficiency. OFDM became a serious alternative for modern digital signal processing methods based on the Fast Fourier Transform (FFT).The problems with Orthogonal subcarriers can be addressed with FFT in communication applications. An 8-bit processing element (PE3), used in the execution of a pipeline FFT processoris designed and presented in this paper. Simulations are carried out using Mentor Graphics tools in 130nm technology.

***KEYWORDS*:**

Multiplexing, OFDM, FFT processor, Mentor Graphics tools.

1. INTRODUCTION

InDiscrete Signal Processing and telecommunications, Discrete Fourier Transform (DFT) is essential. Cooley and Tukey [1] proposed FFT to overcome the intensive computation, which has applications involving OFDM, such as WiMAX, LTE, DSL, DAB/DVB systems, and efficiently reduced the time complexity from $O(N^2)$ to O (Nlog 2N), where N denotes the FFT size. Different FFT processors developed for hardware implementation are classified as memory based and pipeline based architectures [2-4]. Memory-based architecture (single Processing Element (PE) approach), consists of a principal Processing Element and multiple memory units resulting in reduced power consumption and less hardware than the pipeline architecture, but have disadvantages like low throughput, long latency, and cannot be parallelized. Besides, the pipeline architecture can overcome the disadvantages of the memory based architecture style, with an acceptable hardware overhead.

Single-path Delay Feedback (SDF)pipeline and Multiple-path Delay Commutator (MDC) pipeline architectures are the two widely used design styles in pipeline FFT processors. SDF pipeline FFT [2-5] requires less memory, easy to design, utilizes less than 50% of the multiplication computation, and its control unit is used in portable devices In view of the advantages, the Radix-2 SDF pipeline architecture is considered in implementing the FFT

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processor. Three processing elements are used in the architecture of the proposed design of FFT processor [1]. In this paper, design of 8-bit processing element (PE3) is implemented.

2.FFT ALGORITHM

The DFT X_k of an N-point discrete-time signal x_n is defined by:

$$X_k = \sum_{n=0}^{N-1} x_n W_N^{nk}, \qquad ,0 \le k \le N-1 \tag{1}$$

where $W_N^{nk} = e^{-j2\pi nk/N}$ is twiddle factor.

The direct implementation of DFT is difficult to realize due to the requirement of more hardware. Therefore, to reduce its hardware cost and speed up the computation time, FFT was developed. By using Decimation-in-Time (DIT) or decomposition or Decimation-in-Frequency (DIF), FFT analyzes an input signal sequence to construct a Signal-Flow Graph (SFG) that can be computed efficiently. DIF decomposition is employed as it meets the operation of SDF pipeline architecture. A radix-2 DIF FFT SFG for N=8 is presented in Figure1.

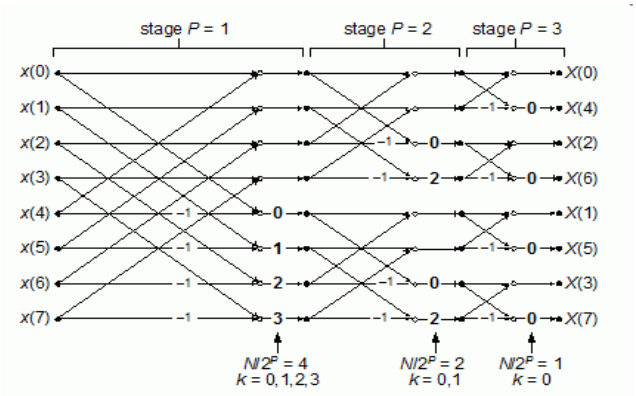

Figure1. Radix-2 Decimation-In-Frequency Fast Fourier Transform Signal Flow Graph for N=8.

To perform FFT computing, complex multiplication scheme [6-11] is used, as a result hardware cost is increased due to the use of ROM and complex multipliers.

DIF FFT is suitable for hardware implementation as it has a regular SFG and requires less complex multipliers resulting in smaller area of the chip. For example, an input signal multiplied by W^1_8 in Figure. 1 can be expressed as:

$$(x + jy)W_8^1 = \sqrt{2}[(x + y) + j(x - y)]/2, \tag{2}$$

Where $(x+ jy)$ denotes a complex discrete-time signal.

Similarly, the complex multiplication of W^3_8 is given by

$$(x+jy)W_8^3 = \sqrt{2}[(x-y)-j(x+y)]/2 \tag{3}$$

Both the equations (2) and (3) will ease hardware implementation.
From symmetric property of the twiddle factors, the complex multiplications can be one of the following three operation types:

$$\text{Type 1: } W_N^k(x+jy) = W_N^{k-(N/4)}(y-jx) \qquad \frac{N}{4} < k < \frac{N}{2} \tag{4}$$

$$\text{Type 2: } W_N^k(x+jy) = -W_N^{k-(N/2)}(x+jy) \qquad \frac{N}{2} < k < \frac{3N}{4} \tag{5}$$

$$\text{Type 3: } W_N^k(x+jy) = -W_N^{k-\left(3N/4\right)}(y-jx) \qquad \frac{3N}{4} < k < N \tag{6}$$

Any twiddle factor can be obtained by combining the twiddle-factor primary elements (equations (4-6)). The three operation types are used to find the twiddle factor required to reduce the size of the ROM. Additional operation types are given below:

$$\text{Type 4: } W_N^k(x+jy) = \left[W_N^{(N/4)-k}(y+jx)\right]^* \qquad 1 \le k < \frac{N}{4} \tag{7}$$

$$\text{Type 5: } W_N^k(x+jy) = -j\left[W_N^{(N/2)-k}(y+jx)\right]^* \qquad \frac{N}{4} < k < \frac{N}{2} \tag{8}$$

Where * indicates conjugate value. A significant shrinkage of twiddle- factor ROM table can be obtained, after the third butterfly stage as the complex multiplications will be reduced by using the five operation types.

3.ARCHITECTURE OF FFT:

A radix-2 8point pipeline FFT processor is presented in Figure 2.The architecture of the pipeline FFT processor contains three processing elements namely,PE3, PE2 and PE1, a complex constant multiplier and delay-line buffers. To remove the twiddle-factor ROM, a reconfigurable complex constant multiplier is used which reduces chip area required and power consumption of FFT processor.

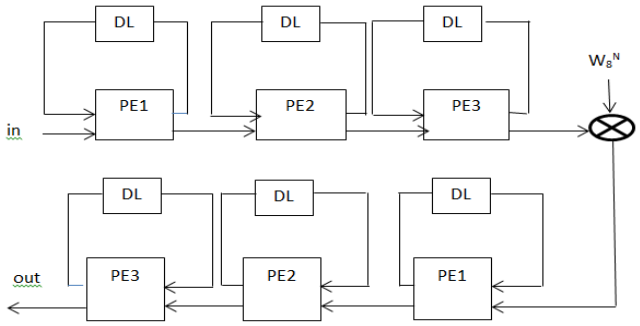

Figure 2. Radix-2 8 point pipeline FFT processor.

PROCESSING ELEMENTS

The three processing elements PE1, PE2, and PE3 of the radix-2 pipeline FFT processor are presented in Figures.3 to 5, respectively. The Processing Elements processes each stage of the butterfly presented in Figure.1. PE3 stage implements a simple radix-2 butterfly, and functions as the sub module for PE2 and PE1 stages.

In Figure 3, Iinand Iout denote the real parts, and Qin and Qoutare the imaginary parts of the input and output data, respectively. Similarly, DL_Iinand DL_Iout stand for the real parts and DL_Qinand DL_Qoutare for the imaginary parts of input and output of the DL buffers, respectively. The multiplication by *–j* or 1 is required for PE2 stage. By taking 2's complement of the input value, multiplication by -1 in Figure.4 can be done practically.

Compared to PE2 stage, calculations in PE1 stage are more complex, as it computes the multiplications by –j, $W_N^{N/8}$ and $W_N^{3N/8}$ respectively. Since $W_N^{N/8}$ =- $W_N^{3N/8}$either the multiplication by $W_N^{N/8}$followed by multiplication with *–j* or the reverse of the previous calculation can be done. The cascaded calculations along with multiplexers are used in PE1 stage calculations and forms a low -cost hardware by saving a bit-parallel $W_N^{3N/8}$ multiplier for computing

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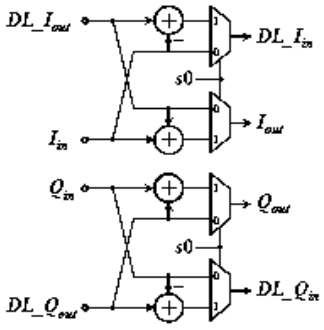

Figure 3. Architecture of PE3

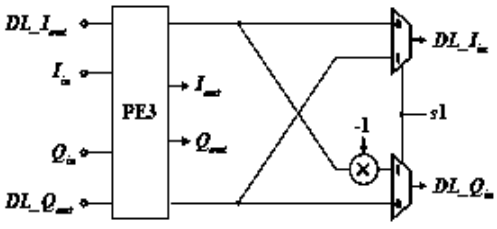

Figure 4. Architecture of PE2

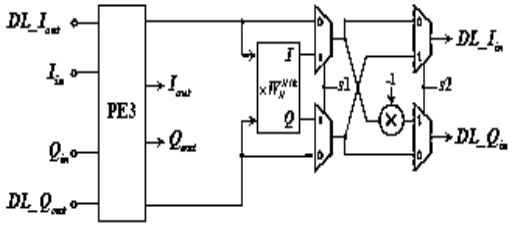

Figure 5.Architecture of PE1.

4. PROCESSING ELEMENT(PE3)

PE3 is the main component in FFT processor as it serves as the sub module for PE2 and PE1 stages. It processes the stage P=3 of the radix-2 8 point DIF FFT butterfly structure in Figure1. Hardware implementation of PE3 employs a ten transistor adder and a multiplexer.1-bit and 8-bit PE3 elements are presented in Figure. 6 and 7 respectively.

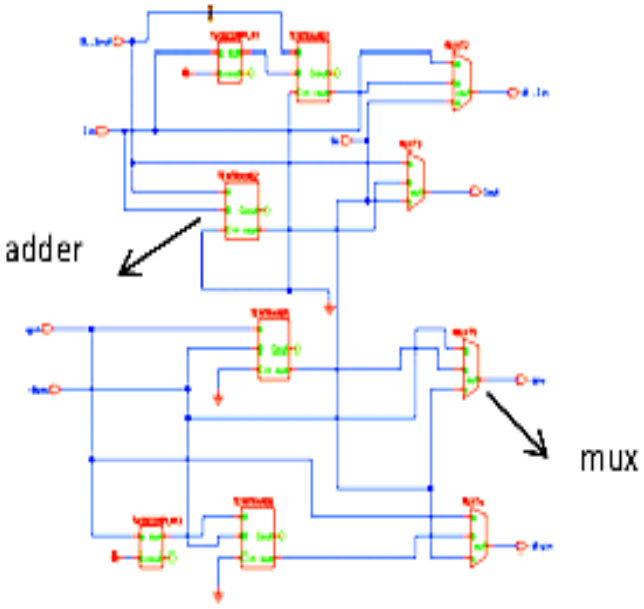

Figure 6.Schematic of 1-bit PE3.

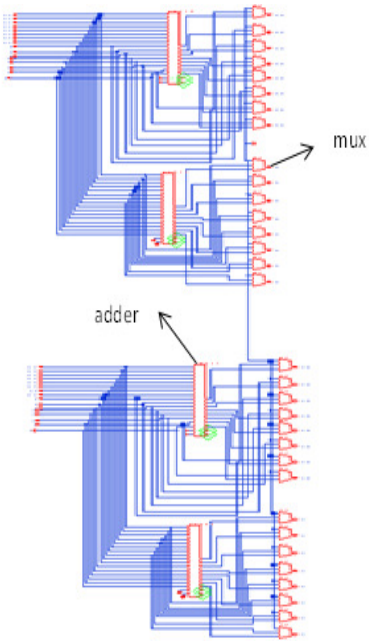

Figure 7.Schematic of 8-bit PE3.

5. RESULTS

PE3 element is simulated with ELDO software in Mentor Graphics. The simulated waveforms of 1-bit and 8-bit PE3 are shown in figure 8 and figure 9-10 respectively.

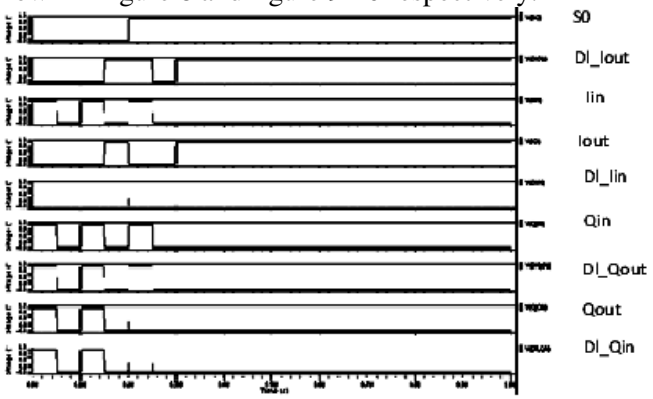

Figure 8. 1-bit PE3 simulated waveforms.

PE3 element processes the stage P=3 of theradix-2 DIF-FFT . It takes Input data (Iin) and Delay Output(DL_Iout) as the inputs and gives the Output data(Iout) and Input Delay to the next buffer(DL_Iin) based on the selection line of the multiplexer.

When S_0=0 DL_Iin = Iin (9)

Iout = DL_Iout (10)

S_0=1 DL_Iin = DL_Iout – Iin (11)

Iout = = DL_Iout + Iin. (12)

From Figure 8,

When So=0, Inputs are Iin= 1010 ; Dl_Iout=0001 then outputs are Dl_Iin=1010 ; Iout = 0001

When So=1, Inputs are Iin=1000 ; Dl_Iout=1011 then outputs are Dl_Iin=0011; Iout=0011

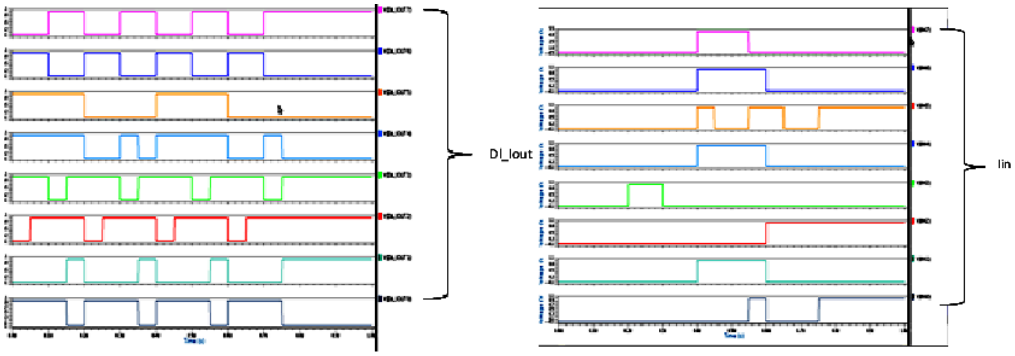

Figure 9Input waveforms of 8-bit PE3.

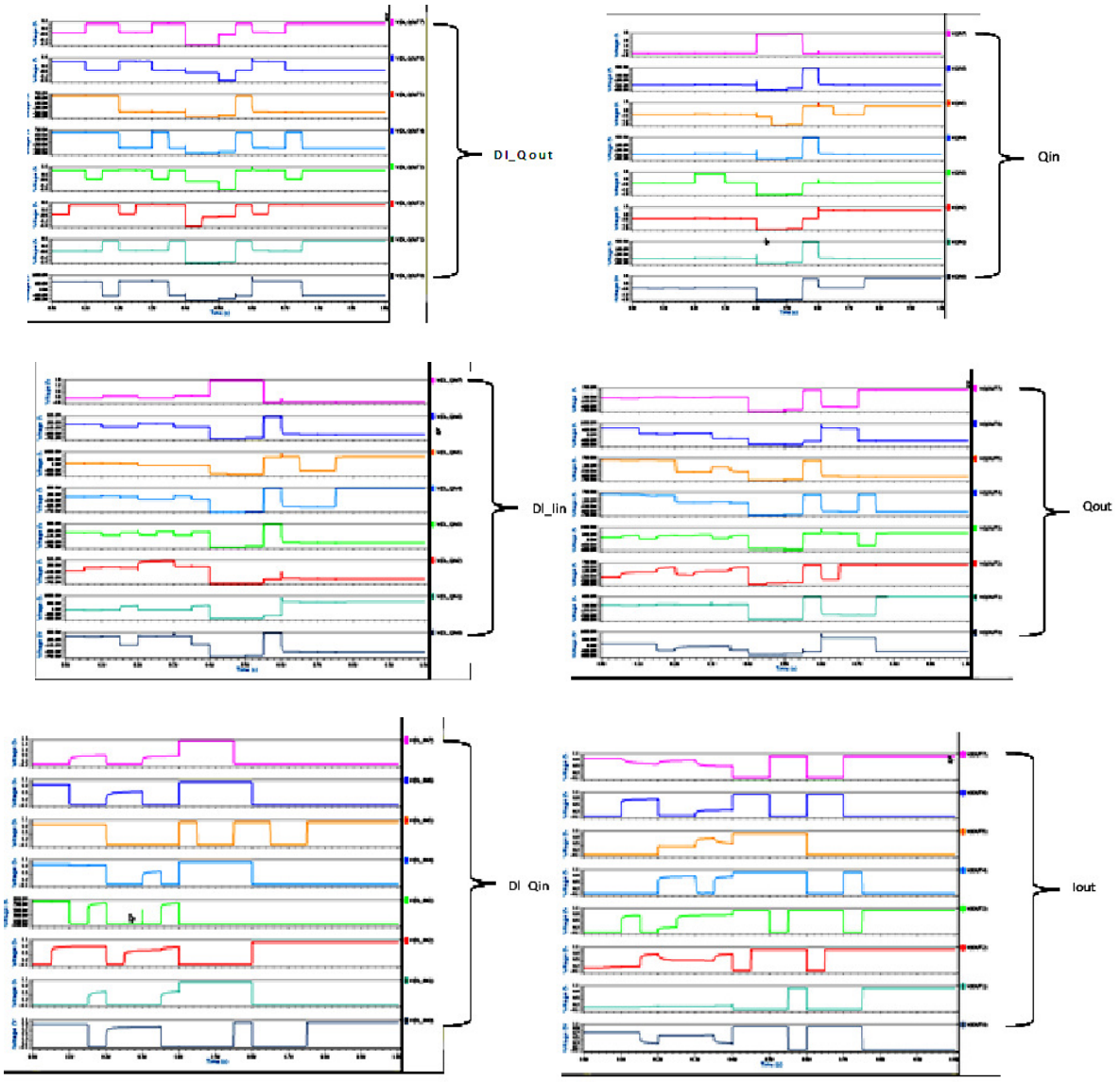

Figure 10 Output waveforms of 8-bit PE3.

The power dissipation (from the E-Z wave)of 1-bit PE3 is 0.5517 mwatts and for 8-bit PE3 it is 0.9237mwatts.

6. CONCLUSIONS

The pipelined FFT architecture contains three processing elements PE1, PE2, PE3. PE3 is the important element as it serves as a sub module to the other two processing elements PE2 and PE1.PE3 (1- bit and 8-bit) is implemented using Mentor Graphics tools and the power dissipation is observed. To implement the proposed pipelined architecture of FFT, PE2 and PE1 are to be further designed.

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