THE INFLUENCE OF SILICON AREA ON THE PERFORMANCE OF THE FULL ADDERS

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ABSTRACT

Recently, the influence of the silicon area on the delay time, power dissipation and the leakage current is a crucial issue when designing a full adder circuit. In this paper, an efficient full adder design referred to as 10-T is proposed. The new design utilized the use of XNOR gates instead of XOR in the full adder implementation and, as a result, the delay time and power dissipation are significantly decreased. In order, to show the influence of the silicon area and transistors count on the performance of the 10-T full adder, it is compared to the most recent full adders : 28-T , 20T , 16-T , and 14 –T. Simulation result based on HSPICE simulator using 16nm technology showed that the 10-T XNOR full adder significantly improved the performance of full adder through decreasing the transistors count. In addition using the multi-supply voltage of 130nm technology, in this case the proposed full adder demonstrated is the best power consumption in comparison to other designs.

I. INTRODUCTION

Addition is one of the fundamental arithmetic operations. It is used extensively in many VLSI systems such as microprocessors, embedded systems and applications with specific DSP architecture. In addition to its main task, which is adding two numbers, it is primarily used in many other useful operations such as, subtraction and multiplication [1].

In general, dynamic power dissipation, static power dissipation and leakage current power dissipation are the main factors of power dissipation in electro components [2]. Moreover, the advances in battery technology have not taken place as fast as the advances in electronic devices. Hence, designing a VLSI system faced with a number of challenges like high speed, high throughput and at the same time, consuming as minimal power as possible [3]. The full adder cell can be implemented in many different logic circuit such as complementary pass-transistor logic (CPL) , dual pass-transistor logic (DPL) , swing restored pass-transistor logic (SRPL) plus variant (SRPL2) , complementary pass transistor– transmission gate (CPL-TG) , or transmission gate logic (TG) plus variant. In this paper, only the static CMOS structure is discussed.

Recently, the size of transistor in a nanometer technology has been reduced. The number of transistors per unit area is already increased, while the supply voltage has been reduced to maintain acceptable average dynamic power dissipation per silicon area unit. Thus in order to maintain high speed transistors, some SPICE parameters such as the threshold voltage must be scaled down at the same rate as the supply voltage [4]. Consequently, the leakage current power is increased dramatically with each technology generation. The most efficient parameters that reduce the power dissipation are scaling the supply voltage, and the total load capacitor [5]. For this purpose, various techniques are proposed to efficiently reduce the power dissipation. Examples on these techniques include multithreshold voltage and low swing voltage techniques.

This paper is organized as following. In section two it described the proposed 10-T Full adder. Section three included simulation results for the Full Adders, section four discussed the minimum leakage vector technique applied in the Full Adders, while the last section was the conclusion.

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2. PROPOSED 10-T FULL ADDER

In fact, the XNOR gate forms the fundamental building block of the Full Adder. Therefore, enhancing the performance of the XNOR gates is an important trend in order to improve the performance of the Full Adder. One way to achieve this is to decrease the number of transistors constituting the XNOR gate. In this case, the full adder speed will be increased, whilst the delay time and the power dissipation are decreased. The basic Full Adder design can be given as by

$$Sum = A \text{ XOR } B \text{ XOR } C_{in} = A \text{ XNOR } B \text{ XNOR } C_{in} \quad (1)$$

$$C_{out} = C_{in} * (A \text{ XOR } B) + AB \quad (2)$$

As shown in the next table and by Boolean algebra theorem that said X'' = X , we show that

$A \text{ XOR } B \text{ XOR } C_{in}$ equal to $A \text{ XNOR } B \text{ XNOR } C_{in}$

A XOR B= A'B+AB'

So A XOR B XOR C = (A'B+AB')' C + (A'B+AB') '

=AB'C'+A'BC'+((AB')'(A'B)')C

= AB'C'+A'BC'+((A'+B)(A+B'))C

= AB'C'+A'BC'+((A'C+BC)(AC+B'C))

= AB'C'+A'BC'+(A'CAC+A'CB'C+BCAC+BCB'C)

= AB'C'+A'BC' +(C(A'A+A'B'+BA+B'B)

= AB'C'+A'BC' +C(A'B'+AB)

= AB'C'+A'BC'+A'B'C+ABC (3)

A XNOR B = AB+A'B'

So A XNOR B XNOR C = (AB+A'B')C+ (AB+A'B')'C'

=ABC+A'B'C +((AB)'(A'B')')C'

= ABC+A'B'C+(((AB)'C')((A+B)C'))

= ABC+A'B'C+(((A'+B')C')(AC'+BC'))

ABC+A'B'C+((A'C'+B'C')(AC'+BC'))

= ABC+A'B'C+(A'C'AC'+A'C'BC'+B'C'AC'+BC'B'C')

= ABC+A'B'C+C'(A'A+A'B+B'A+B'B)

= ABC+A'B'C+C(A'B+B'A)

= ABC+A'B'C+ A'BC'+AB'C' (4)

Table 1: truth table for XNOR / XOR Gate

A	B	C	Sum	carry	A XOR B	A XOR B XOR C	A XNOR B	A XNOR B XNOR C
0	0	0	0	0	0	0	1	0
0	0	1	1	0	0	1	1	1
0	1	0	1	0	1	1	0	1
0	1	1	0	1	1	0	0	0
1	0	0	1	0	1	1	0	1
1	0	1	0	1	1	0	0	0
1	1	0	0	1	0	0	1	0
1	1	1	1	1	0	1	1	1

2.1 THE DESIGN OF XNOR GATE

Figure 1 shows an efficient 2-Input XNOR logic gate [11], it contains from one pMOS transistor to produce logic one while the other two nMOS transistors are used to produce logic 0 , the output characteristic for this gate shown in Table I

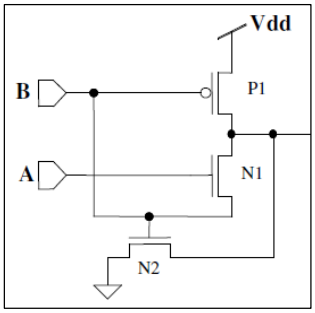

Figure 1. XNOR Logic Gate [11]

This gate is more preferable than any other XNOR logic gate, as the total power dissipation and speed operation in this circuit is less than all other XNOR gates in the same logic families as will be discussed in details in the reset of this paper.

Table2: Truth table for XNOR gate in Figure 1

INPUTS		OUTPUT
A	B	
0	0	1
0	1	0
1	0	0
1	1	1

At any Full Adder, the SUM circuit constitute from two XNOR gates as declared from equation (1). Therefore, applying the 3-transistor XNOR gate shown in Figure 2.a, could perform the SUM function by only 6 transistors, while the Carry out could be implemented using only two NMOS transistor, as shown from Figure 3.

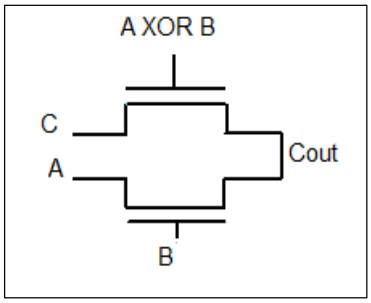

Figure2.The carry out circuit of new Full Adder design

Figure 3 shows Full Adder with 10 transistors that perform the SUM circuit; the SUM circuit consists from two XNOR gates in series. The output of (A XNOR B) is XNORed again with the Cin to perform the SUM. The Carry out circuit contains from two nMOS transistor built by CPL logic gate. The logic operation of the Carry out is very simple, it is ANDed the (A XOR B) with Cin or it is ANDed A with B. This simple gate implemented by 2 transistors only to perform the Carry out successfully.

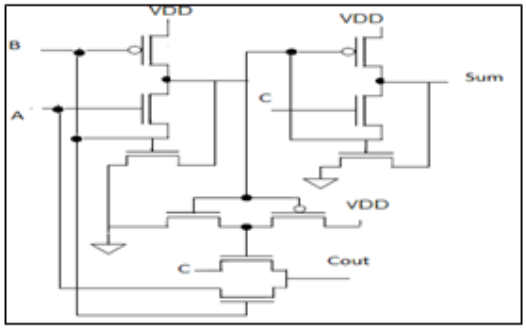

Figure3. The 10-Transistor Full Adder design

Simulation results of three inputs are shown in Figure 4, from these waveforms, it seems that for three input combinations; there are correct waveforms in the output which verifies the validity of the 8-T Full Adder. The weakness of this Full Adder appears at the outputs when the inputs A is High, B is Low, & C is High, or when the inputs A is High, B is High & C is High correspondingly.

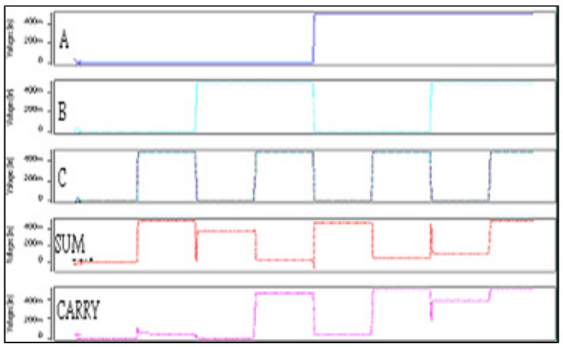

Figure4. Input/Output waveforms of the 10-T Full Adder

To solve this problem, multi-supply voltage technique is applied on this Full Adder to get efficient results at the output. Multi-Supply voltage technique is an efficient technique used recently to reduce the total dynamic and static power dissipation [12]. This technique is based on using different levels of supply voltages in the circuit in order to reduce the power dissipation and increase the speed operation In the next figure we put 2 inverter after SUM circuit and Carry circuit to get good one and zero at the output as shown in fig 5

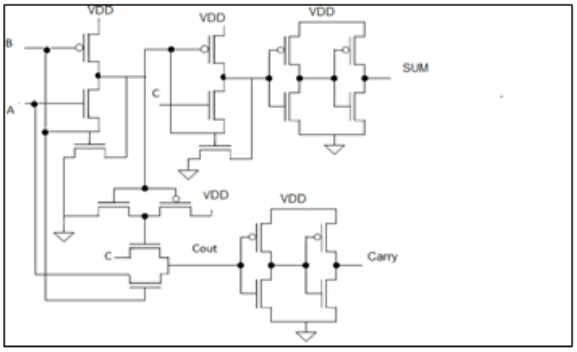

Figure 5. The 10-Transistor Full Adder design with inverters

Applying Multi-supply Voltage Technique on the 10-transistor Full Adder, as shown in Figure 6, it will yield correct outputs as shown in Figure 4.c, it seems that the output operates correctly without any degradations.

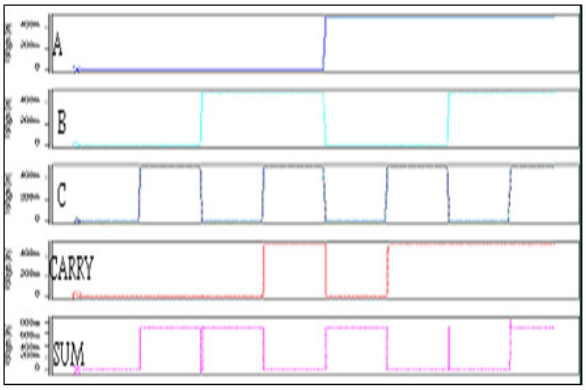

Figure6. Simulation Result Waveforms of the 10-T Full Adder with Inverters

3. SIMULATION

In order to evaluate the performance of the 8-Transistor Full Adder, various evaluations and comparison results between this Full Adder with other types are discussed and analyzed in this section. The simulation results are given under the same circumstances of SPICE parameters, the comparatives are given between the dynamic power dissipation with different values of load capacitor, delay time, and leakage power, under 16nm technology SPICE Foundries.

3.1 DELAY TIME

Delay analysis of VLSI circuits is a key element in timing verification and speed execution, gate-level simulation and performance layout design [9]

One of the most important parameters in the circuit level is the delay time, the delay time increases by decreasing the power supply voltage. For this purpose, the logic high of three inputs is taken as 0.7V. This value is selected after different tests and simulations using the range between (0.6V to 1.2V). The difference between the delay time of these Full Adders appeared very clear around this value. Table 4 shows the delay time of six Full Adders using different values of load capacitance at the output of these Full Adders. It is clearly shown that the 8-Transistor Full Adder is the fastest design in comparison to all others. SERF Full adder behaves highly comparable with the 8-Transistor Full Adder for load capacitance of 10fF and 20fF. However for higher values, the 8-Transistor Full Adder achieved the lowest delay. Figure 7 shows these simulation results.

Table 3: Delay time in different value of load capacitor (e-007)

CL	28-T	20-T	16-T	14-T	10-T	10T(P)
10fF	0.095	0.06	0.04	0.01	0.015	0.01
20fF	0.13	0.075	0.065	0.025	0.03	0.026
30fF	0.15	0.1	0.082	0.04	0.045	0.042
40fF	0.16	0.13	0.1	0.045	0.05	0.048
50fF	0.18	0.15	0.12	0.055	0.07	0.060
60fF	0.21	0.17	0.14	0.065	0.09	0.072

Figure 7 shows the values in Table IV as a chart in order to declare the difference between the Four tested Full Adders

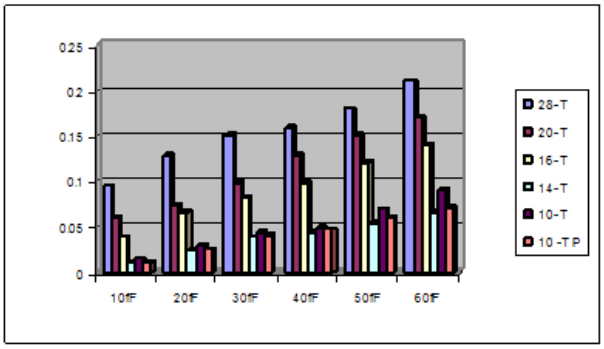

Figure 7. The delay time for each Full Adder under different values of load capacitors

3.2 DYNAMIC POWER DISSIPATION

Dynamic power dissipation is appeared when the transistor changes its status from high to low or from low to high. The most efficient parameters of dynamic power dissipation are the supply

voltage. For this purpose, Table V shows the dynamic power dissipation for each Full Adder at different values of load capacitor. Simulation results show that the 8-Transistor Full Adder has the lowest dynamic power dissipation. This is because it does not contain direct supply voltage (VCC) within its circuit except the two added Inverters (in case they are added). Figure 8 shows that the TFA Full Adder consumes higher than others. Then SERF and 14-T Full Adder, respectively, while the 8-T Full Adder consumes the lowest power dissipation comparing to all other circuits.

Table 4: Dynamic power dissipation for each Full Adder in different value of Load Capacitor

L	8T	0T	6T	4T	0T	0T Proposed
0Ff	10	02	50	1	2	7
0fF	14	05	55	3	4	8
0fF	19	08	63	4	7	0
0fF	22	15	69	9	4	2
0fF	26	21	70	3	9	9

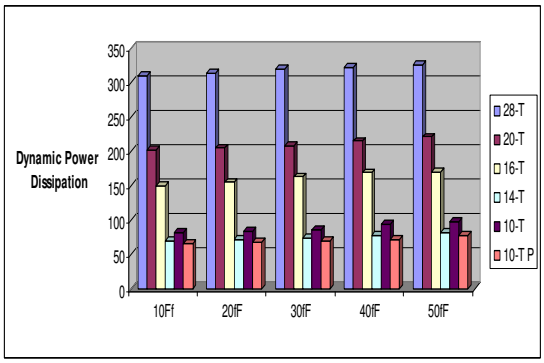

Figure 8. Dynamic power dissipation in deferent value of load capacitor

3.3 LEAKAGE CURRENT:

The leakage current is defined as the small amount of current that flows through a photonic semiconductor device when it is not operating. It is also known as dark current [10]

The leakage current becomes important issue especially when the nano-scale technology is used. The value of leakage current will be increased as the length of the gate is reduced. Therefore, it is interesting to look for new techniques that reduce the leakage power dissipation when transistor is in off state. One of these techniques is the Minimum Leakage Vector [12] [13]. The main concept of this technique is to select the proper input vector so that the major transistors of the circuit remain in ON state when the circuit is off. In our case, for one single Full Adder, it is easy to

select the proper input combination of three inputs manually. The second step of this technique is to calculate the leakage current of each transistor independently. For 16nm SPICE parameters, the leakage current for NMOS is 2.8e-011A and the Leakage current for PMOS is 7.37e-011A.Therefore, the leakage power dissipation could be calculated from the following equation:

$$P_{Leakage} = I_{Leakage} \times V_{CC} \qquad (5)$$

3.4 Leakage Power

Table 5 shows the leakage power dissipation for each Full Adders using different values of supply voltage (VCC). As can be seen from this table, the proposed 10-T adder is the best adder in terms of leakage power; the second adder is the 10-T adder, while the worst case appeared for the 28-T Full Adder.

Table 5: Leakage power for each FA in different value of load capacitor (nA)

Vcc	28-T	20-T	16-T	14-T	10-T	10-T Proposed
2.4	1366.8	989.8	976.3	512.4	444.3	400.6
2.1	1195.9	866	845.3	448.3	388.7	350.3
1.8	1025.1	742.3	732.2	384.3	333.2	300.3
1.5	854.25	618.6	610.2	320.3	277.6	250.2
1.2	683.4	494.8	488.1	256.2	222.1	200.1
1	569.5	412.4	406.8	213.5	185.1	166.8

3.5 SWITCHING ACTIVITIES

Switching activity known as how many times the transistor is switching from one to zero or from zero to one. In addition, switching activity is important to decide the critical path in the design. In Table 6, the switching activity for each adder is shown. As expected, when the transistor counts of full adder coming down, the switching activity for all full adders is coming down with positive proportional. It is apparent that the 28-T full adder has the largest value of switching activity while the 10-T full adder has the lowest switching activity.

Table 6: Switching activity for each full adder

full adder type	switching activity
28-T	104
20-T	50
16-T	40
14-T	42
10-T	26
10-T P	27

Figure 9 shows the switching activity for each full adder. The 28-T full adder has the largest value of switching activity, because it have a largest number of transistors while the 10-T full adder has the lowest value of switching activity because it has the least number of transistor

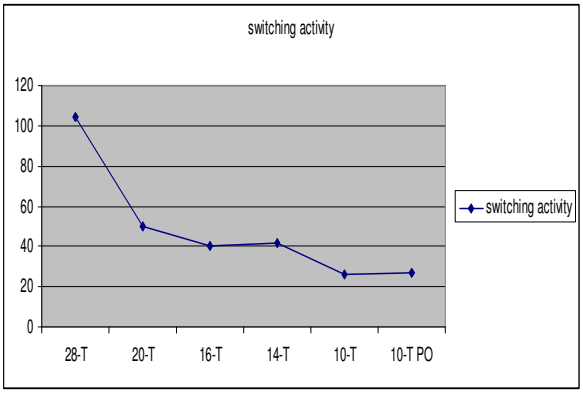

Figure 9: switching activates of all full adders

4. CONCLUSION

In paper, 8-transistor of NOR gate to build a full adder design was proposed. Three different Full Adder circuits based on Complementary Pass Transistor Logic has been compared with the proposed 8-transistor Full Adder.. The comparison results between these transistors in terms of power dissipation, delay time, and leakage power, were conducted, it is shown that the 8-transistor Full Adder has superiority in reducing the power dissipation of dynamic and leakage current, as well as the delay time. In order to verify these results, three various predictive SPICE parameters were tested in this paper. Multi supply voltage technique was used to get exact levels of high and low. The 8-transistor Full Adder was proved to be the most usable Full Adder for next decade's applications.

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