DUAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH LOW POWER CONSUMPTION

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ABSTRACT

In this paper, a novel low-power dual edge-triggered (DET) D-type flip-flop is proposed. This design achieves dual edge-triggered with two parallel data paths work in opposite phases of the clock single. Among them, a latch circuit structure employs differential input data signals which deposits very little capacitance on the clock line is accomplished. For fair comparison, four previously reported DET flip-flops along with the proposed DETFF (DET flip-flop) are compared in terms of power consumption and power-delay product (PDP), under different data activities and different data rates. Several HSPICE simulation results show that the proposed DETFF is superior in power reduction at different parameters as compared to the existing DETFFs. Hence, the proposed DETFF is well suited for low power applications.

KEYWORDS

Single Edge-Triggered (SET), Dual Edge-Triggered (DET), Flip-Flop, Power Consumption, Power-Delay Product (PDP)

1. INTRODUCTION

Flip-flops are the basic storage elements used in synchronous digital VLSI circuits and in other digital electronic circuits. Edge-triggered flip-flops are often used to operate in selected sequences during recurring clock intervals to sample and hold data. Edge-triggered flip-flop circuits may be classified into one of two types. The first type latches data either on the rising or the falling edge of the clock cycle is so-called single edge-triggered flip-flop (SETFF). A conventional SETFF is triggered either at the rising edge or the falling edge of a clock cycle. This configuration is inefficient as half of the clock edges being unused, data flow tends to be slow. The other type is dual edge-triggered flip-flop (DETFF), which can operate at half of the clock frequency while maintaining the same data throughput compared to SETFF [1]. As a result, power consumption is reduced, making DETFFs desirable for low power applications [2]-[19]. There are several ways to implement a dual edge-triggered flip-flop. Among them, the most common one is to duplicate the pathway to enable the flip-flop to sample and hold data on every clock edge. However, the implementation of conventional static DETFF needs many transistors and spends too much area [20]. Furthermore, a clock chain is required to produce the correct timing that enables the DETFF circuit to function; this requirement increased the total power consumption of the design.

Currently, power consumption of VLSI chips is becoming an increasingly critical problem as modern VLSI circuits continue to grow and technologies evolve. In portable systems, very low power consumption is desired to increase battery life [20]. Accordingly, for any digital circuit design, power consumption has to be taken into account very seriously. In digital CMOS circuits, there are four components of power consumption as following:

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$$\begin{aligned} P_{avg} &= P_{sw} + P_{sc} + P_{leakage} + P_{static} \\ &= \alpha C_L V_{DD} V_S f_{ck} + I_{sc} V_{DD} + I_{leakage} V_{DD} + I_{static} V_{DD} \end{aligned} \quad (1)$$

where P_{sw} is the switching power, P_{sc} is the short-circuit power, $P_{leakage}$ is the leakage power, and P_{static} is the static power. In general, the switching power component usually dominates, and may account for more than 90% of the total power [3]-[6]. Further, α denotes the transition activity factor. *Vs* is the voltage swing, where in most cases it is the same as the supply voltage V_{DD}. C_L is the node capacitance, f_{ck} is the clock frequency. Although the clock frequency is determined by the system specifications, the usage of DETFFs can reduce the clock frequency to half of its original value for the same data throughput. As a result, power consumption is reduced, making DETFFs desirable for low power applications [3]. As can be seen from this equation, a decrease in the capacitance on the clock line will decrease the power consumption of the clock line.

In order to reduce the complexity of circuit design, a large proportion of digital circuits are synchronous circuits; that is, they operate based on a clock signal. Among the more popular synchronous digital circuits are edge-triggered D-type flip-flops. The total clock related power consumption in synchronous VLSI circuits can be divided into three major factors: power consumption in the clock network, power consumption in the clock buffers, and power consumption in the D-type flip-flops [9]. It is worth noting that the frequency at which synchronous devices are able to operate has been limited by clock skew. The greater the frequency of the clock, the smaller the clock skew must be kept to maintain synchronization of the device. It has been observed that clock skew decreases as capacitance on the clock line is decreased. Thus, reducing capacitance on the clock line may allow synchronous circuits to operate at higher clock frequencies. Therefore, the improvement of such flip-flops circuits a decreasing in power consumption, without impairing other characteristics, is of prime importance to the VLSI industry. Though several contributions have been made to the art of DETFFs, a need evidently occurs for a design that still further improves the relative power consumption of DETFFs.

The remainder of this paper is organized as follows. Section II presents a brief description of existing DETFFs. The proposed DETFF is described in Section III. The simulation results and a comparison between the existing DETFFs and the proposed DETFF in terms of power consumption and power-delay-products are discussed in Section IV. Last section is a conclusion and summary for the paper.

2. EXISTING DUAL EDGE-TRIGGERED FLIP-FLOPS

There are several DETFFs have been proposed [2]-[19]. Among them, some DET D-type flip-flops have been presented by Unger [2]. Even though the flip-flops described in his paper are faster compared with some SETFFs, their complex design has made it undesirable. Gago *et al.* [3] presented a static DET master-slave flip-flop. The design duplicates a SETFF but shares the clock transistors that are common to both latches. These implementations suffer from a larger clock load at the same level of performance as a SETFF. Hossain *et al.* [4] proposed a static DETFF which including a 16-transistor arranged in a parallel configuration. The design also comprises two latches, each of which has a loop within itself for maintaining charge levels for providing static functionality. The loops are isolated from each other. Blair [5] provided a static DET design and a semi-static DET design. The static DET design is a modified version of Hossain's static design. Varma *et al.* [6] provided a static DET design and a dynamic DET design. This includes a 16-transistor CMOS implementation of the static design in which the availability of an inverted clock is assumed. The design requires two more transistors if the clock is to be inverted locally.

The flip-flop DET_{pedram} proposed in [7] is illustrated in Fig. 1. To reduce the overall transistor count as well as the load on the clock signal, two pass transistors are employed in the feedback portion instead of transmission gates. This results in reducing the driving capability of the succeeding stages and causing DC power consumption in the output inverter. Fig. 2 shows the circuit implementation of DET_{llopis} proposed in [8]. There is made unidirectional on the data paths, which is a modified version of the DETFF proposed in [4]. Complementary logic gates are employed to balance the output rise and fall times of the original DETFF. Advantageously, the usage of DETFFs leads to a reduction of 50% in power consumption of the clock network, and a reduction of up to 45% in the power consumption inside the flip-flops. However, the area and delay penalties are rather large.

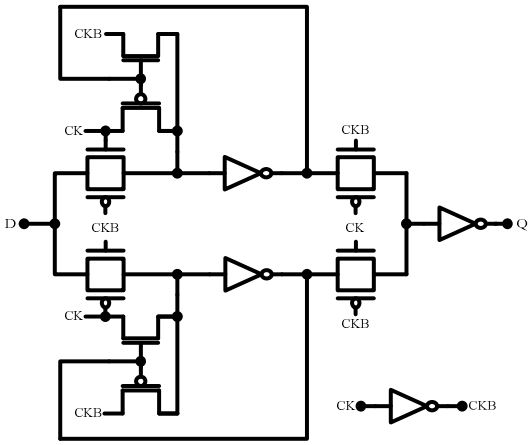

Figure 1.DET_{pedram} proposed in [7].

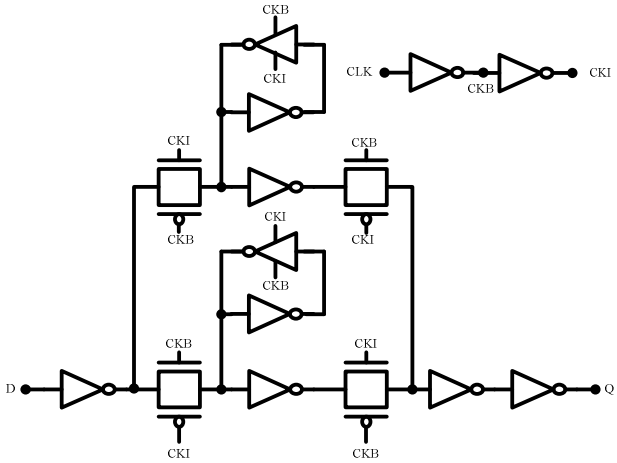

Figure 2. DET_{llopis} proposed in [8].

Strollo *et al.* [9] proposed a low power DETFF using a single latch, $DET_{Strollo}$, shown in Fig. 3. The operation of $DET_{Strollo}$ is highly dependent on the internal clock buffer sizing and the propagation delay of the internal clock buffers. It compares the input data D to output data Q and according to the comparison will disable those unnecessary clock switching. More particular for this clock-gating scheme, whenever the comparator detects the change at the input, the gated clock signal will generate a pulse. Otherwise, the gated clock signal maintains logic high. If this clock-gating scheme is used on the DETFF, then the flip-flop will be triggered twice for every

data transition, which causes extra power consumption. $DET_{Strollo}$ uses only eight MOS devices in addition to the clock driver, and hence requires a small silicon area. Another DETFF illustrate in Fig. 4, DET_{chung}, is proposed by Chung *et al.* in [10], which comprises two differential SETFFs connected in parallel. The data path is duplicated. Both SETFFs have a pair of cross-coupled inverters as the master stage and a tri-state inverter as the slave stage, respectively. The left data path samples data when CLK=1, the right data path samples data when CLK=0. The main advantage of this design is the ability to avoid stacking PMOS transistors over NMOS transistors, and the prevention of floating nodes. However, a relatively large crossover current exists in the internal nodes, causing significant delays and high power consumption [11].

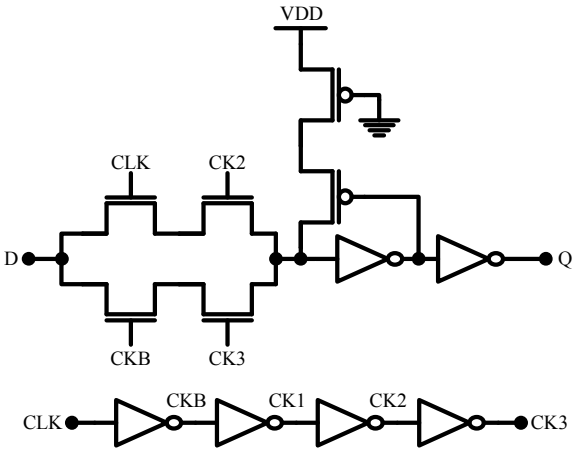

Figure 3. $DET_{Strollo}$ proposed in [9].

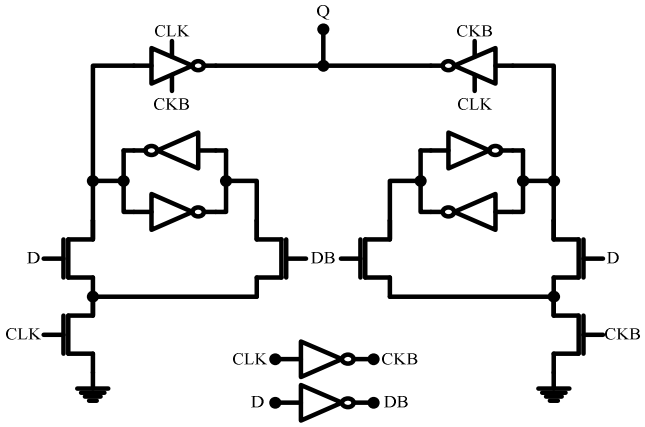

Figure 4. DET_{chung} proposed in [10].

As shown above, a problem with static flip-flop circuits is a requirement for more than one clock signal. Usually, a clock chain is required to produce the correct timing that enables the circuit to function. This requirement increased the total power consumption of the design. In order to overcome the problem of distributing several clock signals and avoid the serious problems caused by clock skew, only one clock signal is employed in the proposed DETFF design.

3. PROPOSED DUAL EDGE-TRIGGERED FLIP-FLOP

The proposed DET D-type flip-flop is illustrated in Fig. 5. The proposed DETFF is composed of six pass transistors, two latches, and an output keeper circuit. Among them, the latches are respectively constructed by back-to-back configuration of inverters I1, I2 and inverters I3, I4; the output keeper circuit is formed by inverter I5 and regenerative transistor MP4. In the output near the supply voltage VDD when output terminal Q is at logic low.

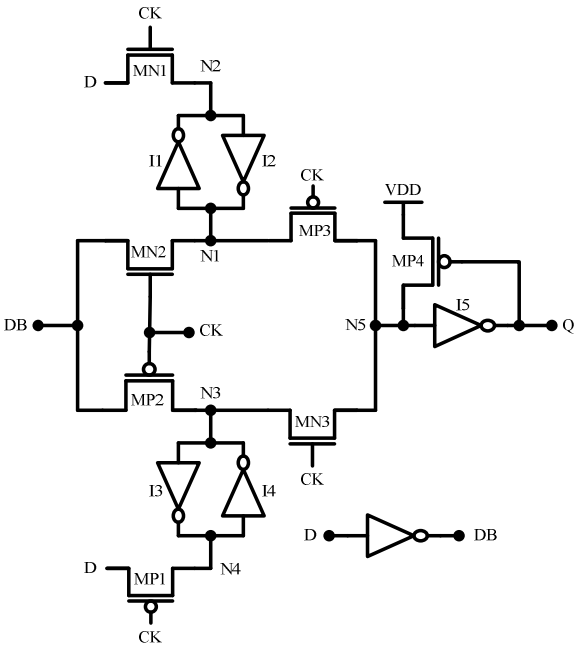

Figure 5.Circuit diagram of the proposed flip-flop DET $_{proposed}$.

This design also can be thought of as a parallel structure which similar to that of DET_{chung}. Similarly, two differential master-slave flip-flops connected in parallel and each of flip-flop utilizes differential data signals at the master stage. As shown in Fig. 5, master latch can be further divided into sample portion and hold portion. The sample portion of the latch receives the differential data signals and passes them to the hold portion responsive to a control signal. However, the hold portion stores and outputs the differential data signals. In more detail, in the upper data path, the sample portion is for providing the differential data signals to hold portion when the clock signal is at logic high. The hold portion is for storing the differential data signals it receives from sample portion. A clock signal CK is provided to the gate terminal of both transistors MN1 and MN2. When the clock signal is at logic high, both transistors MN1 and MN2 are turned on. Conversely, when the clock signal is at logic low, both transistors MN1 and MN2 are turned off. The clock signal thus selects when the data signal D and the inverted data signal DB are passed to hold portion. The back-to-back configuration of inverters I1 and I2 stores the data signal D and the inverted data signal DB which are passed to hold portion. Finally, node N1 and node N2 provide the inverted data signal and the data signal, respectively, stored in hold portion. Besides, in the lower data path, master latch is essentially the same as that of the upper data path previously described, except transistors MP1 and MP2 are provided in place of transistors MN1 and MN2, respectively. Thus, sample portion provides the differential data signals to hold portion when the clock signal is at logic low. It is worth noting that, in this design, each data line in the sample portion comprises a single pass transistor for selectively passing one of the differential data signals responsive to the control signal, unlike that of DET_{chung} which a tri-state inverter is used.

Next, the operation of the proposed DETFF circuit will be explained as follows. When the clock signal CK is at logic low, transistors MP1, MP2, MP3 are turned on and transistors MN1, MN2, MN3 are turned off. The inversed signal of input signal D and the input signal DB are quickly conducted into the node N3 and hold by the latch constructed by inverters I3 and I4. Meanwhile, the previously hold data in node N1 is quickly pass to the output terminal Q with the help of transistor MP3. If the voltage level of the output terminal Q is at logic low, node N5 goes logic high with the help of regenerative transistor MP4. Node N5 remains high as long as the output terminal Q is at logic high. On the contrary, when the clock signal CK is changed from logic low to logic high, transistors MN1, MN2, MN3 are turned on and transistors MP1, MP2, MP3 are turned off. Because MN1 and MN2 are turned on and MP3 is turned off, the inversed signal of input signal D and the input signal DB are temporarily stored in the node N1 and hold by the latch constructed by inverters I1 and I2. Meanwhile, the data signal stored in node N3 output to the output terminal Q via transistor MN3. Furthermore, if the voltage level of the output terminal Q is at logic low, the storage node N5 will be pulled up to a logic high via regenerative transistor MP4. Therefore, when the clock makes a inverse transition, the role of upper pathway and lower pathway is exchanged, exhibiting alternative sampling and transporting behaviour.

4. SIMULATION AND RESULTS

Several metrics are available for analysis of VLSI circuits, such as the delay from data to the output (t_{dq}), the total power consumption (P_{total}), the power-delay product (PDP_{dq}), and the energy-delay product (EDP_{dq}). In the section, simulations are performed to examine the performance and merit of the proposed DETFF.

4.1. TESTBENCH

The testbench for this paper is illustrated in Fig. 6 [8]. The input buffers are used to provide realistic data and clock signals. A fanout of five inverters is used as the nominal load for each DETFF. These inverters, in turn, drive a capacitive load C_L of 25 fF each, to simulate the loading from the previous logic stages, as well as the following stages. The total power consumption is composed of three components: local data power consumption, local clock power consumption, and internal power consumption. It is worth noting that the clock power consumption is determined solely by the clock load of the flip-flop, whereas the distribution of the internal and data power consumption is affected by the structure and operation of the latching element itself as well as the input switching activity [10].

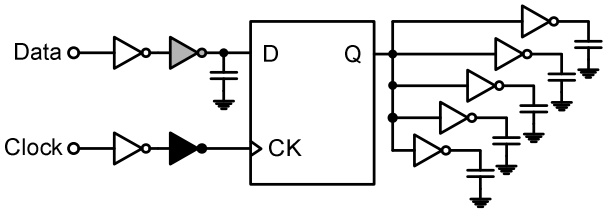

Figure 6.The simulation testbench for each DETFF.

4.2. SIMULATION RESULTS AND DISCUSSION

This subsection presents the simulation results of power consumption of the proposed DETFF with four previously DETFFs discussed in section 2, under different data activities and different data rates, respectively. To evaluate the performance of the proposed DETFF, other designs are simulated under similar conditions. All simulations are carried out using a 0.18 um CMOS technology at nominal conditions: VDD=1.8V and at room temperature. Fig. 7 illustrates the

simulated analysis waveform of the proposed DETFF. During this simulation, a data activity of 0.5 and a data rate of 500 Mbits/sec are assumed.

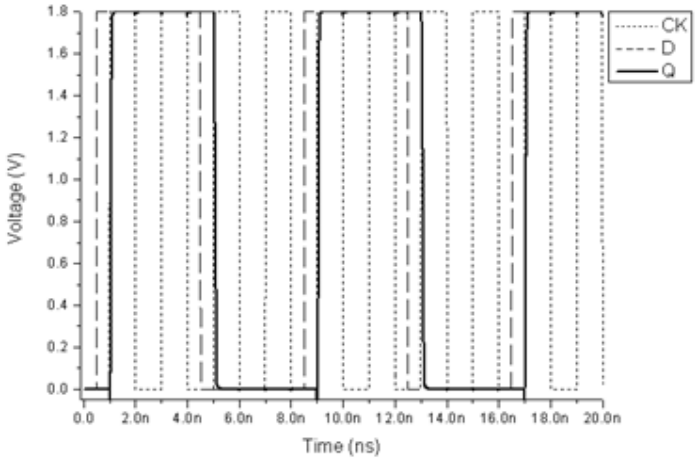

Figure 7.Transient analysis waveform of the proposed DETFF.

Table 1 illustrates a comparison among different metrics for various DETFFs are performed, based on the same conditions as above. As shown in Table 1, it appears that DET_{pedram} consumes the most power, due to an extensively large internal and data power consumption. $DET_{strollo}$ has the longest delay. This also leads to the maximum energy consumption. $DET_{proposed}$ consumes the least power and has the minimum delay, hence the least energy. Compared to the previously proposed DETFFs, the power reduction of this work has 26.60%, 53.63%, 16.75%, and 24.67%, respectively.

Table 1. Comparison among different parameters for various DETFFs.

	P_{total} (uW)	t_{dq} (ps)	PDP_{dq} (fJ)	EDP_{dq} (fJ)
DET_{llopis}	39.14	347.47	13.6	4725.4
DET_{pedram}	61.96	290.96	18.0	5245.4
$DET_{strollo}$	34.51	465.77	16.1	7489.7
DET_{chung}	38.14	316.68	12.1	3824.9
$DET_{proposed}$	28.73	251.63	7.2	1819.1

In general, the power-saving of using DETFF is strongly dependent on data activity α [20]. Therefore, it is desirable to simulate various DETFFs with different data activities. Table 2 demonstrates the power consumption of various DETFFs at different data activities. Also, the relationship of power consumptions versus different data activities is illustrated in Fig. 8. It can be seen that the power consumption increases with the increasing in data activity because the power consumption is proportional to the data activity. For example, in the case of applications with data activity $\alpha = 1$, exhibit the largest total power consumption.

However, one exception is DET_{pedram}, in which the data sequence consists of all 0's, the power consumption is remarkably large. On the other hand, for the case of all 1's, the power consumption is especially small, whereas the data power is notably larger. Furthermore, the total power consumption of DET_{llopis} is very close to DET_{chung} in all data activities. In addition, one

finds that $DET_{proposed}$ represents a significant power reduction over four previously reported DETFFs under different data activities, except in the case of $\alpha = 1$, in which it exhibits a substantially more internal power consumption.

Table 2.Power consumption of various DETFFs at different data activities

	α= 0 (all 0's)	α= 0 (all 1's)	α= 0.1	α= 0.2	α= 0.3	α= 0.4	α= 0.5	α= 1
DET_{pedram}	55.52	21.14	43.12	47.84	52.33	60.54	61.96	85.41
DET_{llopis}	11.23	10.63	16.60	22.25	28.26	33.79	39.14	65.32
$DET_{strollo}$	20.03	18.78	22.39	25.41	29.12	31.59	34.51	47.69
DET_{chung}	8.02	8.46	14.25	20.29	26.65	32.38	38.14	65.45
$DET_{proposed}$	2.73	3.28	8.10	13.15	18.88	23.76	28.73	54.25

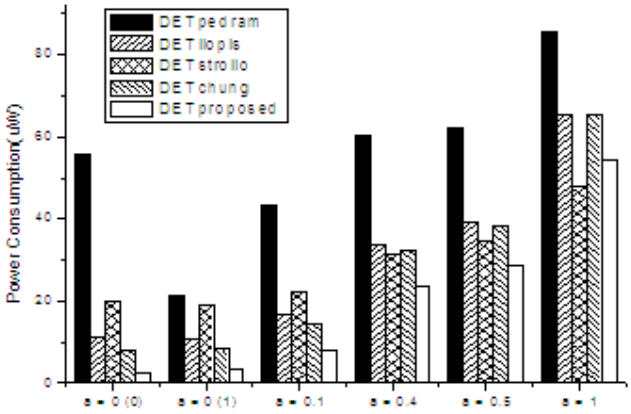

Figure 8.Power consumption of various DETFFs at different data activities.

In the following, four previously reported DETFFs along with the proposed DETFF are analysed for their power consumptions at varying data rates. The power consumptions of various DETFFs under different data rates, for different data activities, are depicted in Tables. 3-5. Table 3 indicates the power consumption at different data rates for data activity α= 0.

Table 3. Power consumption comparison under different data rates (@α= 0)

Data Rate (Mbits/s)	2000	1667	1333	1000	667	333	167
DET_{pedram}	52.09	47.34	43.14	38.33	35.87	35.61	37.76
DET_{llopis}	23.04	19.22	15.50	10.93	7.80	3.95	2.00
$DET_{strollo}$	39.55	32.88	26.38	19.41	13.11	6.72	3.28
DET_{chung}	17.50	14.51	11.85	8.24	5.80	3.06	1.50
$DET_{proposed}$	6.84	5.79	4.76	2.99	2.35	1.47	0.65

Figure 9 is a curve of power consumption versus data rates for Table 3. As can be seen from this figure, DET_{pedram} consumes the most power for all data rates. Further, the total power consumption of DET_{llopis} is very close to that of DET_{chung} for all data rates. In addition, the proposed flip-flop $DET_{proposed}$ has the least power consumption among all the designs for all data

rates. Finally, it is indicated that the proposed $DET_{proposed}$ has up to 86.87% power-saving compared with that of DET_{pedram} for data rate is 2000 Mbits/s.

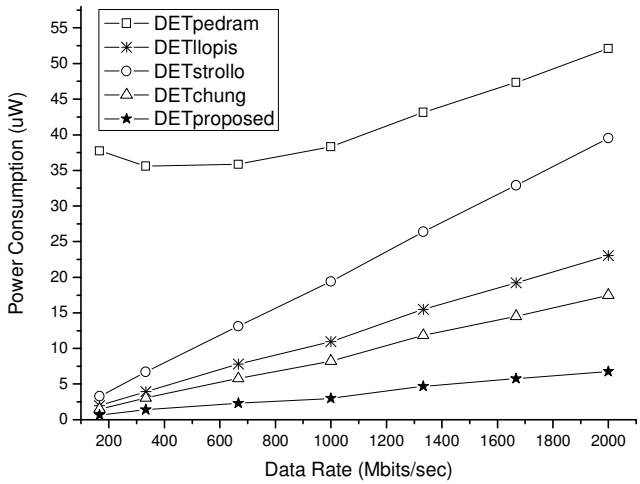

Figure 9. Power consumption dependence on data rates for data activity α= 0.

Table 4. Power consumption comparison under different data rates (@α= 0.5)

Data Rate (Mbits/s)	2000	1667	1333	1000	667	333	167
DET_{pedram}	102.91	91.12	75.17	61.96	51.08	42.93	41.26
DET_{llopis}	80.02	68.06	52.82	39.14	26.42	13.16	6.43
$DET_{strollo}$	68.45	57.80	45.49	34.51	22.43	11.25	5.54
DET_{chung}	77.12	64.86	50.84	38.14	25.37	12.69	6.21
$DET_{proposed}$	58.43	49.57	38.82	28.67	19.23	9.61	4.65

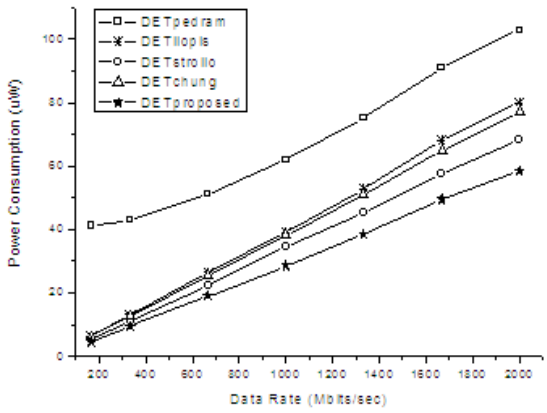

Figure 10. Power consumption dependence on data rates for data activity α= 0.5.

Table 4 indicates the power consumption at different data rates for data activity α= 0.5. Figure 10 is a curve of power consumption versus data rates for Table 4. From Table 4, one finds that the proposed $DET_{proposed}$ represents a significant power-saving over four previously reported DET

flip-flops. As can be seen from Fig. 10, DET_{pedram} consumes the most power for all data rates. Further, the total power consumption of DET_{llopis} is very close to that of DET_{chung} for all data rates. In addition, the proposed flip-flop $DET_{proposed}$ has the least power consumption among all the designs for all data rates. Finally, it is indicated that the proposed $DET_{proposed}$ has up to 88.73% power-saving compared with that of DET_{pedram} for data rate is 167 Mbits/s.

Table 5. Power consumption comparison under different data rates (@α= 1)

Data Rate (Mbits/s)	2000	1667	1333	1000	667	333	167
DET_{pedram}	140.25	118.67	102.54	85.41	66.17	50.20	44.72
DET_{llopis}	128.89	107.72	86.38	65.32	43.50	21.58	10.54
$DET_{strollo}$	91.20	76.14	62.37	47.69	31.60	16.12	8.31
DET_{chung}	121.96	103.13	85.17	65.45	44.24	22.01	10.80
$DET_{proposed}$	101.65	86.78	70.59	54.18	36.15	17.87	8.73

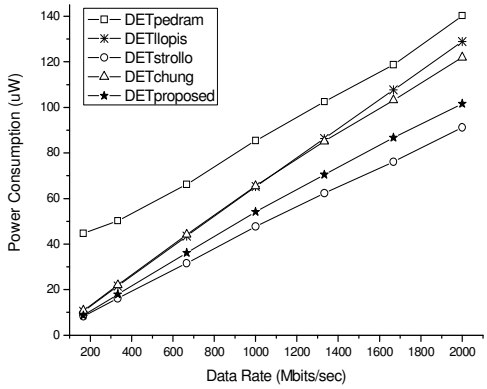

Figure 11. Power consumption dependence on data rates for data activity α= 1.

Table 5 indicates the power consumption at different data rates for data activity α= 1. Figure 11 is power consumption versus data rates curves for Table 5. From this figure, From this figure, one finds that for a low data rate, DET_{llopis} saves more power than that of DET_{chung}. However, at a high data rate, the power consumption curve of DET_{chung} starts to intersect the power consumption curve of DET_{llopis}, which means that DET_{chung} begins to save more power than that of DET_{llopis}. Furthermore, for $DET_{strollo}$, which is composed by 18 transistors always consumes less power than $DET_{proposed}$ under varying data rates, and the saving power percentage is between 4.8% and 12.6% for data activity α= 1.

In summary, from Tables 3-5 and Figures 9-11, one finds that DET_{pedram} has the worst power consumption under all parameters. Generally, although the proposed $DET_{proposed}$ consumes a little more power than the circuit of the DET_{stroll} for data activity α= 1, this situation does not affect its low power applications.

5. CONCLUSIONS

It has been observed that a significant amount of power consumption is generated by the clock line. This paper compares four previously published DETFFs together with our design for different metrics. As compared to four previously published DETFFs, our design outperforms in

terms of power consumption and power-delay-product. Especially, the proposed flip-flop is superior in power reduction at different parameters, hence, it is well suited for low-power digital system applications.

One major advantage of the proposed DETFF is that it only requires a single clock signal, as contrasted with conventional DETFFs which require a clock chain to produce the correct timing that enables the circuit to function. In addition, the usage of differential data signals in the master portion of the proposed flip-flop circuit places very little capacitance on the clock line that will decrease the power consumption of the clock line. Furthermore, the proposed DETFF has the other advantages as following: (1) results in a latch sufficiently immune from glitches; (2) allows for the strong passage of data signals using single pass transistor of the same transistor type; (3) sufficiently reduces contention in the hold portion; (4) because of the reduction in the number of devices, the wiring necessary for the clock line of this latch is reduced. The proposed DETFF is simple in design, robust and reliable in operation, and efficient in operation.

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