CONCURRENCY WITHIN TERNARY GALOIS PROCESSING OF HIGHLY-REGULAR 3D NETWORKS VIA CONTROLLED NANO SWITCHING

Anas N. Al-Rabadi

Computer Engineering Department, The University of Jordan, Amman – Jordan &
Department of Renewable Energy Engineering, Isra University, Jordan

ABSTRACT

New implementations for concurrent computing applications of 3D networks using corresponding nano and field-emission controlled-switching components are introduced. The developed implementations are performed within 3D lattice-based systems to perform the required concurrent computing. The introduced 3D systems utilize recent findings in field-emission and nano applications to implement the function of the basic 3D lattice networks using nano controlled-switching. This includes ternary lattice computing via carbon nanotubes and carbon field-emission techniques. The presented realization of lattice networks can be important for several reasons including the reduction of power consumption, which is an important specification for the system design in several future and emerging technologies, and in achieving high performance and reliability realizations. The introduced implementations for 3D lattice computations, with 2D lattice networks as a special case, are also important for the design within modern technologies that require optimal design specifications of high speed, high regularity and ease-of-manufacturability, such as in highly-reliable error-correcting signal processing applications.

KEYWORDS

3D Circuits and Systems, Carbon Nanotubes, Controlled Switching, Lattice Networks, Nanotips.

1. INTRODUCTION

With future logic realization in technologies that are scaled down rapidly in size, the emphasis will be increasingly on the mutually linked issues of regularity, predictable timing, high testability, fast fault localization and self-repair [1-8, 17, 34]. For the current leading technologies with the active-device count reaching the hundreds of millions, and more than 80% of circuit areas are occupied by local and global interconnects, the delay of interconnects is responsible for about 40-50% or more of the total delay associated with a circuit [2, 34].

In future technologies, interconnects will take even higher percent of area and delay which creates interest in regular cellular circuits, especially for deep sub-micron and nano technologies. For example, Figure 1 illustrates the delays of electrical signals for global interconnects with repeaters and without repeaters versus the gate and local interconnects [2, 34].

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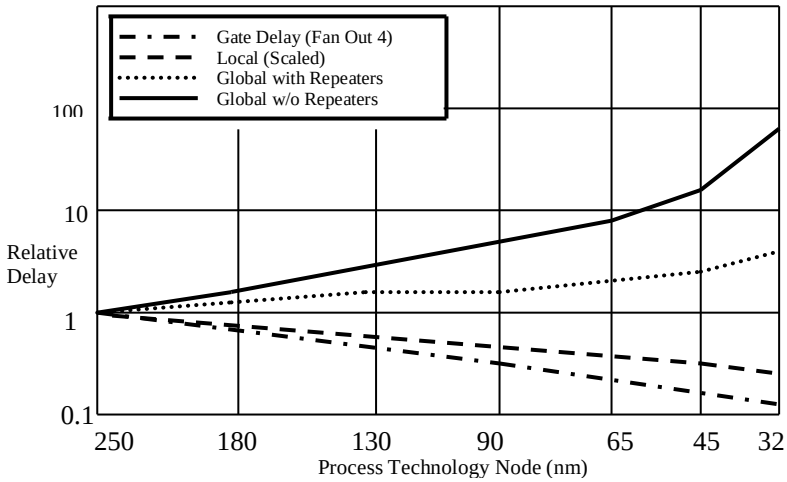


Figure 1. Delays for local and global wiring versus feature size.

Lattice circuits [2, 6] generalize the ideas from the well-known regular circuits: Fat trees, Generalized PLAs, Maitra cascades and Akers arrays [1], into a more systematic framework which is closely related to the symmetry of functions and symmetric networks [2-5]. Realization of logic circuits in 3D space can be very important for future technologies, as it shows that the best way is to place combinational logic functions in a 3D space where all local interconnections are of the same length and global interconnections are only inputs on parallel oblique planes. Moreover, 3D cubical lattice circuits have special importance since 3D crystal lattices exist where inter-related atoms, that lay in a potential field, are spaced on the corners of 3D cubes, and thus the potential of the physical implementation of 3D lattice networks using 3D crystal lattices.

Nanotechnology is an important modern scientific field that utilizes analysis and synthesis techniques from several overlapping science and engineering sectors such as physics, chemistry, electronics and biology [2, 9 - 10, 13 - 15, 18, 20 - 24, 29 - 31, 33, 35 - 36]. Nanowires, nanoparticles, Carbon nanotubes (CNTs) and Carbon nanofibers are just few examples of such important and widely-used nano systems. The CNT is an important emerging technology within nanotechnology that has wide range of applications in several various fields in technology and science, where recent examples include TVs based on CNT field-emission that are of much higher resolution than the available best plasma-based TVs, thinner and consume much less power, and CNT-based nanocircuits such as CNT-based Field Effect Transistors (FETs) that are much faster than the available silicon-based FETs and possess high potential for less power consumption. Recently, carbon nanotubes have attracted much attention not only for their unique morphologies and relatively small dimensions, but also for their potential applications in several current and emerging technologies [10, 13, 22 - 24, 31, 33]. CNT is made from graphite that is shaped in three forms within nano dimensions: (1) Carbon nanoball (or buckyball) with the shape of a soccer ball, (2) Carbon nanotube that is shaped as multi-wall CNT (MWCNT) and single-wall CNT (SWCNT), and (3) Carbon nanocoil. Field electron emission is defined as electron emission under the influence of the applied electric field from the surface of a cathode which is highly dependent upon the emitting material work function [25 – 26, 11 – 12, 16, 19, 27, 29].

In this article, the utilization of Carbon field emission – based devices that realize a basic building block in modern synthesis known as the controlled switch [2, 32] is presented, and the use of the presented Carbon field emission-based devices in three-valued 3D computations is

also shown for the widely-utilized case of ternary Galois logic. In this new realization, the applied Carbon field-emission is obtained using carbon-based nanotubes [19, 27] and carbon-based fiber nano-apex tips [11 - 12, 25]. This article introduces concurrent processing using field emission-based lattice systems. Figure 2 illustrates the corresponding layout of the introduced system design method.

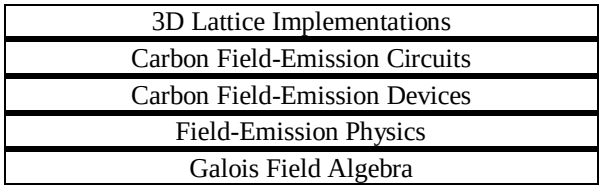


Figure 2. The introduced and utilized system implementation hierarchy.

The remainder of this article is organized as follows: Basic background on fundamentals of 3D lattice circuits and carbon-based nanotubes and nanotips are presented in Section 2. The utilization of the Carbon field emission – based devices in controlled switching is presented in Section 3. The extension of the utilization of Carbon field emission – based controlled switching to the important case of ternary computations is presented in Section 4. The implementation of controlled switching that use Carbon field emission – based devices within 3D lattice architectures is introduced in Section 5. Conclusions and future work are presented in Section 6.

2. BASIC BACKGROUND

This Section presents basic fundamentals and important background material in the fields of lattice-based networks and processing, and Carbon-based nanotubes and nanotips. This will be utilized in Section 5 for the concurrent processing within 3D lattice networks using controlled-switching via field emission – based nano multiplexing devices.

2.1. Galois Processing

The binary hierarchy of families of canonical forms [2, 28] and the corresponding decision diagrams [2, 17] are based on three basic functional expansions: Shannon, positive Davio, and negative Davio expansions, which are given below respectively [2, 28]:

$$f(x_1, x_2, \ldots, x_n) = x_1' \cdot f_0(x_1, x_2, \ldots, x_n) \oplus x_1 \cdot f_1(x_1, x_2, \ldots, x_n) \quad (1)$$

$$f(x_1, x_2, \ldots, x_n) = 1 \cdot f_0(x_1, x_2, \ldots, x_n) \oplus x_1 \cdot f_2(x_1, x_2, \ldots, x_n) \quad (2)$$

$$f(x_1, x_2, \ldots, x_n) = 1 \cdot f_1(x_1, x_2, \ldots, x_n) \oplus x_1' \cdot f_2(x_1, x_2, \ldots, x_n) \quad (3)$$

Where $f_0(x_1, x_2, \ldots, x_n) = f(0, x_2, \ldots, x_n) = f_0$ is the negative cofactor of variable x_1, $f_1(x_1, x_2, \ldots, x_n) = f(1, x_2, \ldots, x_n) = f_1$ is the positive cofactor of variable x_1, and function $f_2(x_1, x_2, \ldots, x_n) = f(0, x_2, \ldots, x_n) \oplus f(1, x_2, \ldots, x_n) = f_0 \oplus f_1$. All operations in Equations (1) - (3) are performed using Boolean algebra, where the symbols ($\oplus$) is Boolean XOR and ($\cdot$) is Boolean multiplication.

Multiple-valued spectral methods are used in many applications in analysis, synthesis, testing, classification, and verification of logic circuits and systems [2]. Because Galois field proved to possess desired properties in many implementations such as VLSI testing, communications and signal processing, the developments of 3D circuits will be conducted in this work on the

corresponding Galois field algebraic structures. Radix three Galois field GF(3) addition and multiplication are defined in Figures 3a and 3b, respectively.

+	**0**	**1**	**2**
0	0	1	2
1	1	2	0
2	2	0	1

(a)

*	**0**	**1**	**2**
0	0	0	0
1	0	1	2
2	0	2	1

(b)

Figure 3. Radix three GF operations: (a) GF(3) addition, and (b) GF(3) multiplication.

A literal is a function of a single variable. An important kind of functions is the 1-Reduced Post literal (1-RPL) [2] which is defined as follows:

$$ {}^{i}x = 1 \text{ iff } x = i \text{ else } {}^{i}x = 0 \tag{4} $$

For example $\{{}^{0}x, {}^{1}x, {}^{2}x\}$ are the zero, first and second polarities of the 1-RPL, respectively. Ternary 1-RPLs will be used in later parts of the article to construct 3D lattice circuits by controlling the propagation of sub-functions in three-dimensions.

2.2. Regular 2D Lattice Circuits

The concept of lattice circuits for switching functions [1 - 2] involves three components: (1) *expansion* of a function - that corresponds to the initial node (root) in the lattice - which creates several successor nodes of the expanded node, (2) *joining* (*collapsing*) of several nodes of a decision tree level to a single node, which is the reverse operation of the expansion process, and (3) *regular geometry* to which the nodes are mapped that guides which nodes of the level are to be joined.

While the realization of Boolean non-symmetric functions in Akers arrays [1] requires an exponential growth of repetition of variables in the worst case, the realization of Boolean non-symmetric functions in lattice circuits requires a linear growth of repetition of variables, and consequently one needs not to repeat the variables of non-symmetric functions too many times to realize such functions in lattice circuits for most practical benchmarks [2 - 6].

Figure 4 illustrates, as an example, the geometry of a 4-neighbor lattice circuit and joining operations on the nodes where each cell has two inputs and two outputs (i.e., four neighbors). The construction of the lattice circuit in Figure 4 implements the following one possible convention: (1) top-to-bottom *expansion* and (2) left-to-right *joining* (i.e., left-to-right propagation of the corresponding correction functions in Figures 4c and 4d, respectively).

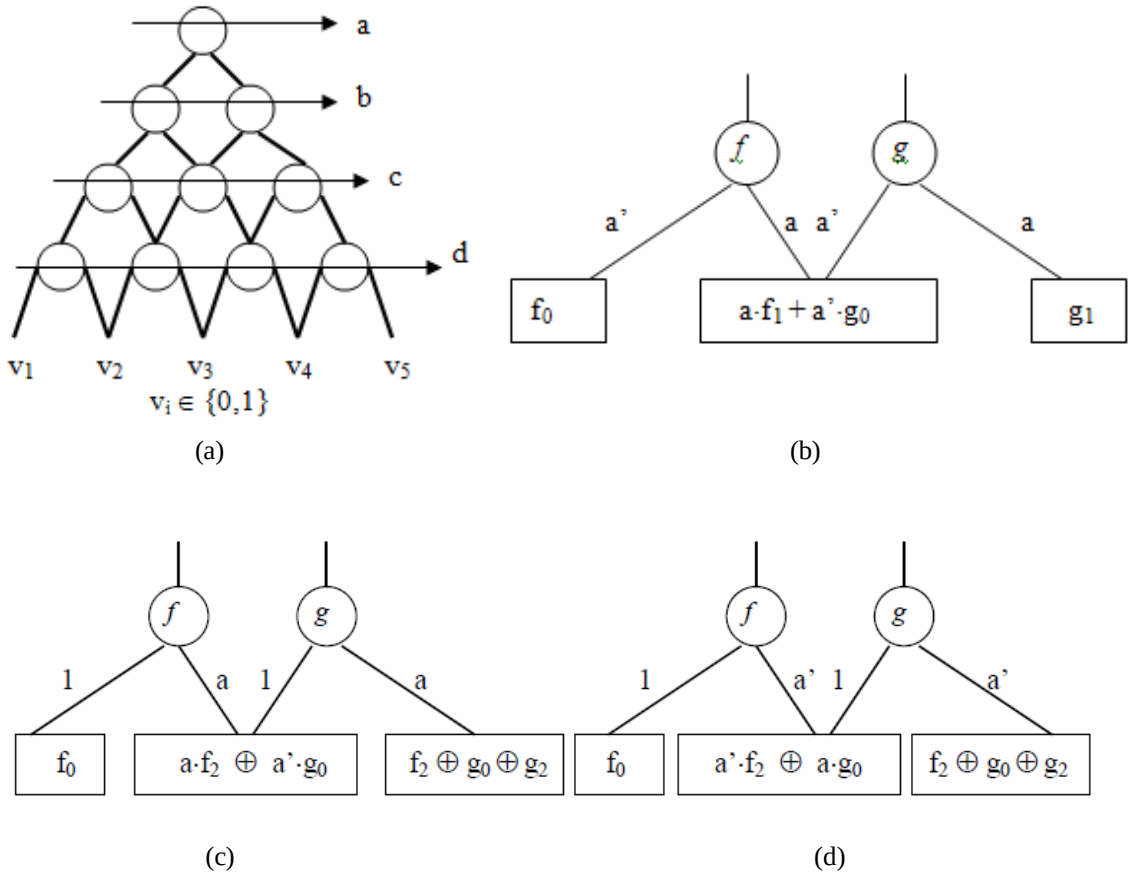


Figure 4. Regular 2D lattice networks: (a) A general 2D 4-neighbor lattice circuit, (b) joining rules for binary Shannon lattice circuit, (c) joining rules for binary positive Davio lattice circuit, and (d) joining rules for binary negative Davio lattice circuit, where the symbols (+) is the Boolean addition, (·) is the Boolean multiplication and (⊕) is the Boolean XOR.

Definition 1. The function that is generated by joining two nodes (sub-functions) in a lattice circuit is called the *joined function*. The function that is generated in nodes other than the joining nodes, to preserve the functionality within the lattice circuit, is called the *correction function.*

Note that the lattices shown in Figure 4 preserve the functionality of the corresponding sub-functions *f* and *g*. This can be observed, for instance, in Figure 4b as the negated variable *a*' will cancel the un-complemented variable *a*, when propagating the cofactors from the lower levels to the upper levels or vice versa, without the need for any correction functions to preserve the output functionality of the corresponding lattice circuit. This simple observation cannot be seen directly in Figures 4c and 4d, as the correction functions are involved to cancel the effect of the new joining nodes for the preservation of the functionality of the new lattice circuits (these correction functions are shown in the extreme right leaves of the second level in Figures 4c and 4d, respectively).

It is shown in [2 - 5] that every function that is not symmetric can be symmetrized by repeating variables, and that a totally symmetric function can be obtained from an arbitrary non-symmetric

function by the repetition of variables. Consequently, lattice circuits and the symmetry of functions are very much related to each other.

Example 1. For the following non-symmetric three-variable Boolean function F = a·b + a'·c, by utilizing the joining rule that was presented in Figure 4b for 2D lattice circuit with binary Shannon nodes, one obtains the following lattice circuit.

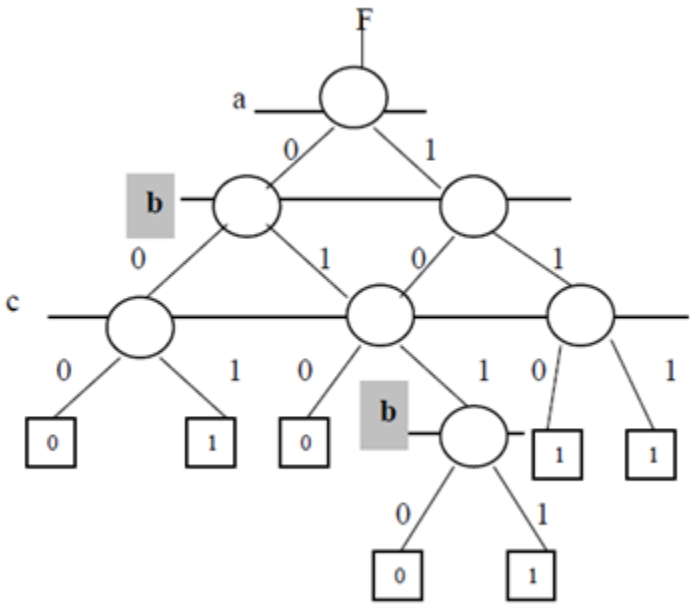


Figure 5. Shannon lattice circuit for the non-symmetric function: $F = a \cdot b + a' \cdot c$.

One can note that without the repetition of variable(s) (e.g., variable *b* in Figure 5) *F* cannot be produced by any 2D lattice circuit. All internal nodes in Figure 5 are 2-to-1 multiplexers (i.e., selectors). In Figure 5, if one multiplies each leaf value, from left to right, with *all* possible bottom-up paths (from the leaves to the root *F*) and add them over Boolean algebra then one obtains the required function *F* (i.e., the root) as follows:

$F = (0 \cdot c' \cdot b' \cdot a') + (1 \cdot c \cdot b' \cdot a') + (0 \cdot c' \cdot b \cdot a') + (0 \cdot b' \cdot c \cdot b \cdot a') + (1 \cdot b \cdot c \cdot b \cdot a') + (1 \cdot c' \cdot b \cdot a) + (1 \cdot c \cdot b \cdot a) = (1 \cdot c \cdot b' \cdot a') + (1 \cdot b \cdot c \cdot b \cdot a') + (1 \cdot c' \cdot b \cdot a) + (1 \cdot c \cdot b \cdot a) = a' \cdot c + a \cdot b.$

One can observe that in order to represent the non-symmetric function in Example 1 in the 2D lattice circuit, variable *b* is repeated, where the nodes in Figure 5 are Shannon nodes, which are merely two-input one-output multiplexers, whose output goes in two directions, with the set of variables {*a*, *b*, *c*} operate as control signals [2 - 5].

The results from this sub-section will be generalized to ternary logic in sub-section 2.3, and thus from 2D space to 3D space. It is important here to prove that the repetition of variables will have an end in the process of the symmetrization of the non-symmetric functions. An intuitive proof is as follows: For totally symmetric functions the number of variables are equal to the number of levels of the lattice circuit, as there is no need to repeat variables, and as it is known that by the repetition of variables every non-symmetric function is symmetrized [2 - 5], then this must result in definite number of levels in the corresponding lattice circuit and as a consequence in certain

number of total variables (repeated and non-repeated) that will result in the termination of the process of symmetrization.

2.3. Regular 3D Lattice Circuits

The concept of 2D lattice circuits that was presented in sub-section 2.2 can be generalized to include the case of 3D lattice circuits. Since the most natural way to think about a binary lattice circuit is the 2D 4-neighbor lattice circuit that was shown in Figure 4a, one can extend the same idea to utilize the full 3D space in the case of ternary lattices. Such lattices represent 3D 6-neighbor lattice circuits (cf. Figures 9 and 10).

Although regular lattices can be realized in the 3D space for the third Galois radix while maintaining their full regularity, they are unrealizable for radices higher than three [2 - 5]. Higher dimensionality lattices can be implemented in 3D space but on the expense of loosing the full regularity. This is because the circuit realization for the ternary case produces a regular circuit in 3D that is fully regular in terms of interconnections; *all interconnections are of the same length*. Realizing the higher dimensionality lattices in lower dimensionality space is possible but with the expense of regularity; the lattices will not be fully regular due to the uneven length of the interconnections between nodes.

As a topological concept, and as stated previously, lattice circuits can be created for two, three, four and any higher Galois radix. However, because our physical space is three-dimensional, lattice circuits, as a geometrical concept, can be realized in solid material, with all the interconnections between the cells are of the same length, only for Galois radix two (within 2D space) or Galois radix three (within 3D space). It is thus interesting to observe that the characteristic geometric regularity of the lattice circuit realization, which is observed for binary and ternary functions, will be no longer observable for quaternary and higher radix functions. Thus, the ternary lattice circuits have a unique position as highly-regular networks that can make the best use of 3D space.

Because 3D lattice circuits exist in a 3D space, a geometrical reference of coordinate systems is needed in order to be systematic in the realizations of the corresponding logic circuits. Consequently, the right-hand rule of the Cartesian coordinate system is adopted (cf. Figures 9 and 10) where each dimension in a 3D lattice circuit corresponds to a value of the corresponding control variable: value zero of the control variable propagates along the *x*-axis, value one of the control variable propagates along the *y*-axis, and value two of the control variable propagates along the *z*-axis.

Example 2. This example shows the realization of ternary 3-digit full adder using 3D lattice circuits. Ternary addition is performed utilizing the corresponding modsum operator. Figure 6 shows the modsum addition for ternary inputs.

	0	1	2
0	0	1	2
1	1	2	0
2	2	0	1

Figure 6. Ternary modsum addition.

The circuit of the ternary 3-digit full adder is shown in Figure 7.

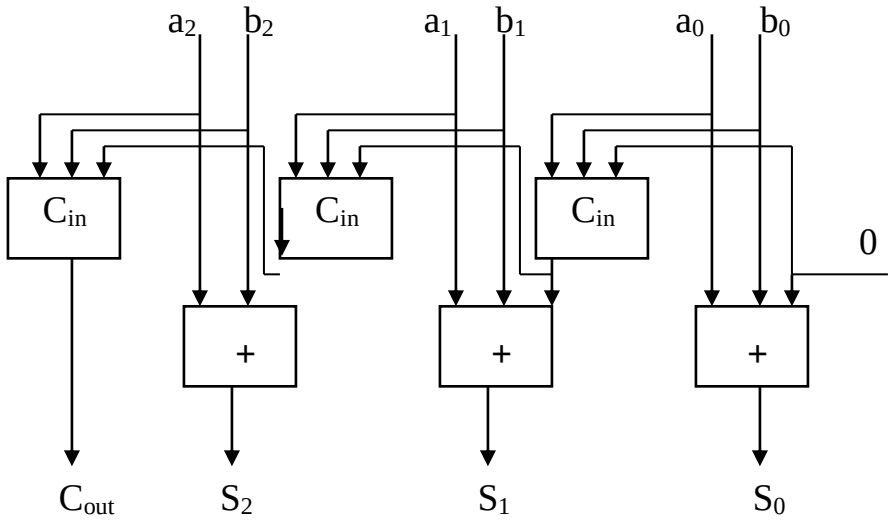


Figure 7. Ternary 3-digit full adder.

The following maps are the Sum S and the output Carry C_{out} functions that appear in the logic circuit in Figure 7 using 1-RPLs for variables a, b and c, and using the corresponding Galois field addition and multiplication.

a b \ c	0	1
0 0	0	1
0 1	1	2
0 2	2	0
1 0	1	2
1 1	2	0
1 2	0	1
2 0	2	0
2 1	0	1
2 2	1	2

F_1

(a)

a b \ c	0	1
0 0	0	0
0 1	0	0
0 2	0	1
1 0	0	0
1 1	0	1
1 2	1	1
2 0	0	1
2 1	1	1
2 2	1	1

F_2

(b)

Figure 8. Ternary maps: (a) ternary Sum: $F_1 = {}^0a^0b^1c + {}^0a^1b^0c + 2{\cdot}{}^0a^1b^1c + 2{\cdot}{}^0a^2b^0c + {}^1a^0b^0c + 2{\cdot}{}^1a^0b^1c + 2{\cdot}{}^1a^1b^0c + {}^1a^2b^1c + 2{\cdot}{}^2a^0b^0c + {}^2a^1b^1c + {}^2a^2b^0c + 2{\cdot}{}^2a^2b^1c$, and (b) ternary Carry: $F_2 = {}^0a^2b^1c + {}^1a^1b^1c + {}^1a^2b^0c + {}^1a^2b^1c + {}^2a^0b^1c + {}^2a^1b^0c + {}^2a^1b^1c + {}^2a^2b^0c + {}^2a^2b^1c$.

Figures 9 and 10 show the corresponding 3D lattice realizations of the functions in Figure 8.

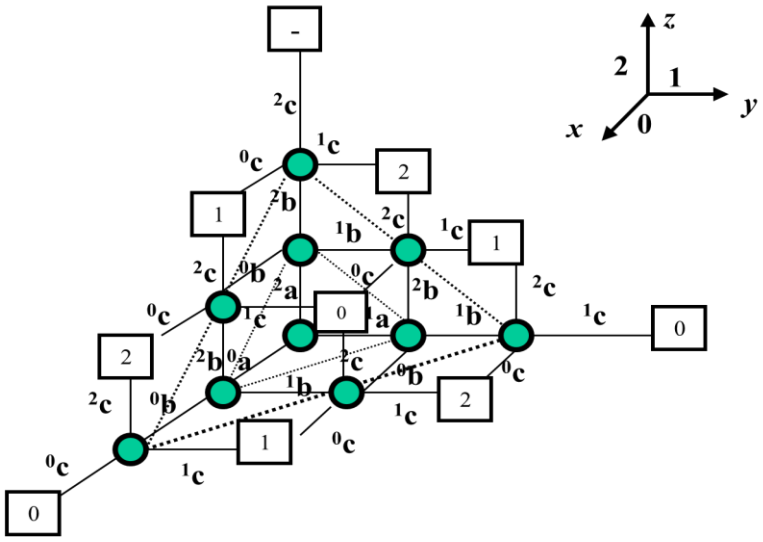


Figure 9. The Sum F_1 of the ternary 3-digit full adder, where – is a ternary don't care (i.e., 0, 1, or 2).

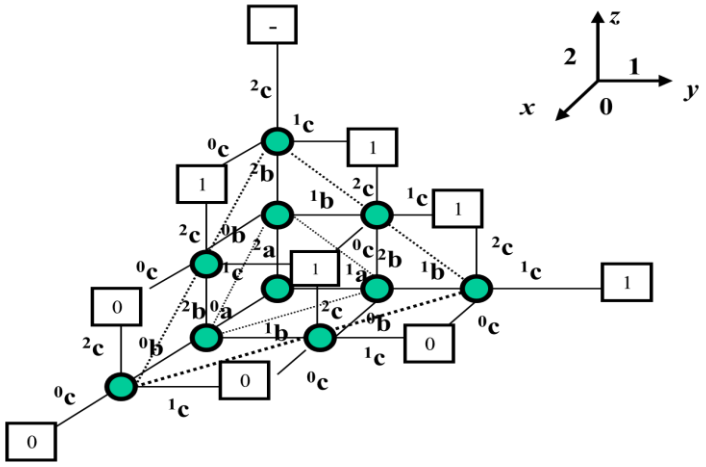


Figure 10. The Carry F_2 of the ternary 3-digit full adder, where – is a ternary don't care (i.e., 0, 1, or 2).

As observed in Example 2, Figures 9 and 10 represent a fully regular 3D lattice circuit. Each dimension corresponds to a value of the corresponding control variable: value zero of the control variable propagates along the *x*-axis, value one of the control variable propagates along the *y*-axis, and value two of the control variable propagates along the *z*-axis. Since the ternary function in Example 2 is fully symmetric [2 – 6], no variables are needed to be repeated in the corresponding lattice circuit. In 3D space, each control variable spreads in a plane to control the corresponding nodes (these parallel planes are represented using the dotted triangles in Figures 9 and 10), in contrast to the binary case where each control variable spreads in a line to control the corresponding nodes (these control signals are represented in the solid horizontal lines in Figure 4a). Each node in Figures 9 and 10 represents a three-input one-output multiplexer, whose output goes in three directions, where if one multiplies each leaf value, going counter clock wise (CCW), with all possible *out-to-in* paths (i.e., from the leaves to the root) and add them over

Galois field then one obtains the maps of F_1 and F_2, respectively. Also, one notes that internal nodes in Figures 9 and 10 lay on the corners of 3D cubes, in contrast to the binary case (cf. Figure 4) where nodes lay on the corners of 2D squares.

From Figures 9 and 10, one observes that the Sum and Carry functions are both symmetric, since there is no conflict in leaf values, and consequently there is no need to repeat variables to make the ternary functions realizable in the 3D lattice circuits. On the other hand, for ternary non-symmetric functions, at least one leaf has conflict values, and one needs to *repeat* variables to symmetrize the corresponding non-symmetric functions [2 - 6] in order to realize such functions in the corresponding regular 3D lattice circuits.

2.4. Carbon Nanotubes and Nanotips

This sub-section presents important background on Carbon-based nanotubes and nanotips and their corresponding characteristics. The presented Carbon-based nanotubes and nanotips will be utilized in building controlled-switching that will be later used for constructing the corresponding 3D lattice networks in Section 5.

2.4.1. Carbon nanotubes – based multiplexing

Carbon nanotube, which is a cylindrical graphite sheet, is geometrically formed in two distinct shapes that affect CNT characteristics: (a) straight CNT and (b) twisted CNT. The emerging CNT technology has been applied in several new implementations [9 - 10, 13 - 15, 18 - 19, 22 - 24, 27, 31, 33]. Table 1 illustrates several of the important CNT characteristics.

Table 1. Carbon nanotube characteristics.

Characteristics	Single-Walled CNT	Comparing Examples
Size	diameter of 0.6 - 1.8 nm	Electron-based beam lithography can generate lines 50 nm wide and few nm thick
Density	1.33 – 1.40 g/cm^3	Aluminum: 2.7 g/cm^3
Strength	≈ 45·10^9 Pascals	High-strength steel alloys break at ≈ 2·10^9 Pascals
Resilience	Can be bent at large angles and re-straightened without damage	Metals and carbon fibers fracture at grain boundaries
Current Capacity	≈ 1·10^9 A/cm^2	Copper: ≈ 1·10^6 A/cm^2
Field Emission	Can activate phosphors at 1 – 3 V if electrodes are spaced 1 micron apart	Molybdenum tips need ≈ 50 – 100 V/micrometer with very short lifetimes
Heat Transmission	≈ 6,000 W/m·K at room temperature	Almost pure diamond transmits ≈ 3,320 W/m·K
Thermal Stability	Stable up to 2,800 C in vacuum and 750 C in air	Metal wires in microchips melt at ≈ 600 – 1,000 C
Cost	≈ 1,500 $/g	Gold: ≈ 40 $/g
Quantum Electron Spin	Preservation is very high	Preservation is low in regular conductors
Power Consumption	Very low	Higher in metal wires
Performance (Speed)	≥ 1·10^{12} Hz nanoswitch	≥ 1,000 times as fast as µP
Electron Scattering	Almost none	Comparatively high
Energy Band Gaps	Easily tunable: almost zero like a metal, as high as a Silicon, and almost anywhere in between	No other recognized material can be adjusted so simply

One important implementation of CNT is within the construction of solid-state CNT-based devices. For example, Figure 11 shows the design of a logic inverter. This device functions in the same way as a regular CMOS-based inverter, where it uses two nanotube-based FETs [24]. In Figure 11, silicon is used as back-gate in the device, silicon dioxide is used as an insulator, gold is used as conductors (electrodes), and PMMA is utilized as a cover that protects anything beneath it from being exposed to oxygen since oxygen is used to obtain p-CNTFET from the corresponding n-CNTFET.

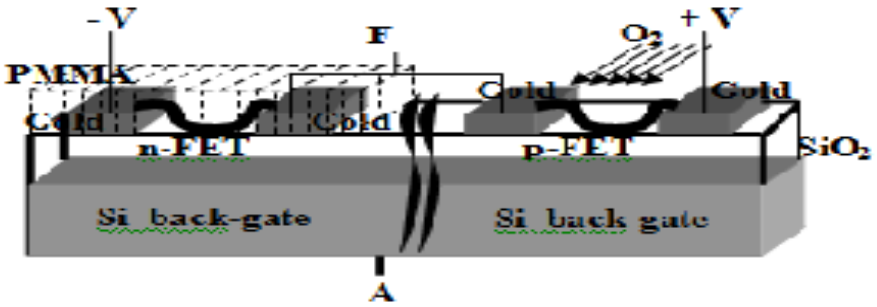


Figure 11. Inverter gate using two nanotube-based FETs.

As another important example, Figure 12 illustrates solid-state CNT-based multiplexer [10]. In Figure 12, CNT is used as a channel in the corresponding FET transistor, variable *C* is control input, selected inputs are *A* and *B*, and *F* is the output. The device operates as a controlled-switch by switching between inputs *A* and *B* depending on the specified value of control *C*.

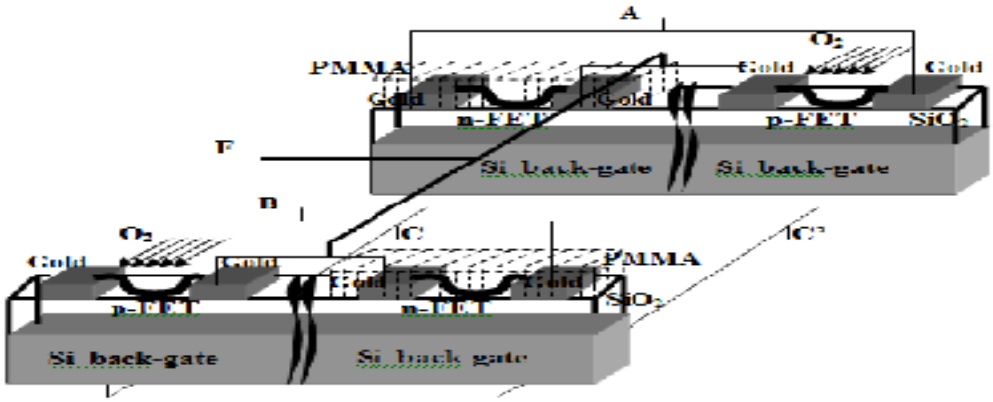


Figure 12. The device structure of solid-state inter-molecular CNT multiplexer.

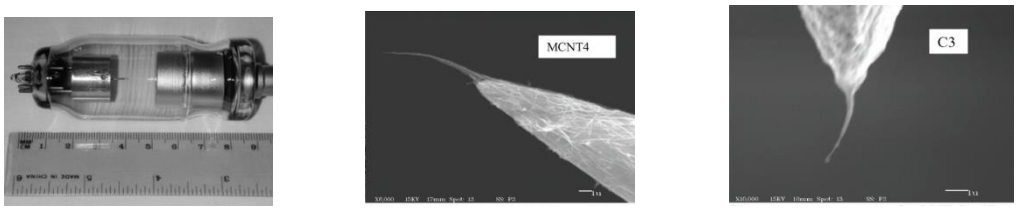
2.4.2. Carbon nanotubes - based field emitters

Field electron emission is the electron emission under the influence of the applied electric field (≈ 3 x 10^9 V/m) from a cathode surface which is highly dependent upon the material work function. The general form of Fowler-Nordheim-type formulae [25 - 26] can be obtained as follows:

$$J = \lambda_L a \varphi^{-1} F^2 EXP[\ -V_F\ b\ \varphi^{3/2} / F\ ] \qquad (5)$$

Equation (5) is used in all cases of field emission processes, where J is the local emission current density, a and b are the first and the second Fowler – Nordheim constants, v_F is the barrier

form correction factor where it accounts for the particular shape of the potential barrier model, and λ_L is the local pre-exponential correction factor where it takes into account all of the other factors that influence the emission. Factors v_F and λ_L depend on the implemented field F.
To achieve the static modeling of CNT field emitters, field emission CNTs shown in Figures 13b - 13c [14 - 16] were manufactured by Xintek, Inc. The copper anode is at the right and the CNT emitter is mounted on a tungsten wire which is attached to the copper cylinder at the left as shown in Figure 13a. Carbon nanotube M-4 has a single MWCNT as the emitter, and carbon nanotube C-3 has a single SWCNT as the emitter. The utilized CNTs were shaped in bundles of 10-30 nm diameters, but in each carbon nanotube the field emission is performed from the single CNT at the end of the bundle where the most intense electric field exists.



(a) (b) (c)

Figure 13. Field emission from CNT: (a) field emission CNTs made by Xintek, Inc. and (b) - (c) Scanning Electron Microscopy (SEM) images of CNT emitters using JEOL Ltd. model JEM 6300.

The I-V DC characteristics were measured for these CNTs, as well as a field emitter tube from Leybold Didactic GmbH, which has an etched tungsten single crystal as the emitter. The data from the DC measurements were reduced by the Fowler-Nordheim analysis which is based on the following simplified form of the Fowler-Nordheim equation:

$$J = A\,E^2\,\mathrm{e}^{(-B/E)}, \tag{6}$$

where J and E are the magnitudes of the current density and the electric field intensity, $A = 1.541 \times 10^{-6}/\Phi$, and $B = 6.831 \times 10^9\ \Phi^{3/2}$. The work function values are $\Phi = 4.5$ eV for tungsten and was set to $\Phi = 4.9$ eV for graphene. In order to apply the Fowler-Nordheim equation to the I-V DC data, the following equation was also utilized which is correct for provided CNT:

$$I = CV^2\,\mathrm{e}^{(-D/V)}. \tag{7}$$

where the following equations are used to get the equations for parameters S and R, which are utilized to characterize the used field emitters:

$$S = CD^2/AB^2, \tag{8}$$
$$R \equiv V/E = D/B, \tag{9}$$

where parameter S refers to the effective emitting area which would be the physical area of the emitter if the current density were uniform over a fixed area and zero elsewhere, and parameter R refers to the effective radius of curvature of the emitter but also includes the effects of local intensification of the electric field caused by elongation of the emitter or the reduction of the field which may be caused by shielding due to adjacent structures. The Fowler-Nordheim plots of the I-V DC data were performed as shown in Figure 14.

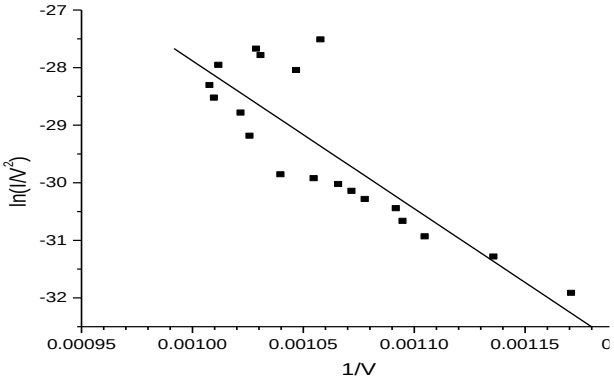


Figure 14. The Fowler-Nordheim plot for experimented CNT that have a single SWCNT as emitter.

The values of parameter *R*, which is the effective radius of emitter curvature, were found to vary within 77-110 nm for the utilized carbon nanotubes with CNT emitters. This suggests that values of the local electric field at the emitting sites were as high as 14 V/nm in some of these measurements. The Fowler-Nordheim analysis gave a value of 91 nm for the effective radius of emitter curvature in the Leybold tube, suggesting that the local electric field was as high as 5 V/nm in some of the performed measurements [14 - 16]. Current densities as high as 10^9 and 10^{12} A/m^2 may be drawn from a tungsten emitter in steady-state and pulsed operation, respectively, and the corresponding values of the applied static field are 4.7 and 8.6 V/nm which may be considered as limiting field strengths for tungsten under these applied conditions.

The Fowler-Nordheim analysis also showed that the parameter *S* varied within 81-230 nm^2 for the carbon nanotubes with CNT emitters. If the current density was uniform, this would correspond to circular emitting spots having radii of approximately 5-9 nm. The Fowler-Nordheim analysis also showed that the effective emitting area for the tungsten tip in the Leybold tube would correspond to a hemisphere with a radius of 290 nm. This result, and the value of 91 nm for the effective radius of emitter curvature in the Leybold tube, were in good agreement with the radius of 100-200 nm which was indicated by Leybold.

2.4.3. Carbon fiber nanotips - based field emitters

Because of the technological significance of carbon fibers, there has been a rising interest with regards to investigating the mechanism of field electron emission from these fibers under the effect of the implemented electric field [11, 36]. Several advantages are obtained by using carbon fibers as cathodes such as high current stability, long emitter durability, simplicity of emitter manufacturing, and offering the ability to work in a relatively high pressure environment (10^{-6} mbar). These utilized cathodes are made either from carbon fibers or from other carbon-based materials. Carbon fiber emitters can be achieved by electrolytic etching technique, where a 0.1 Molarit of sodium hydroxide solution (250 ml of distal water with 2g of NaOH) is used [11]. This etching process could be controlled by choosing a suitable etching current. The etching process is started after dipping the tip in the solution by about 2 mm and using a power supply to increase the voltage until a certain initial current of about 30 μA is reached. The chosen etching current produces sharp tips at the liquid surface which are afterwards being ultrasonically cleaned using an ultrasonic cleaning device and mounted in a standard FEM microscope with a tip screen distance of 10 mm. The anode is formed as phosphored screen to allow the recording of the corresponding emission images.

The FEM was evacuated to ultra high vacuum (UHV) conditions using rotary pump that produce pressures of about 10^{-3} mbar and a diffusion pump system in addition to a liquid nitrogen (LN2) trap that lead to finally reaching a base pressure of about 10^{-9} mbar. Then, the tips received sample conditioning which consists of an initial baking of the system for 12 hours at 170 °C, a follow up baking of the system for 12 hours, thermal relaxation for 12 hours at 170 °C, and finally cooling the sample by liquid nitrogen while studying emission behavior [10, 11]. This allowed the recording of the effects of these conditioning processes on carbon fiber tips.

To record the emission behavior, the applied voltage from extra high tension (EHT) to the tip was slowly increased until the emission current increased to about one µA, and then the voltage was slowly reduced until the emission current disappeared. Within this range, a linear Fowler-Nordheim plot is expected. Figure 15 presents the scanning electron micrograph of a produced very sharp carbon fiber tip at about 10,000 x magnification.

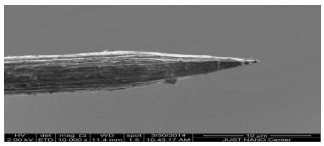


Figure 15. Scanning electron micrograph of a very sharp carbon fiber tip at 10,000 × magnification.

The apex radii of carbon fiber tips have been measured as the average of the graphically best-fitting circles [10, 11]. During the experiments, electronic emission images have been recorded by a standard digital camera to study the stability of the emission current and spatial distribution. For practical applications, stability as well as brightness are important factors for judging the quality of the used electron source. One of the very sharp carbon fiber tips has been tested during sample conditioning treatment [10, 11] where the apex radius of this tip was around 57 nm.

Figures 16 - 19 show the emission characteristics that are derived as the I-V characteristics and the corresponding Fowler-Nordheim plots. After initial baking, as was shown in Figure 16, the FN plot shows that emission current was unstable and a non-linear behavior. The follow up baking, as shown in Figure 17, shows a disconnected plot because the voltage drops from 66 V to 5.5 V where this drop is due to hysterical current.

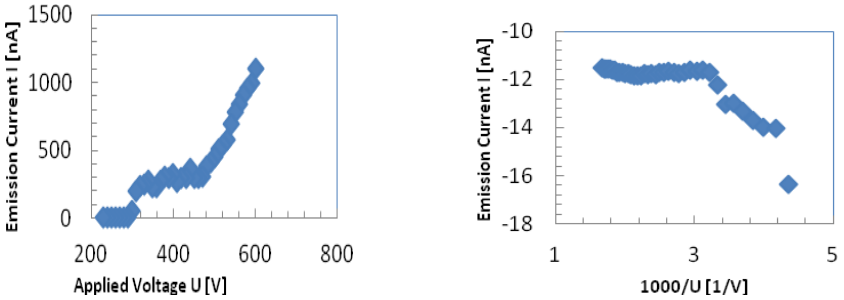


Figure 16. The I-V characteristics (left) and FN plot (right) of very sharp tip after initial baking for 12 hours at 170°C.

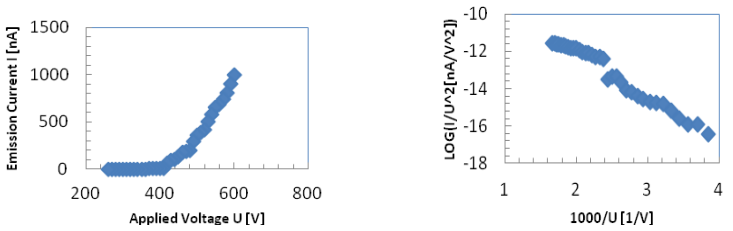


Figure 17. The I-V characteristics (left) and FN plot (right) of very sharp tip after follow-up baking for 12 hours at 170°C.

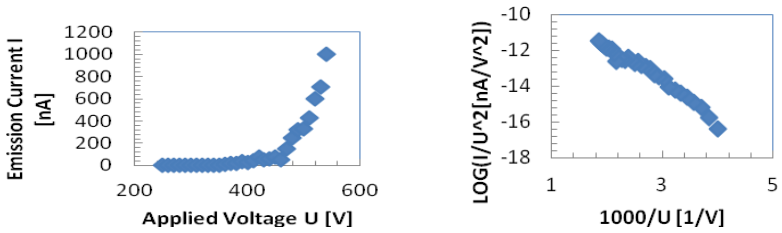


Figure 18. The I-V characteristics (left) and FN plot (right) of very sharp tip after thermal relaxation process for 12 hours.

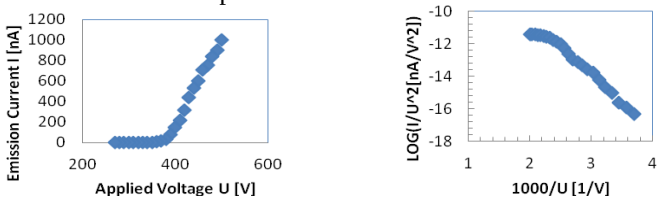


Figure 19. The I-V characteristics (left) and FN plot (right) of very sharp tip during cooling process.

As shown in Figures 18 and 19, the emission current stability becomes much higher after the corresponding sample conditioning [10, 11]. This is due to the performed process of thermal relaxation for about 12 hours and the cooling process that produce the corresponding behavior of I-V characteristics and Fowler-Nordheim plot for the utilized very sharp tip.

3. CARBON FIELD EMISSION – BASED CONTROLLED SWITCHING

This Section introduces the Carbon field emission – based controlled switches and their extension to the case of multiple-valued Galois logic.

3.1. Nano 2-to-1 Controlled Switching

Utilizing the previously presented characterizations and operations of Carbon field emission, Figure 20 introduces the Carbon field emission – based primitive that realizes the 2-to-1 controlled switch. The applied electric field intensity E, or equivalently the voltage V or work function Φ, is utilized to implement the input control signal that is used to control the electric function of the device.

The description of the operation of the Carbon field emission – based device which is shown in Figure 20b is as follows: by the implementation of the high voltage control signal (HV), the

voltage difference between the facing anode and Carbon cathodes is altered. This change will cause the Carbon cathode with (HV) control signal to be field emitting while Carbon cathode with complementary ($\overline{\overline{HV}}$) control signal to be without field emission. When the voltage difference is reversed, Carbon cathode with complementary ($\overline{\overline{HV}}$) control signal will be field emitting while Carbon cathode with (HV) control signal will be without field emission. Therefore, the device in Figure 20b realizes the function of 2-to-1 controlled switching.

The distance *d* needed between the facing anode and cathodes – as shown in the experimental results - must be around 10 mm. If this distance is not applied, beam distortion will exist that will affect the collected current at the facing anode screen.

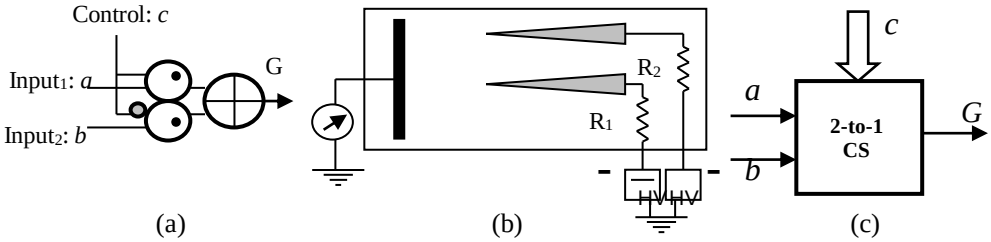


Figure 20. The implementation of the operation of 2-to-1 controlled switching using Carbon field emission: (a) 2-to-1 multiplexing, (b) controlled switching via CNT field emission, and (c) 2-to-1 multiplexer block diagram, where HV is the source with high-voltage and $\overline{\overline{HV}}$ is the complementary source.

Since the equations that relate the electric field intensity *E*, voltage *V*, distance *d*, current density *J*, and work (energy) function *Φ*, are as follows:

$$\Phi = e \cdot V, \tag{10}$$
$$V = E \cdot d, \tag{11}$$
$$d = V / E, \tag{12}$$
$$J = I / (a/\Omega) = I \cdot (\Omega/a), \tag{13}$$

where *e* is the electron charge ≅ $1.602 \cdot 10^{-19}$ C, *a* is the tip area and *Ω* is the emission angle, then the following represents the equation that models current value on the anode screen:

$$I = \left(\frac{aA}{\Omega d^2} e^{-\frac{Bd}{V}} \right) V^2 \tag{14}$$

One can note the proportionality relation between the current value *I* and both of the voltage difference *V* and tip area *a*, and the inverse relation with the emission angle *Ω*, where $A = 1.541 \times 10^{-6}/\Phi$ and $B = 6.831 \times 10^9 \, \Phi^{3/2}$. For instance, the value of the work function is $\Phi = 4.9$ eV for CNT, where the value used for electric field intensity *E* is ≥ $3 \cdot 10^9$ V/m, the distance *d* between the anode screen and CNT cathode is ≅ 10 mm, and $V \cong 3 \cdot 10^7$ V.

3.2. Nano *m*-to-1 Controlled Switching

The synthesis of *m*-to-1 controlled switching via Carbon field emission can be performed utilizing the basic two-to-one controlled switching from Figure 20b. For instance, for the case of

three-valued logic, two devices from Figure 20b are required to implement the function of 3-to-1 controlled switching as shown in Figure 21.

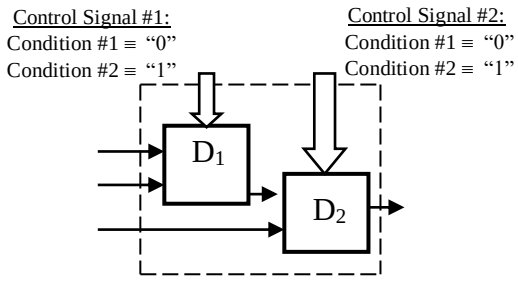


Figure 21. The three-to-one controlled switching utilizing Carbon field emission, where devices $\{D_1, D_2\}$ can be implemented using the switching device from Figure 20b.

For the more general case of *m*-valued logic, and to realize the function of an *m*-to-1 controlled switching, one requires (*m*-1) of 2-to-1 controlled switches as shown in Figure 22.

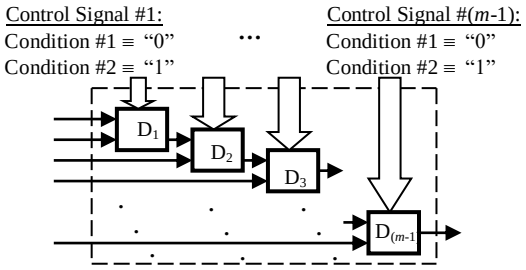
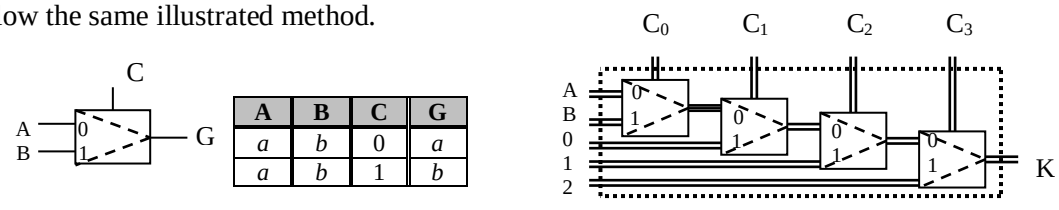


Figure 22. The realization of (*m*-to-1) controlled switching, where devices $\{D_1,..., D_{(m-1)}\}$ can be the Carbon field emission – based controlled switching from Figure 20b.

4. TERNARY PROCESSING VIA CARBON FIELD EMISSION-BASED DEVICES

The previously developed GF(3) Carbon field emission–based device will be used in this section for implementing three-valued processing. This section demonstrates the utilization of Carbon-based controlled switching for the ternary case, but implementations for higher Galois radices follow the same illustrated method.



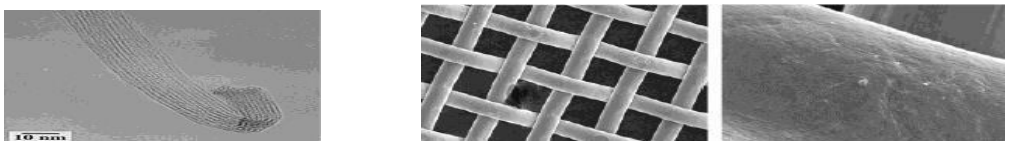
A	B	C	G
a	*b*	0	*a*
a	*b*	1	*b*

(a) (b)

Figure 23. The Carbon - based implementation of Galois arithmetic operations: (a) controlled switch that can be implemented using the device from Figure 20b, and (b) circuit that uses controlled-switching to implement GF(3) addition and multiplication tables.

Figure 23 shows a controlled switch-based circuit that implements GF(3) addition and multiplication tables, where Figure 23a can be implemented using the 2-to-1 Carbon field

emission – based device from Figure 20b. The internal nano interconnects in Figure 23b can be implemented using CNTs as shown in Figure 24. In Figure 23b, variables $\{A, B\} \in \{0, 1, 2\}$ and inputs C_k (k = 0, 1, 2, 3) are 2-valued control variables $\in \{0, 1\}$. Note that Figure 23b implements GF(3) addition and multiplication operations by using the appropriate values of C_k that select variable inputs $\{A, B\}$ and constant inputs $\{0, 1, 2\}$. Table 2 illustrates an example for implementing the corresponding GF(3) addition and multiplication tables using Figure 23b.



(a) (b)

Figure 24. The realization of nano interconnects using CNT: (a) image from TEM of a bundle of SWCNTs catalyzed by Ni/Y mixture, and (b) developing CNT wires on catalysts, where CNT meshes are illustrated on which the metal catalyst is covered.

Table 2. An example for the implementation of GF(3) addition and multiplication tables using Figure 23b, where + means GF(3) addition, * means GF(3) multiplication, C_k (+) means that control variable C_k implements the ternary addition operation, and C_k (*) means that control variable C_k implements the ternary multiplication operation.

A	B	C_0 (+)	C_1 (+)	C_2 (+)	C_3 (+)	C_0 (*)	C_1 (*)	C_2 (*)	C_3 (*)	+	*
0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0
0	2	1	0	0	0	0	0	0	0	2	0
1	0	0	0	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	0	0	0	2	1
1	2	0	1	0	0	1	0	0	0	0	2
2	0	0	0	0	0	1	0	0	0	2	0
2	1	0	1	0	0	0	0	0	0	0	2
2	2	0	0	1	0	0	0	1	0	1	1

Example 3 shows the system-level design of an Arithmetic and Logic Unit (ALU) circuit by illustrating the implementation of a 2-digit multiplier using the introduced Carbon field emission based devices, where the circuit in Figure 23b can be used in the system design where GF(3) addition and multiplication operations are applied.

Example 3. For a 2-digit m-valued multiplication performed using mod-multiplication, Figure 25 shows maps for the ternary multiplication and carry out functions, and Figure 26 shows the corresponding 3-valued circuit realization. The corresponding GF(3) addition and multiplication operations in Figure 26 can be implemented using Table 2 that specifies input values to the circuit in Figure 23b.

x / y	0	1	2
0	0	0	0
1	0	1	2
2	0	2	1

(a)

x / y	0	1	2
0	0	0	0
1	0	0	0
2	0	0	1

(b)

Figure 25. Ternary multiplication for ternary 2-digit multiplier: (a) multiply and (b) carry out.

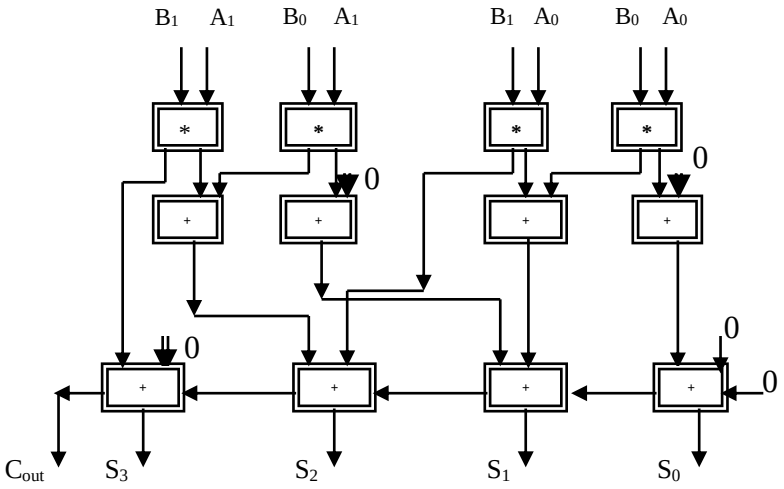


Figure 26. Circuit of a ternary 2-digit multiplier.

5. CONCURRENT 3D LATTICE PROCESSING VIA CARBON FIELD - EMISSION MULTIPLEXING

This section introduces the synthesis of 3-valued Galois functions using Carbon field emission – based 3D lattice networks utilizing the method shown in Figure 27. In this method, mapping 3-valued functions into the 3D lattice network can be achieved using either of the following two functional forms: (1) the function *expression form* directly through the RPL-based decomposition, or (2) using the *tabular form* of the corresponding 3-valued function.

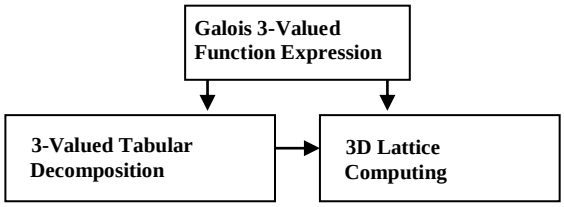


Figure 27. Utilized method to realize 3-valued Galois logic by using function decompositions.

Example 4 shows the realization of a ternary non-symmetric function in a 3D lattice through the repetition of variables and utilizing the synthesis scheme from Figure 27, where in general the operations performed in each nano node in the 3D lattice network can be implemented using the nano circuit from the Figure 23b and using specified input values from Table 2.

Example 4. For the non-symmetric two-variable 3-valued function $F = ab + a'b''$ shown in Figure 28, and by adopting the right-hand rule of the Cartesian coordinate system, Figure 29 illustrates the 3D logic circuit to implement such non-symmetric function. In Figure 29, if one multiplies each leaf value, going counter clock wise (CCW), with all possible *out-to-in* paths (i.e., from the leaves to the root) and add them over Galois field then one obtains the corresponding map, where $\{{}^0a, {}^1a, {}^2a\}$ are the zero, first, and second polarities of the 1-RPL of variable a, $\{{}^0b,$

^1b, ^2b} are the zero, first, and second polarities of the 1-RPL of variable *b*, and variables *a* and *b* can take any value in the set {0, 1, 2}.

a \ b	0	1	2
0	2	0	1
1	1	1	1
2	0	2	1

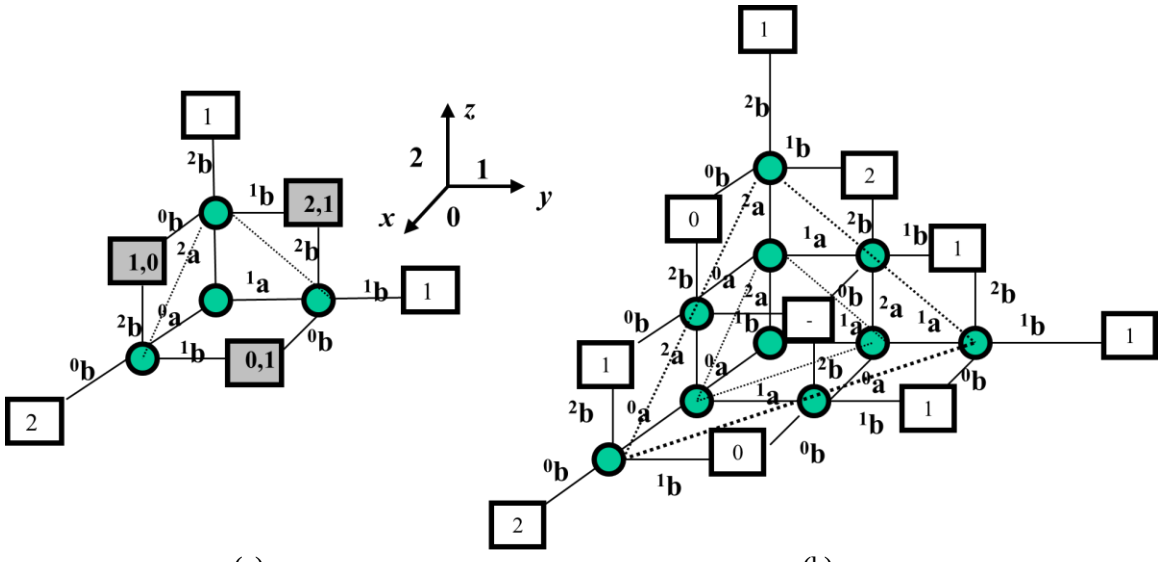
F = ab + a'b"

(a)

aa \ b	0	1	2	
00	2	0	1	
01	-	-	-	
02	-	-	-	
10	-	-	-	
11	1	1	1	
12	-	-	-	
20	-	-	-	
21	-	-	-	
22	0	2	1	F

(b)

Figure 28. Symmetrization of ternary functions: (a) Ternary non-symmetric function, and (b) the corresponding symmetrization by the repetition of variable *a*, where *a*' represents a single shift to the value of the variable *a*, and *b*" represents double shifts to the value of variable *b*.



(a) (b)

Figure 29. Regular nano-based 3D lattice networks: (a) 3D lattice circuit that corresponds to Figure 28a with conflicting leaves (in dark boxes), and (b) the final 3D lattice circuit that corresponds to Figure 28b with non-conflicting leaves.

As mentioned previously, and in general for the corresponding three-valued Shannon and Davio lattice networks, the operations performed in each nano node in the resulting 3D lattice networks can be implemented using the nano circuit from Figure 23b and by utilizing the corresponding specified input values from Table 2.

The resulting synthesized 3D lattice networks (e.g. Figure 29) have the characteristics of the full utilization of regularity and thus compactness in 3D space, ease of manufacturability due to the existence of high regularity, the relative ease of testability and the corresponding repair when fault occurrence, and the lower power consumption due to (1) the use of only local interconnects and (2) the use of low-power carbon-based nano switches.

6. CONCLUSIONS AND FUTURE WORK

In this article, the synthesis and operation of 3D lattice networks for the implementation of general three-valued Galois functions using carbon field emission – based nano switching devices is introduced.

Regular 3D lattice circuits generalize the concept of 2D 4-neighbor lattice circuits into 3D 6-neighbor lattice circuits. Lattice circuits possess a very important property of high regularity, which is useful in many applications including fault-related issues of (1) fault testing, (2) fault localization and (3) fault self-repair. Other advantages of the 3D lattice circuits include (a) no need for 3D layout routing and placement analogously to the 2D case, and (b) regularity that leads to comparable ease of manufacturability. The 3D lattice circuits can be especially well suited for future 3D based technologies, where the intrinsic physical delay of the irregular and lengthy interconnections limits the device performance in the form of high power consumption and high delay in the interconnects especially at high frequencies.

The resulting 3D lattice networks in this article have the characteristics of the utilization of full regularity and thus high compactness in 3D space, ease of manufacturability due to the existence of high regularity, the relative ease of testability and the corresponding repair, and the lower power consumption due to the use of only local interconnects and the utilization of low-power carbon-based nano switches.

Future work will include items such as the fabrication and testing of the full system-level nano-switching 3D lattice networks for real-time signal processing applications.

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