ANALYTICAL AND NUMERICAL MODELING OF V_{TH} AND S FOR NEW CG MOSFET STRUCTURE

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ABSTRACT

In this work, we study analytical model such threshold voltage (V_{TH}) and Subthreshold swing (SS) for a new Surrounding Gate MOSFET. This new SG-MOSFET is composed of Dual-metal Gate (DMG) M_1 and M_2 with different work function, Graded Channel (GC) whose the doping is higher near the source side than the drain side and Dual Oxide Thickness (DOT). Analytical model for V_{TH} and SS are developed by solving 2D Poisson equation using parabolic approximation method. Results for new device are compared to those obtained by numerical simulation and have been found to be in good agreement. Comparative study between (DMG-GC-DOT) SG MOSFET and with different device engineering shows that the new structure provides improved electron transport and reduced short channel effects (SCE).

KEYWORDS

Surrounding gate MOSFET, Dual Oxide Thickness (DOT), Threshold voltage, Subthreshold swing, Short channel effects.

1. INTRODUCTION

With the decrease of the length of the channel, short-channel effects (SCE) impose a physical limit on the ultimate performance of traditional planar metal-oxide-semiconductor field effect transistors (MOSFETs) [1]. Over the past few years, various alternative structures have been proposed to address these gaps, among them surrounding cylindrical MOSFET gate (SG) offers a better control of the SCE, and is regarded as one of the devices of the most promising [2]. In addition, SG MOSFET can be used for the construction of integrated circuits to very high density for its dimensions extremely reduced [3].

New structures are proposed incorporating dual-material gate (DMG), graded channel (GC) and dual layer oxide (DOT) to strengthen the immunity against the effects of short canals (SCE), such as the threshold voltage, and Subthreshold Swing (SS) degradation, and to provide choice more realistic for the process of MOSFET.

Dual-material gate (DMG) structure using two metals with different work functions provides a step in the surface potential profile [4, 5], the electric field peak near the drain is lowered considerably. In addition, the dual-material gate achieves simultaneous suppression of SCE, and the performance improvement is dependent on the work function difference [6]. The structure of GC constitutes an excellent immunity despite the SCEs [7], with doping near the side of the source is high and low doping near the side of the drain. The use of two oxides thickness (DOT) in the dielectric oxide has became an attractive solution to reduce the short effects of channel [8].
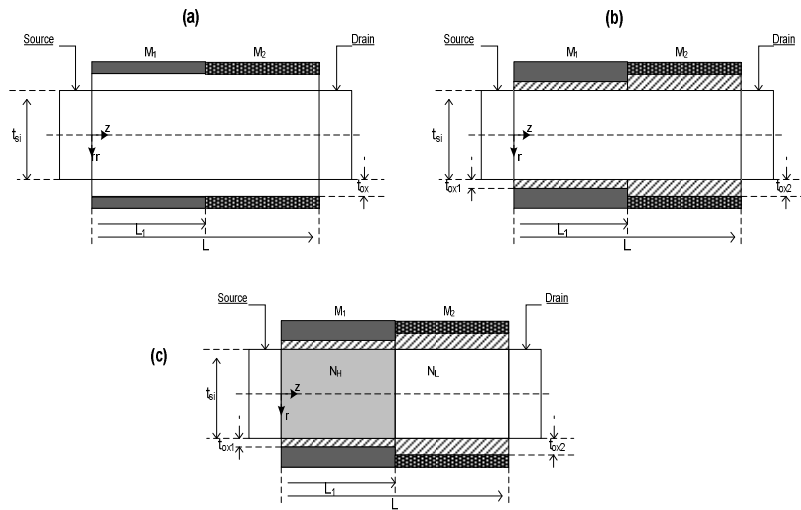
Figure 1. Cross-sectional views of various device design engineering on SG MOSFET. (a) DMG, (b) DMG-DOT, (c) DMG–GC–DOT

In this study, a new device structure as Dual Material Graded Channel Dual Oxide Thickness Surrounding Gate (DMG-GC-DOT) MOSFET is suggested as shown in Figure 1, which the gates has two metal (M1 and M2) with different work functions, an oxide structure with two different layers oxide t_{ox1} and t_{ox2} and a graded channel with two different doping (N_H and N_L) (H, high; L, low).

By solving 2D Poisson equation using parabolic approximation method, the expressions for surface potential, electric field, and threshold voltage are derived [9]. Subsequently, using device simulation and employing the analytical models [10], the reduction of SCE in DMG-GC-DOT MOSFET is presented. The results obtained are compared to results for (DMG) and (DMG-DOT) SG MOSFET. Also the analytical model results are verified by comparing them with the simulated results obtained from the numerical simulation.

2. MODEL DERIVATION

In our new structure (DMG-GC-DOT) MOSFET, as shown in figure 1(c), the channel can be divided in two parts the lengths of the two metal M_1 and M_2 are L_1 and $L_2=L-L_1$ respectively, the doping concentration N_H in the halo region (L_1) is higher than N_L in the rest of the channel ($L_2=L-L_1$) and the thickness oxide t_{ox1} in the rest of the channel in region L_1 is large than t_{ox2} in region $L_2=L-L_1$.

Analytical and numerical models of threshold voltage and subthreshold swing for DMG-GC-DOT MOSFET are compared to those for DMG, and DMG-DOT MOSFET.

2.1. SURFACE POTENTIAL MODEL

The surface potential and electric field distribution in the silicon are derived by solving 2D Poisson's equation. Presuming that the impact of fixed charges and charge carriers can be ignored on electrostatics of the channel.

The electrostatic potential $\varphi_i(r,z)$ in two regions (i=1, 2) of the channel can be written as:

$$\frac{1}{r}\frac{\partial}{\partial}\left(r\frac{\partial\varphi_i(r,z)}{\partial r}\right)+\frac{\partial^2\varphi_i(r,z)}{\partial z^2}=\frac{qN_i}{\varepsilon_{si}} \qquad 0\leq z\leq L, 0\leq r\leq\frac{t_{si}}{2}$$

$$(1)$$

Where t_{si} is the thickness of the silicon channel, ε_{si} is the dielectric constant of silicon pillar, $N_1=N_H$ and $N_2=N_L$.

The potential distribution in the two regions is assumed to be a parabolic profile in the radial direction and can be written as:

$$\varphi_i(r,z)=p_{i0}(z)+p_{i1}(z).r+p_{i2}(z).r^2$$

$$(2)$$

Where $p_{i0}(z)$, $p_{i1}(z)$, and $p_{i2}(z)$ are functions of z only.

In the centre of the silicon pillar, the electric field equal zero by symmetry

$$\left(\frac{\partial\varphi_i(r,z)}{\partial r}\right)_{r=0}=0=p_{i1}(z)$$

$$(3)$$

At the oxide-silicon interface, the electric flux is given as

$$\left(\frac{\partial\varphi_i(r,z)}{\partial r}\right)_{r=\frac{t_{si}}{2}}=\frac{c_{ox_i}}{\varepsilon_{si}}\left(V_{GS}+V_{FB_i}+\varphi_{si}(z)\right)=p_{i2}(z)t_{si}$$

$$(4)$$

Where $c_{oxi}=\dfrac{2\varepsilon_{ox}}{t_{si}\ln\left(1+\dfrac{2t_{oxi}}{t_{si}}\right)}$ is the oxide capacitance of slice oxide (i=1, 2), V_{GS} is the gate to source voltage. $\varphi_i(r,z)$ is the surface potential, ε_{ox} the dielectric constant of SiO$_2$ gate oxide and t_{ox1} is the oxide layer of region L$_1$ and t_{ox2} is oxide layer of region L-L$_1$.

V_{FB_i} is The flat band voltages of the two part of regions (i=1, 2) will be different and they are presented as:

$$V_{FB_1}=\varphi_1-\varphi_{siH}, \quad V_{FB_2}=\varphi_2-\varphi_{siL}$$

$$(5)$$

Where φ_1 is the work function of M$_1$ and φ_2 is also the work function of M$_2$, and φ_{siH} and φ_{siL} the work functions of the region L$_1$ and the rest of silicon pillar, respectively.

By using the boundary conditions, the Poisson equation in the two parts of regions is resolved, and is reduced as following:

$$\frac{\partial^2 \varphi_{si}(z)}{\partial z^2} - \lambda_i^2 \varphi_{si}(z) = D_i \qquad \text{i=1, 2}$$

(6)

Where $\lambda_i = \sqrt{4c_{oxi}/\varepsilon_{si}t_{si}}$ is characteristic length and $D_i = \frac{qN_i}{\varepsilon_{si}} - \lambda_i^2(V_{GS} - V_{FBi})$

At the source end, the potential is $\varphi_1(0,0) = V_{bi1}$, where V_{bi1} is the built in potential

$V_{bi1} = V_t \ln\left(\frac{N_H N_d}{N_i^2}\right)$.

At the drain end, the potential is $\varphi_2(0,L) = V_{bi2} + V_{ds}$, Where L is the device channel length,

V_{DS} is drain to source voltage and $V_{bi2} = V_t \ln\left(\frac{N_L N_d}{N_i^2}\right)$.

The general solution for the surface potential has the form:

$$\varphi_{si}(z) = A_i \exp(-\lambda_i z) + B_i \exp(\lambda_i z) - \frac{D_i}{\lambda_i^2}$$

(7)

Using boundary conditions, the coefficients A_i and B_i (i = 1, 2) can be determined as:

$$A_1 = V_{bi_1} + \frac{D_1}{\lambda_1^2} - B_1$$

(8)

$$A_2 = \left(\left(V_{bi_2} + V_{ds} + \frac{D_2}{\lambda_2^2}\right) - B_2 \exp(\lambda_2 L)\right)\exp(\lambda_2 L)$$

(9)

$$B_2 = \frac{U_2}{U_0}, \ B_1 = \frac{U_1}{U_0}, \ U_2 = a_0 C_2 - c_0 C_1, \ U_1 = d_0 C_1 - b_0 C_2, \ U_0 = a_0 d_0 - b_0 c_0$$

(10)

$$C_1 = \left(V_{bi_2} + V_{ds} + \frac{D_2}{\lambda_2^2}\right)\exp(-\lambda_2 L_1) - \left(V_{bi_1} + \frac{D_1}{\lambda_1^2}\right)\exp(-\lambda_2 L)\exp(-\lambda_1 L_1)$$

$$+ \left(\frac{D_1}{\lambda_1^2} - \frac{D_2}{\lambda_2^2}\right)\exp(-\lambda_2 L)$$

(11)

$$C_2 = -\lambda_2\left(V_{bi_2} + V_{ds} + \frac{D_2}{\lambda_2^2}\right)\exp(-\lambda_2 L_1) + \lambda_1\left(V_{bi_1} + \frac{D_1}{\lambda_1^2}\right)\exp(-\lambda_2 L)\exp(-\lambda_1 L_1)$$

(12)

The differentiation of surface potential is carried out along the channel to get the distribution of the Electric Field disposed by:

$$E_i(z) = -A_i \lambda_i \exp(-\lambda_i z) + B_i \lambda_i \exp(\lambda_i z) \qquad 0 \le z \le L \quad \text{i=1, 2}$$

(13)

2.2. THRESHOLD VOLTAGE MODEL

In the structure which has two material gates, the position of the minimum surface potential is always located under the gate material having higher work function (M_1). Accordingly, the derivative of the expression of surface potential under M_1 to zero, the position of the minimum surface potential can be found. By equating $\dfrac{d\varphi_{s1}}{dz} = 0$, we get:

$$z_{min} = \frac{1}{2\lambda}\sqrt{\frac{B_1}{A_1}}$$

(14)

By definition, the threshold voltage V_{TH} is determined as the value of V_{GS} at which the minimum surface potential is $\varphi_{si,min} = \varphi_{si}(z_{min}) = 2\varphi_B$, where φ_B is the bulk Fermi potential.

We considered the minimum surface potential in the region L_1, where the concentration of doping N_H is high (region (1)).

$\varphi_{si,min}$ can be deduced from Equation (7):

$$\varphi_{si,min} = 2\sqrt{A_1 B_1} - \frac{D_1}{\lambda_1^2}$$

(15)

The threshold voltage can be expressed as:

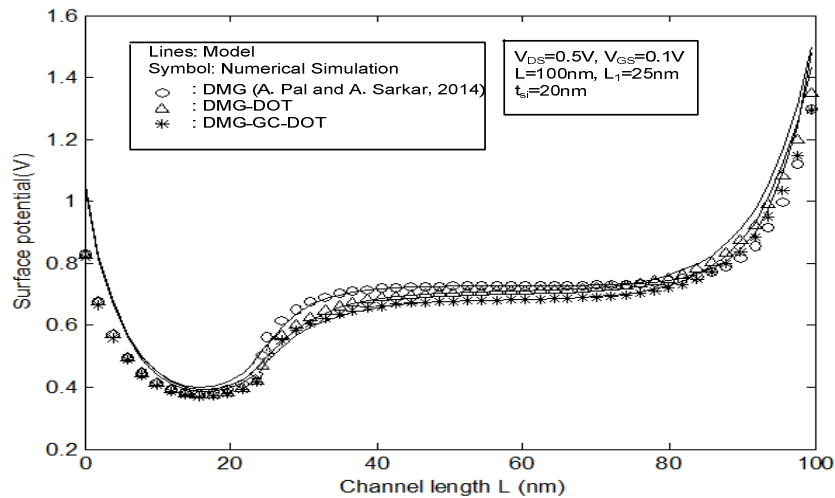$$V_{TH} = \left(-\eta + \sqrt{\eta^2 - 4\sigma\xi}\right)/2\sigma$$

(16)

Figure 2. Surface potential along the channel for DMG-GC-DOT, DMG-DOT and DMG.

Where:

$$a_0 = 2\exp(-\lambda_2 L)\sinh(\lambda_1 L_1), \quad b_0 = 2\sinh(\lambda_2(L-L_1)) \quad (17)$$

$$c_0 = 2\lambda_1\exp(-\lambda_2 L)\cosh(\lambda_1 L_1), \quad d_0 = -2\lambda_2\cosh(\lambda_2(L-L_1)) \quad (18)$$

$$U_0 = a_0 d_0 - b_0 c_0, \quad e_0 = \exp(-\lambda_1 L_1), \quad e_1 = \exp(-\lambda_2 L_1) \quad (19)$$

$$e_2 = \exp(-\lambda_2 L), \quad a_1 = \frac{(qN_{aH})}{\varepsilon_{si}\lambda_1^2} + V_{FB_1}, \quad a_2 = \frac{(qN_{aL})}{\varepsilon_{si}\lambda_2^2} + V_{FB_2} \quad (20)$$

$$b_1 = e_2 e_0(V_{bi_1} + a_1), \quad c_1 = \lambda_1 b_1 \quad (21)$$

$$b_2 = e_1(V_{ds} + V_{bi_2} + a_2), \quad c_2 = \lambda_2 b_2, \quad E = (d(e_2 e_0 - e_1) + b(\lambda_1 e_2 e_0 - \lambda_2 e_1))/U_0 \quad (22)$$

$$D = (d(b_2 - b_1 + e_2(a_1 - a_2)) + b(c_2 - c_1))/U_0, \quad \sigma = -(4E^2 + 4E + 1) \quad (23)$$

$$\eta = 4(V_{bi_1} + a_1) + E4D - 8DE + 2a_1 + 4\varphi_B$$

$$\xi = 4(V_{bi_1} + a_1)D - 4D^2 - a_1^2 - 4a_1\varphi_B - 4\varphi_B^2 \quad (24)$$

2.3. SUBTHRESHOLD SWING

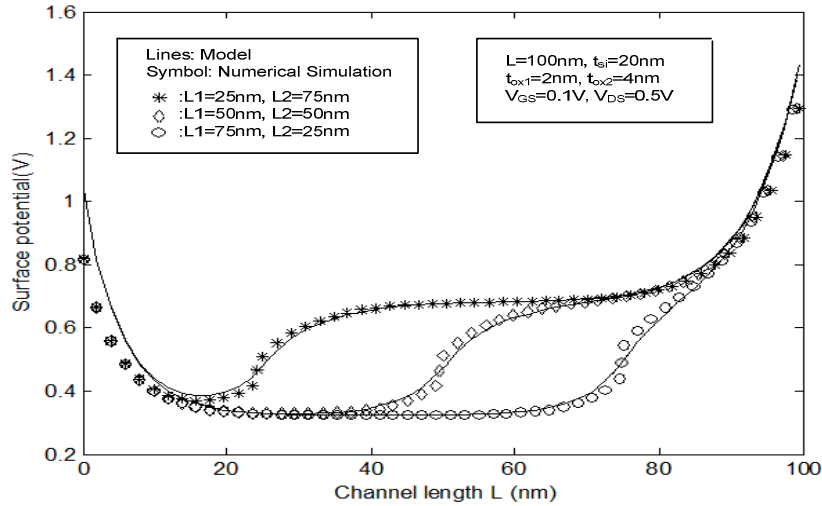In a simple approach, the subthreshold swing (SS) can be expressed as:

Figure 3. Surface potential for DMG-GC-DOT (L_1=25nm), DMG-GC-DOT (L_1=50nm) and DMG-GC-DOT (L_1=75nm) as a function of channel length with L=100nm, t_{si}=20nm, t_{ox1}=2nm, t_{ox2}=4nm, V_{GS}=0.1V and V_{DS}=0.5V

$$SS = \frac{KT}{q}\ln(10)\left(\frac{\partial\varphi_{si,min}}{\partial V_{GS}}\right)^{-1} \quad (25)$$

From Equation (15), we obtain:

$$\left(\frac{\partial \varphi_{si,min}}{\partial V_{GS}}\right) = 1 + (A_1 B_1)^{\left(\frac{-1}{2}\right)}(A_1 P_1 + B_1 P_2)$$

(26)

Where

$$P_1 = \frac{d_0}{U_0}(\exp(-(\lambda_2 L + \lambda_1 L_1)) - \exp(\lambda_2 L_1)) - \frac{b_0}{U_0}\lambda_2(\exp(-\lambda_2 L_1) - \exp(-(\lambda_2 L + \lambda_1 L_1)))$$

$$P_2 = -1 - P_1$$

3. RESULTS AND DISCUSSION

By using the derived analytical models, the performances of DMG-GC-DOT MOSFET are examined in terms of threshold voltage and subthreshold swing. To verify the proposed analytical model, surface potential distribution versus the channel length was plotted and compared with the numerical results. For analytical modeling, the doping concentrations in two regions are: $N_H = 3.10^{17} cm^{-3}$, $N_L = 4.10^{16} cm^{-3}$.
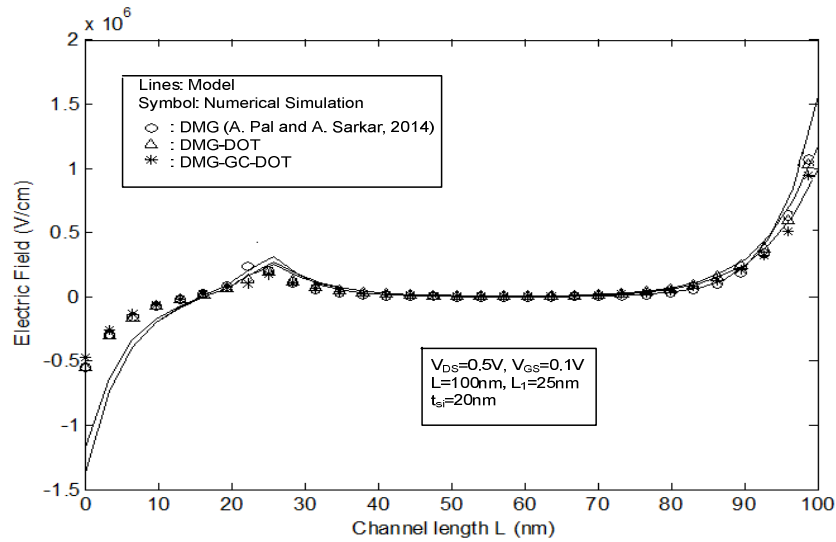

Figure 4. Variation of the Electric Field versus channel length for DMG-GC-DOT, DMG-DOT and DMG with V_{GS}=0.1V and V_{DS}=0.5V

In figure 2, we show the evolution of the surface potential for DMG-GC-DOT, DMG and DMG-DOT along the channel for L=100nm, $L_1 = 25nm$, $t_{si} = 20nm$, $t_{ox1} = 2nm$, $t_{ox2} = 4nm$, $V_{GS} = 0.1V$, $V_{DS} = 0.5V$, $N_d = 2.10^{20} cm^{-3}$, $N_L = 4.10^{16} cm^{-3}$, $\varphi_1 = 4.8$, $N_H = 3.10^{17} cm^{-3}$, and $\varphi_2 = 4.4$.

It can see according to the figure that the minimal surface potential occurs in the first region of DMG-GC-DOT. For DMG-GC-DOT, there is an additional step of potential near the limit of the

two metal gates which indicates a better control of the channel region near the source from drain voltage of DMG-GC-DOT.

Figure 3 shows the variation of surface potential for various values of L_1 by keeping the total sum length of gate constant. Consequently, there is a shift in the potential of surface, a change of step of potential along the channel with interface M_1-M_2.
Figure 4 reveals a Variation of the Electric Field. The profile involves a change of step in the electric Field located at the junction of two metals. The augment in the lateral Electric Field in the channel located under the interface of two gate materials creates an increase in the carrier transport efficiency.

Figure 5 presents the variation of the threshold voltage along the channel for DMG–GC–DOT, DMG and DMG-DOT. The figure indicates that when the channel length reduced, the threshold voltage decreases more quickly in DMG-DOT and DMG compared to DMG-GC-DOT.
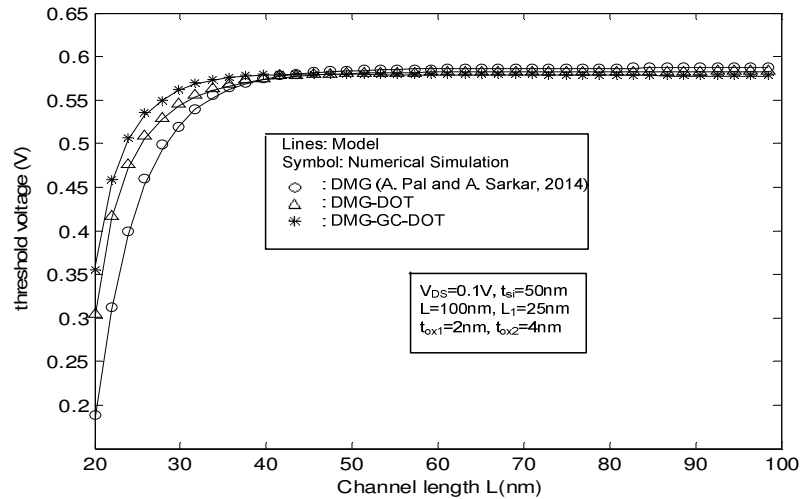

Figure 5. Threshold voltage V_{TH} as a function of channel length L for DMG–GC–DOT, DMG and DMG-DOT.

In figure 6, we plot the threshold voltage shift (ΔV_{TH}) variation versus channel length for DMG, DMG-DOT and DMG-GC-DOT MOSFETs. In Fig.6, it is evident that DMG-GC-DOT MOSFET provides higher efficacy to (ΔV_{TH}) as compared to DMG, and DMG-DOT MOSFETs.
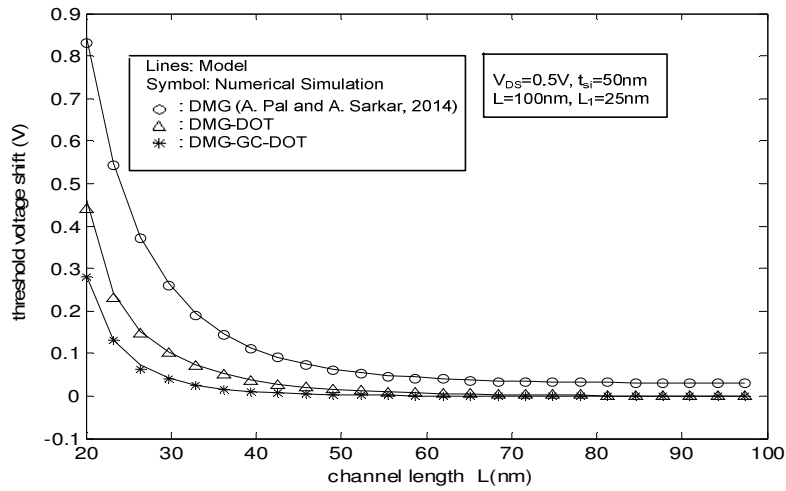
Figure 6. Threshold voltage shift versus channel length for DMG-GC-DOT, DMG and DMG-DOT MOSFET

The threshold voltage variation of DMG-GC-DOT keeps very small when the gate length is over 60 nm. This feature is very important when the device dimensions are continuously shrinking.
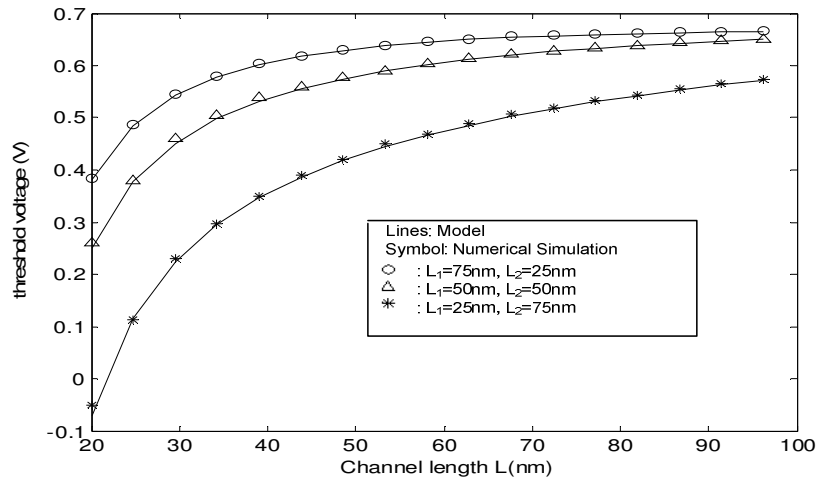

Figure 7. Effect of the gate ratio of L_1 to L_2 on threshold voltage

Figure 7 shows the smallest ratio of L_1 to L_2 degrade the threshold voltage much more than other ratios. It can be concluded that a larger ratio of control gate length to the total gate length can efficiently lower the channel potential barrier and enhance the immunity to SCE.
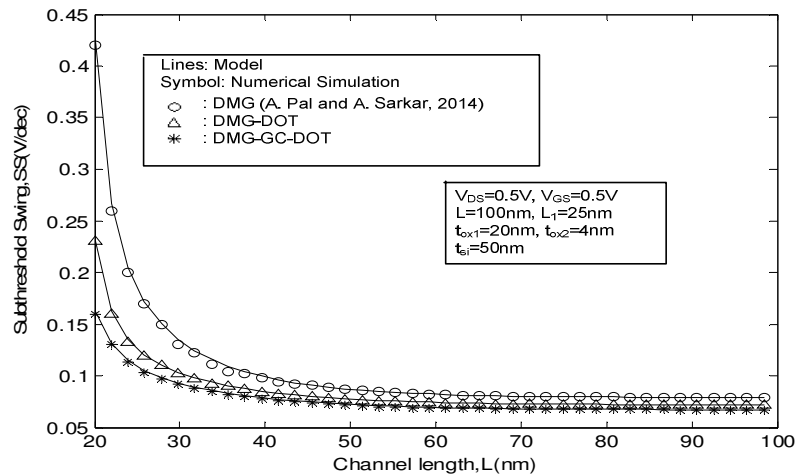
Figure 8. Subthreshold swing (SS) versus Channel length (L) for DMG-GC-DOT, DMG and DMG-DOT.

Figure 8 shows the variation of the subthreshold swing along the channel for DMG-GC-DOT, DMG and DMG-DOT. It is clear that the subthreshold reduced for device DMG-GC-DOT than DMG-DOT and DMG.

4. CONCLUSIONS

In short, two dimensional analytical models of the surface potential, electric field, and threshold voltage are derived for the new structure MOSFET (DMG-GC-DOT), by solving 2D Poisson's equation in the two channel regions. From the results obtained Physics based analytical model of the surface potential, Electric Field and threshold voltage has been developed to find the influence of gate engineering and oxide thickness on the SCEs. It has been demonstrated that DMG-GC-DOT MOSFET provides a better immunity to SCEs as compared to other structure MOSFET, so it can be concluded that the use of two oxide thickness causes better threshold-voltage, SS performance of DMG-GC-DOT devices. By using numerical simulation, the simulated results obtained coincide with The results obtained from the models. In this manner witness of the validity and the accuracy of the developed model. DMG-GC-DOT provides choice of process more flexible to optimize the execution of MOSFETs.

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