IMPROVING THE COMPENSATION CAPACITY OF INTERLINE DYNAMIC VOLTAGE RESTORER

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ABSTRACT

An interline dynamic voltage restorer (IDVR) is a novel c o m p e n s a t i o n piece of equipment for sag mitigation It is made of several dynamic voltage restorers (DVRs) with a common dc link, here each DVR is connected in series with a distribution feeder. In the sag period, active power is transferred from a feeder to other one and voltage sags with long durations can be mitigated. IDVR compensation capacity, still, depends on the load power factor, and a superior load power factor causes lower presentation of IDVR. To beat this limitation, a novel design is obtainable in this paper which facilitate sinking the load power factor under sag conditions and, so, the compensation capacity is enhanced. The proposed IDVR make use of two cascaded H-bridge multilevel converters to infuse ac voltage with lower total harmonic distortion and eliminates the necessity to low-frequency isolation transformers in one side. The validity of the planned configuration is verified by simulations in the MATLAB environment. The Proposed IDVR is applied to the 6.6kv and extension applied to the 11kv transmission lines then, observed that compensation capacity of IDVR is improved.

INDEX TERMS

Back-to-back converter, cascaded H-bridge, interline dynamic voltage restorer (IDVR), Compensation Capacity, power quality (PQ), voltage sag.

I. INTRODUCTION

These days much effort is put forward power-quality (PQ) enhancement. The voltage sag is one of the mainly significant PQ challenges for sensitive loads . Depending on the magnitude and duration of the voltage sag, the resulting damage on industrial customers are dissimilar. The increased costs of these indemnity justify the growing interest toward voltage sag mitigation techniques.

Dynamic voltage restorers (DVRs) are series-type compensation devices. It is used for voltage sag mitigation in the delivery system. This device assist to sustain the load voltage close to the insignificant value by infuseing a series voltage to the supply network. Voltage sag compensation in the DVR can be realized by simply reactive power infuseion or a amalgamation of active and reactive power. But a partial amount of voltage drop can be compensated by only reactive power infuseion; so, in most cases, it is essential to transmit active power from a dc source, such as a battery, into the ac line.

The compensation capacity in the DVR depends on the most attainable inverter voltage, the quantity of stored energy in the dc link, voltage sag duration, and its depth. relating to these factors, several control strategies and circuit topologies presented in the references to get better DVR performance. amid the a variety of compensation technique obtainable for control of a DVR, the in phase compensation technique and least energy strategy are more attractive.

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In the initial one, the infuseed voltage is in phase with the source voltage in the sag period. This technique is simple and the infuseed voltage has the negligible magnitude. In the second technique, the infuseed voltage is perpendicular to the load current and, then, the compensation technique can work with least active power. The capability of compensation with least energy is restricted when the voltage sag go beyond a certain value, which is a function of the load power factor . even though this advance method reduce the energy consumption, the long-term and deep voltage sags cannot be totally compensated just by reactive power infuseion. so, to have widespread voltage sag compensation, it is essential to utilize active and reactive power infuseion into the distribution system. In other words, if the dc link of the DVR can be energized suitably, the DVR will be able to mitigate deeper sags even with long durations.

In an interline DVR (IDVR) has been planned. The arrangement of the IDVR contains of some DVRs with a common dc link which save from harm susceptible loads beside voltage sags, while each DVR has been located in an self-regulating feeder. When one of the DVRs in the IDVR arrangement begin to compensate the voltage sag by fascinating active power from the common dc link, the other ones function in rectification mode and supply the dc link to preserve its voltage at a confident level.

In a novel control strategy for IDVR has been proposed which minimizes the rating of the power devices. Based on this strategy, a reduction in the cost and size of the IDVR without compromising its performance has been achieved.

In an IDVR has been presented and instead of bypassing the DVRs in normal conditions, the DVRs are employed to improve the displacement factor (DF) of a specific feeder. This function is achieved by active and reactive power exchange (PQ sharing) between independent feeders.
In a novel configuration has been planned which enlarge the potential of DVR to mitigate deeper voltage sags. This procedure utilizes a shunt reactance parallel with the load to diminish the load power factor in the sag condition. In other words, much deeper voltage sags can be compensated when the load power factor is minor.

As will be exposed, the presentation of the DVR (or IDVR) diminish at high power factors. For illustration, a DVR (or IDVR) with a capacitive dc link cannot compensate voltage sags which occur on the feeders with ohmic loads. To overcome this limitation, a topology is proposed in this paper which not only get better the capacity of IDVR in sag compensation at high power factors, other than get better the ability of the compensator to mitigate very deep sags at reasonable power factors. This aim is accomplish by addition a reactance in parallel with every load to diminish the power factor deliberately during the sag condition.

In this plan, voltage sag compensation is perform using an IDVR which occupy two 7-level cascaded H-bridge (CHB) converters with a common dc link in the single-phase mode. The novelist occupy the multilevel CHB converter for the first time in the IDVR arrangement since of its modular topology and its fascinating features for high-voltage and high-power applications. lastly, the legality of the planned configuration and its effectiveness is verified by simulation results.

This plan is prearranged as follows: the operating principle of IDVR is given in Section II, the compensation scheme is presented in Section III, the planned IDVR arrangement is presented in Section IV, and the control strategy is exposed in Section V. Finally, the simulation and extension results are given in Sections VI correspondingly.

II. OPERATING PRINCIPLE OF IDVR

A simple IDVR which is exposed in Fig. 1 contains of two back-to-back voltage-source converters (VSC) with a common dc link. By using this topology, it is likely to transfer active power from a feeder to other one during the sag condition and to mitigate deeper and longer voltage sags.

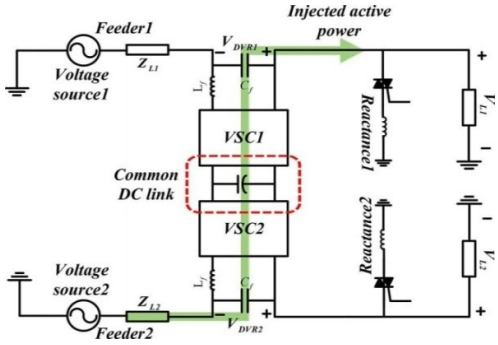


Fig. 1. Power circuit schematic of the IDVR with active power-exchanging capability.

Think about the illustration, the situation in which a voltage sag occurs in feeder1 and DVR1 initiate to compensate it. Assuming $P_{s1}$and P_{L1} are source1 and load1 active powers, then the infuse active power by DVR1 would be

$$P_{DVR1} = P_{L1} - P_{S1} \tag{1}$$

Using the demonstrated phasor diagram in Fig.2(a) can be written as

$$P_{DVR1} = V_{S1}I_{L1}\cos\varphi 1 - V_{S1}I_{L1}\cos(\varphi 1 - \propto) \tag{2}$$

Where it is obvious that load current I_{L1} is equal to source current I_{S1} due to series correlation of DVR1 with load1. When minimum energy technique is adopted for sag compensation, (2) is modified as exposed in (3) .furthermore, active power, which is drawn by DVR2 from feeder2 can be derived from Fig. 2(b) as pursue:

$$P_{DVR2} = V_{L2}I_{L2}\cos(\varphi 2 - \beta) - \cos(\varphi 2) \tag{3}$$

where infuse voltage by DVR2 during the sag period leads to a phase difference between V_{L2} andV_{S2} which is defined as β .According to (4) the maximum transferable active power is achieved when β is equal to $\varphi 2$ (phase of load2). In this condition, $\cos(\varphi 2 - \beta) = 1$ and (4) can be written as

$$P_{DVR1}^{ME} = \begin{cases} 0 & if\ V_{S1} \geq V_{L1}\cos(\mu 1) \\ V_{L1}I_{L1}\left(\cos(\mu 1) - \frac{V_{S1}}{V_{L1}}\right), & if\ V_{S1} < V_{L1}\cos(\mu 1) \end{cases} \tag{4}$$

$$P_{DVR2}^{max} = V_{L2}I_{L2}(1 - \cos(\varphi 2)) \tag{5}$$

Assuming that $S_{L1} = \rho S_{L2}$ and $V_L = I_{L1} = 1$ p.u, β can be derived from (3) and (4) it is seen that for a sag depth of less than $1 - \cos(\varphi 1)$ p.u., DVR2 is not involved with power exchange and just DVR1 compensates the sag. But for sag values greater than p.u., DVR2 starts to exchange active power from feeder2 to feeder1 and participates in the compensation. In this case, the maximum value of β is $\varphi 2$ and the maximum voltage sag that can be compensated is obtained

by

$$P_{DVR1}^{ME} \le P_{DVR2}^{max} \rightarrow V_{sag}^{max} = \frac{\rho+1}{\rho} - (\cos(\varphi 1) + \frac{1}{\rho}\cos(\varphi 2) \quad (6)$$

In other words, for voltage sags greater than p.u., IDVR is not capable of compensating it completely.

$$\beta = \begin{cases} 0 & if\ V_{sag} \le 1 - \cos(\mu 1) \\ \varphi 2 - \cos^{-1}\left(\rho\cos\varphi 1 + \cos\varphi 2 + \rho(V_{sag} - 1\right) & if\ V_{sag} \le 1 - \cos(\mu 1) \end{cases} \quad (7)$$

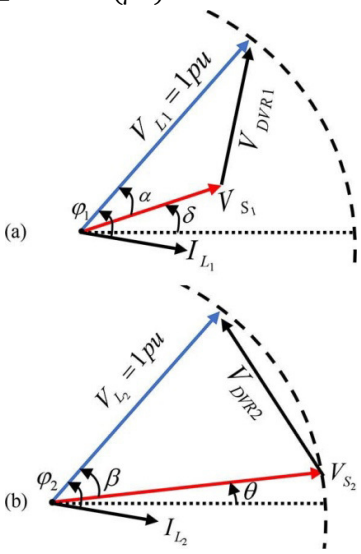


Fig. 2. Phasor diagram of the IDVR during voltage sag compensation: (a) DVR1 infuseed voltage and (b) DVR2 infuseed voltage.

III. Proposed Compensation Scheme

According to (5), P_{DVR2}^{max} depends on the load power factor and at $\cos(\varphi 2) = 1$ P_{DVR2}^{max} =0. In other words, the infuseion of active power is significantly limited at high power factors. From (7), it is also concluded that when $\cos(\varphi 1)$ and $\cos(\varphi 2) \approx 1$ then $V_{sag}^{max} \approx 0$. To overcome this problem and to improve IDVR performance, the load power factor has to be decreased at the sag period.

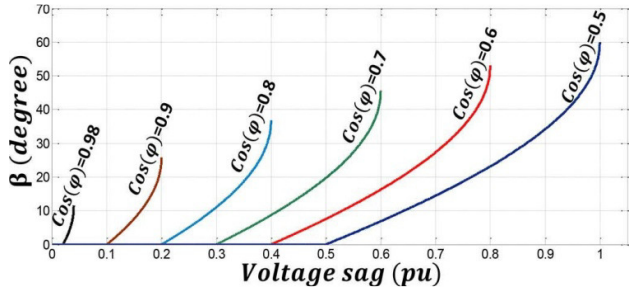


Fig. 3. Effect of load power factor on the performance of IDVR.

The remaining question is how to achieve this goal if the load power factor is higher than the expected value. To resolve this issue, a thyristor-switched fixed value reactance is paralleled to each load. Using this reactance, one can decrease the load power factor when it

is needed. In other words, when the IDVR capacity is not enough for compensation, the shunt reactances are added to the circuit. Other- wise, they are not employed in the compensation period.

To determine the value of shunt reactances, first, the value of V_{sag}^{max} should be specified in the design step. Then, according to the loading of two feeders, the value of ρ is determined. Next, the value of load power factors $\cos\varphi 1$ and $\cos\varphi 2$ should be specified in (7).

However, there is an equation with two unknowns and there is no forward rule for determining the power factors and, consequently, the value of shunt reactances. To solve this issue and obtain sensible results on the design and analysis of IDVR, hereafter, it is assumed that the loading of two feeders is equal

$$\cos(\varphi 1) = \cos(\varphi 2) = \cos\varphi \tag{8}$$

According to (7) and the aforementioned assumptions, the effect of load power factor on the IDVR performance is obtained and demonstrated in Fig. 3. It is observed that the ohmic loads cannot be compensated completely by the IDVR because no exists for these conditions. However, for loads with a lower power factor, IDVR can mitigate larger sags. For example, when the load power factor is 0.5, IDVR can compensate the entire Fig.4 illustrates the improvement of IDVR compensation capability in the presence of shunt reactances. It is seen that by applying the shunt reactances and decreasing the power factor from 0.98 to 0.8, the depth of compensation increases from 0.04 to 0.4 p.u. (A & B points).

Fig.5 shows a comparison between the compensation capability of two separate DVRs and an IDVR for different R_L/X_p ratios. The first topology consists of two independent DVRs in- stalled on feeder1 and feeder2 with capacitive dc links. To extract the corresponding curve of compensation capacity, it is assumed that the load power factor is 1,R_L=1 p.u., and the shunt impedance is X_P. Then, using (3), one can write

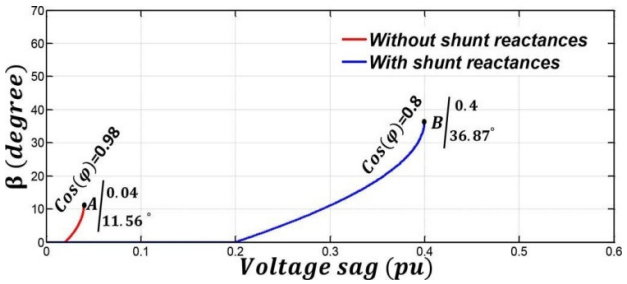


Fig. 4. IDVR performance improvement in the presence of shunt reactances.

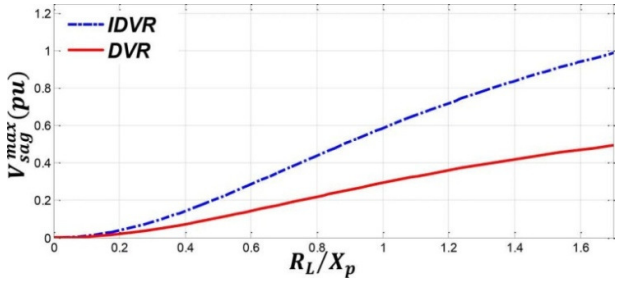


Fig. 5. Comparing the compensation capability of DVR and IDVR

which is depicted in Fig. 5 with a solid line for various R_L/X_P ratios.The second topology is an IDVR that is built from the same DVRs with a common dc link. With a similar techniqueology, one can obtain

$$V_{sag} \leq 1-\cos\varphi \tag{9}$$

$$\cos\varphi = \frac{1}{\sqrt{1+(R_L/X_P)^2}} \tag{10}$$

$$V_{sag}^{max} - 1 = \frac{1}{\sqrt{1+(R_L/X_P)^2}} \tag{11}$$

$$P_{DVR1}^{ME} \leq P_{DVR2}^{max} \rightarrow V_{sag} \leq 2 - 2\cos(\varphi) \tag{12}$$

$$V_{sag}^{max} = 2 - \frac{2}{\sqrt{1+(R_L/X_P)^2}} \tag{13}$$

Comparing (10) with (12) reveals that the compensation capability of IDVR is twice the two separate DVRs for different ratios R_L/X_P.

It is worth mentioning that adding a reactance in parallel to the load increases the IDVR rating, but it helps to compensate deep voltage sags. In other words, the cost of compensating deep voltage sag is the increase of the IDVR rating. Hence, a tradeoff

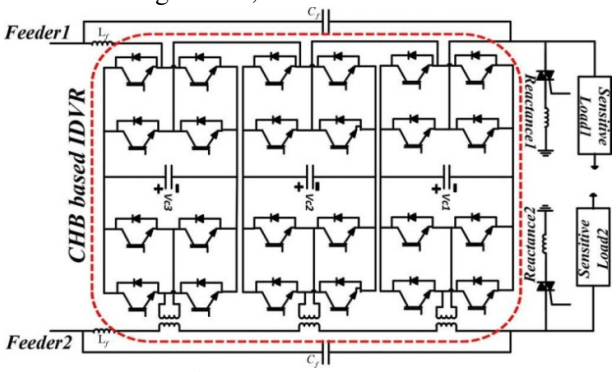


Fig. 6. Proposed IDVR structure

Therefore has to be made among the additional cost, the IDVR rating, and the maximum compensable voltage sag.The worst condition for voltage and current rating of the IDVR occurs when the loads are ohmic. Consider, for example, that the maximum IDVR current rating should not exceed γp.u. from the load nominal current, that is, 1 p.u. Then, one can Write,

$$1+\gamma = \left|\frac{1}{(R_L|jX_P)}\right| = \sqrt{1+(R_L/X_p)^2} \quad (14)$$

And by inserting (13) into (12), the maximum compensable voltage sag can be derived as

$$V_{sag}^{max} = \frac{2\gamma}{1+\gamma} \quad (15)$$

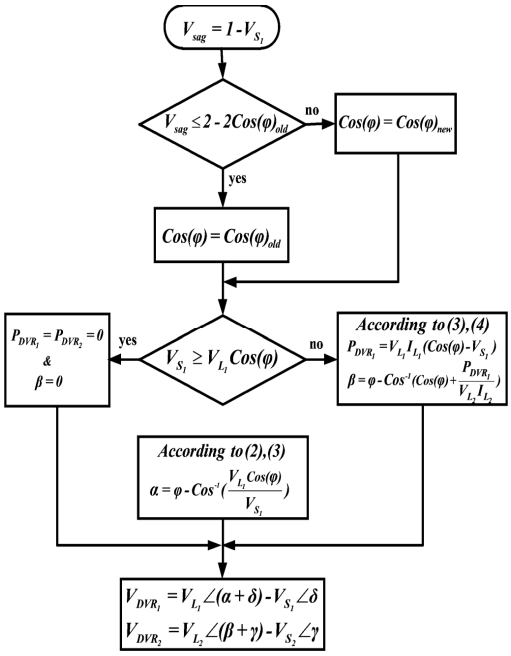


Fig.7. Flow Chart of the IDVR control System

TABLE I

PARAMETERS OF THE UTILIZED IDVR FOR SIMULATION

Parameters	Value
Modulation	Phase Shifted PWM
Switching frequency	1KHz
PFs of the loads (High PF condition)	0.98
PFs of the loads (Fairly moderate PFs)	0.8
Total DC-link voltage	7.5Kv
Rated voltage	6.351Kv
DC-link capacitor (per H-bridge)	2000uF
Shunt inductances (High PF condition)	0.23H
Shunt inductances (Fairly moderate PFs)	1.02H

Based on the phasor diagram depicted in Fig. 2(a), the DVR infuseed voltage is obtained by using the following equation:

$$V_{DVR1} = \sqrt{V_{S1}^2 + V_{L1}^2 - 2V_{S1}V_{L1}cos\alpha} \quad (16)$$

Where its maximum value affects the IDVR voltage rating. In the minimum energy compensation technique, the value of V_{DVR1} is maximum when α=φ. After adding shunt reactance and with respect to (13), φ is derived as

$$\varphi = 90 - \tan^{-1}\left(\frac{1}{\sqrt{\gamma^2+2\gamma}}\right) \quad (17)$$

Now using (14) and (16), (15) is rewritten as

$$V_{DVR1} = \sqrt{\frac{2(1+\gamma 2)}{(1+\gamma)2} - 2\left(\frac{1-\gamma}{1+\gamma}\right)\sin\left(\tan^{-1}\left(\frac{1}{\sqrt{\gamma^2+2\gamma}}\right)\right.} \quad (18)$$

Moreover, low-frequency modulation techniques and fault-tolerant algorithms can be easily applied to CHB-based IDVRs [17]–[19].

where (17) can be used to determine the voltage rating of voltage-source converters (VSCs) in the IDVR. Consequently, from the design point of view, first, γ should be determined from (14), then the X_P value and the IDVR current and voltage rating are obtained with respect to this parameter. According to the above equations, it is obvious that greater V_{sag}^{max} leads to greater γ and, therefore, a greater IDVR rating.

IV. CHB-BASED IDVR

Most of the published literature in the field of DVR and IDVR deals with VSCs realized using two-level converters. But in high-voltage and high-power applications, a CHB-based multilevel converter is a more attractive solution and its application in an IDVR is introduced in this paper. Among the multi- level topologies, the cascaded H-bridge converter is of greater interest for IDVR topology because of its modular structure, reaching medium output voltage levels using only standard low- voltage mature technology components, and higher reliability.

In a CHB converter, depending on the number of voltage levels which have to be synthesized, separate dc links are needed. In the IDVR structure, however, back-to-back connection of two CHB converters and the use of low-frequency isolation transformers in one side, distinct dc links are easily provided. Furthermore, this structure eliminates the necessity for isolation transformers on one side which leads to lower size, weight, and cost. The number of H-bridge cells in a CHB converter is chosen according to the required ac voltage and the voltage rating of power switches. Fig. 6 demonstrates a single-phase 7-level CHB-based IDVR which is used in the simulation study and experimental investigation. Although a 7-level back-to-back converter is chosen for the study in this paper, the proposed control strategy can be applied to any number of voltage levels and there is no limitation from this point of view. In other words, the generated voltage references by the control system will be synthesized by the CHB converter through well-known multilevel modulation techniques. The only issue is related to keeping voltage balance among dc-link capacitors which has been addressed in for any number of voltage levels.

In the utilized 7-level CHB converter, the dc-link voltage and current rating of each cell can be specified with respect to (13) and (17). Assuming the dc-link utilization factor is 0.85, then each cell current and its dc-link voltage must be greater than 1+γ and $V_{\mathrm{DVR}_1}/(3 \times 0.85)$, respectively.

V. IMPLEMENTATION OF CONTROL STRATEGY

As was already mentioned, the minimum energy strategy is utilized for voltage sag compensation in this paper. Based on this technique, the block diagram of the control system is exposed in Fig. 7. In this control strategy, first the magnitude of voltage sag is calculated. If the sag amplitude is greater than this value, then the shunt reactances are parallel to the loads to decrease the load power factor. Next, with respect to the equivalent power factor which is seen by the source, the DVR voltages are determined. This control system needs a fast and accurate estimation system for calculation of phase and magnitude of corresponding waveforms. Among the estimation techniques, which have been proposed in the literature , the fast Fourier transform (FFT) is the most common one and presents relatively good accuracy . In this paper, the FFT algorithm is therefore used for the estimation of $v_{s_1}(t), v_{s_2}(t), i_{L_1}(t)$ and $i_{L_2}(t)$. After estimation of these signals, the control system is able to detect voltage sags and mitigate them by producing the appropriate reference signals for the IDVR (Fig. 7).

VI .SIMULATION RESULTS

To investigate the system performance in voltage sag compensation, several simulations have been done in the SIMULINK/ MATLAB environment on a single-phase IDVR similar to that in Fig. 6. In these simulations, two shunt reactance are used for power factor reduction during the sag periods. By adding the shunt reactance, the dc-current component may occur; how- ever, if the shunt reactance is switched on at near the peak of the voltage, this component will be significantly small. The parameters of the understudy system are listed in Table I.

A. COMPENSATION AT HIGH POWER FACTORS

In this study, sag with a depth of 0.4 p.u. occurs on source1 at 0.3 s. As was already mentioned, at high power factors, the ordinary IDVR is not able to mitigate these kinds of voltage sags. However, after inserting the shunt reactances and reducing the load power factors from 0.98 to 0.8, the IDVR can compensate this voltage sag completely as can be seen in Fig. 8.

B. FAIRLY MODERATE POWER FACTORS

In this part, the power factors of both loads are reduced from 0.8 to 0.7 during the sag condition. According to (11), at this condition, the IDVR can compensate the voltage sags with the maximum depth of 0.6 p.u. Fig. 9 illustrates the IDVR operating principle when the proposed configuration is employed. It can be seen that the IDVR can successfully compensate the voltage sag and keep the load voltage at 1 p.u. provides a numerical example to compare the proposed IDVR previous study, the load power factors are reduced.

Similar to the case study in the simulation part, 40% voltage sag is applied to the voltage source1. Fig.8 shows corresponding waveforms, before and after the voltage sag. It is seen that the IDVR can compensate the voltage sag completely with the help of shunt reactance. These experimental results have been carried out only for the high power factor condition which was mentioned in the simulation study.

A) PROPOSED TECHNIQUE:

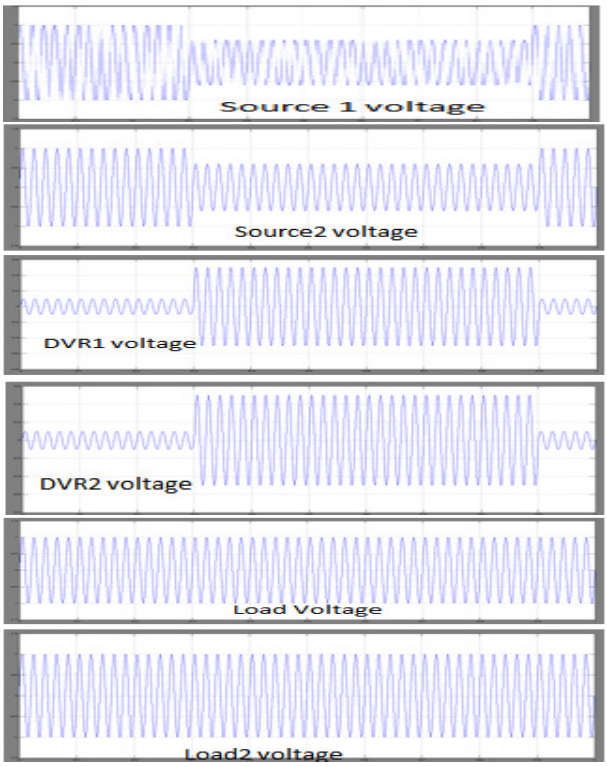
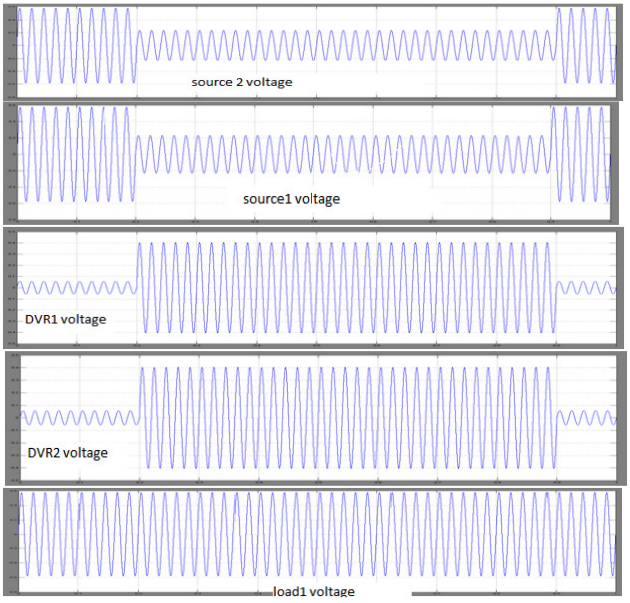


Fig. 8 Simulations results for Proposed technique in the voltage restoration function for 6.6kv transmission line.

B) EXTENSION TECHNIQUE:



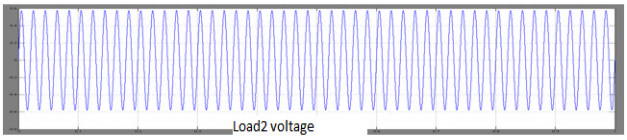


Fig.9 Simulations results for Extension technique the voltage restoration function for 11kv transmission line.

VII. CONCLUSION

In this manuscript, a novel configuration has been proposed which not only improves the compensation capacity of the IDVR at high power factors, but also increases the performance of the compensator to mitigate deep sags at fairly moderate power factors. These advantages were achieved by decreasing the load power factor during the sag condition. In this technique, the source voltages are sensed continuously and when the voltage sag is detected, the shunt reactance are switched into the circuit and decrease the load power factors to improve IDVR performance. Finally, the simulation and practical results on the CHB-based IDVR confirmed the effectiveness of the proposed configuration and control scheme.

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