DUTY CYCLE CORRECTOR USING PULSE WIDTH MODULATION

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ABSTRACT

In circuits, clocks usually play a very important role. Whenever data needs to be sampled, it is done with respect to clock signals. It uses the edges of the clock to sample the data. So, it becomes very much necessary to see to it that the clock signals are properly received specially in receiver circuits where data sampling is done, mainly in Double data rate(DDR) circuits. Due to effects such as jitter, skew, interference, device mismatches etc., duty cycle gets affected. We come up with duty cycle correctors that ensure 50% duty cycle of the clock signals. A duty cycle corrector (DCC) with analog feedback is proposed and simulated in 45nm process technology node. The duty cycle corrector operates for MHz frequency range covering the duty cycle from 35%-65%, with +/- 1.5% accuracy. The design is simple and the power consumption is 1.01mW.

KEYWORDS

DCC, Integrator, Control voltage generator, frequency range

1. INTRODUCTION

Double data rate synchronous dynamic random access memory (DDR SDRAM), makes higher data rate possible making strict control of timing on electrical data and clock signals. Duty cycle distortion is an important specification to be considered when there is minimum and maximum constraint on pulse width. One such situation is when the signal has to be sampled by clock at the receiver, during the valid data window. In such a situation, it has to be ensured that the data signal is wide enough to be sampled in the valid data window range to avoid distortions. Hence Duty Cycle Correctors (DCCs) come into picture for the purpose to correct the distorted clock signal and adjust the pulsewidth to 50%. These are of many types.

2. RELATED WORK

In [1], the paper is the combination of both analog and digital circuits, i.e it's a mixed mode technique for duty cycle correction. It uses a dual feedback loop. This design works at very high frequencies with clock jitter of around 1.62ps. It also has an accuracy rate of +/- 1%. It works on the principle of adjusting the rise and fall time of the input clock which is dependent on pull up and pull down strength of the inverter. It includes two types of correction, the first is course correction which is controlled by binary code finite state machine (FSM) which corrects the duty cycle to maximum extent by incrementing or decrementing the code that enable the inverter ladder leading to increase or decrease in the rise or fall time. Second is fine correction done by thermal code which starts working after binary duty cycle adjuster has stopped working. The advantage of this work is its good accuracy but has minimum duty cycle correction range i.e from 40-60%.Power consumption is also huge which is around 5.87mW due to its complex structure.

In [2], duty cycle corrector is being designed for applications such as software defined radios, cognitive radios etc. it uses a technique called pulsewidth modification to make the circuit to operate over a wide frequency range of 100Mhz-3.5Ghz. It makes use of an inverter whose drive strength is varied by current sources that are connected to the output. This leads to variation in the rise and fall times that are rectified by the comparator and then fed back in the loop leading to variation in the pulsewidth. This work is proved useful in terms of wide correction range of 30-70% but has huge power consumption of 20mW(including load). In [3], the paper investigates different implementation of DCC. This paper mainly highlights the pros and cons of different architectures. It claims that an analog DCC can provide wide correction range and shows little sensitivity to power supply variation in comparison to digital DCC. It also gives some key points on implementation of DCC with and without Delay locked loop(DLL). In [4], the proposed circuit calibrates the duty cycle to reduce the introduced jitter. It is an all analog feedback DCC that includes an differential amplifier to detect the duty cycle and corrects it in the loop till it nears 50%. The design scheme is robust to the process and temperature variations.1-5 GHz of correctionrange is achieved using 1.2V of supply and 3.5 mW of power consumption and very less die area. In [5], successive approximation register (SAR) based DCC is being proposed that uses a binary search algorithm to achieve fast correction of duty cycle and to support the power down mode. 6 bit SAR controller is being used along with an amplifier used for detection. The proposed architecture is prone to PVT variations and may suffer from noise etc. Power consumption is 3.2mW. In [6], an all digital duty cycle corrector is being presented. This architecture uses a time to digital converter, that acts as a duty cycle detector. It needs a DLL to align the phase skew between input and output clock. It consumes 5.6mW of power which is its drawback. In [7], an analog feedback DCC is being designed for 1-660Mhz. They have made used of pulse shrinking and stretching mechanism. In [8], an analog feedback DCC is proposed that works at 1.8V supply and corrects duty cycle from 1M -900Mhz. [9] focuses at DCC that works only at 1-2Ghz, not making it reliable for applications that work at MHz frequencies. It has two stages, where the first stage consists of two amplifiers restricted to correct the duty cycle in between 47-53% by intentionally skewing their references to 47 and 53% of VDD(supply). The second stage has an amplifier that does fine tuning to 50%. The motivation behind this work was, usage of single stage amplifier requires large gain making it sensitive to VDD, hence the author proposed this two stage structure. In [11], a synchronous all digital DCC is presented. It uses dual loop feedback, one corrects the duty cycle and other corrects the skew between input and output clock. It is limited to work between 300-600MHz with duty cycle correction range of 40-60% with huge power consumption of 18mW. In [12], proposed DCC attains the duty cycle of near to 50% for single ended signal. It uses an inverter where input clock is given to the gate of pmos and error voltage that comes from comparator is given to gate of nmos, as duty cycle corrector. But it works only at 500MHz signal. In [13], DLL is proposed along with DCC using feedback edge combiner. Here the main focus is on architectures used on SDRAMs that has DLL included to increase the data rate of the channel. It has 7.2mW of power consumption. In [14], a ring oscillator is used as duty cycle detector, that measures the average frequency by counting the number of oscillations in fixed time period. If upcount is less than downcount, duty cycle is less than 50 and vice-versa. Hence the control bits in duty cycle adjuster are incremented or decremented to achieve 50%. Thus, from all these papers it can be summarised that majority of architectures use inverter stages for duty cycle correction and amplifiers to detect the duty cycle and compare them, the difference in architecture depends on what kind of configuration or method is used to correct the duty cycle in loop, where digital DCCs use FSM, SAR, or TDC that increment or decrement the code and feed it to the inverter ladder to change the rise/fall time and analog DCCs make use of amplifiers that generate the control voltage given to the gate of nmos and pmos to vary the charging and discharging current which in turn affects the dutycycle.

3. CIRCUIT IMPLEMENTATION

The proposed DCC is an analog feedback duty cycle corrector. In the top level, there are three blocks namely duty cycle corrector that corrects the pulsewidth, duty cycle detector which detects the duty cycle error and the third block is the control voltage generator that generates the control voltage based on the error till pulsewidth reaches 50% . Figure 1 shows the top level block diagram, the input distorted clock is fed to the duty cycle corrector, and it travels through the duty cycle detector and feedback control voltage generator till it gives out the corrected output clock that is close to 50%.

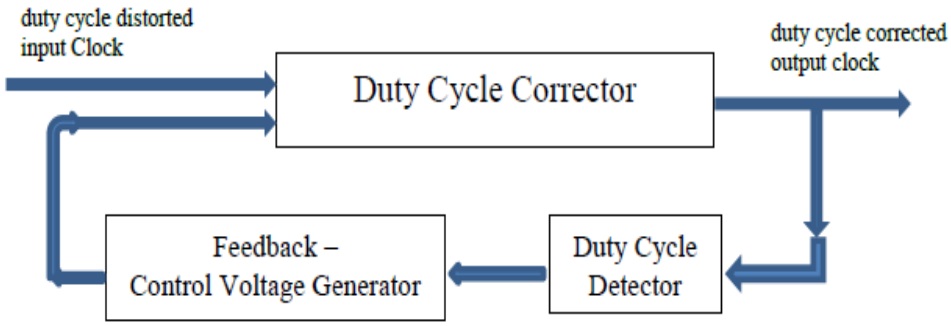

Figure 1 : DCC top level block diagram

3.1. DUTY CYCLE CORRECTOR

The first part in the top level circuit consists of a duty cycle corrector, which is nothing but the series of modified inverters that act as pulsewidth modification cells. One way to control the pulsewidth is by adding the extra two transistors to an inverter as shown in the Figure 2. This method is known as “current starving” [7]. The main purpose here is to increase or decrease the pulse width of a clock. This can be achieved by varying the rise / fall time and then using a regular inverter to sharpen the edge so that the clock edges are shifted, hence changing the pulse width.

When the control voltage (refer to first stage of Figure 2) decreases (below the midpoint, ~vdd/2), the fall time increases – since VGS of nmos transistor is lowered and risetime reduces as VGS of pmos increases (refer to Figure 7 for rise time and fall time curves) [7]. The increase in fall time (Tf) moves the vdd/2 transition point of the falling edge to delayed time and decrease in rise time (Tr) moves the vdd/2 transition point of the rising edge the left. The second stage is an inverter, designed with Voltage threshold equal to vdd/2. Since we varied the midpoint of rising and falling edges from the first stage (Figure 2) the mid point appears at different point of time and since the second inverter switches at this new point of time moving the falling edge to right and rising edge slightly to left. This in effect decrease the pulsewidth of the clock coming out of this block. In the similar way the pulsewidth gets expanded when the Vctrl increases. The gate voltages of nmos and pmos are being generated by control voltage generator discussed later. Change in width $\Delta W = t_{high\_low} - t_{low\_high}$ as shown in the Figure 3.

Modelling of delay cell:

The sizes of the mosfets MPS and MNS are chosen to provide equal rise and fall time at the mid value (~vdd/2) of the control voltage to balance the pulse shrink and stretch mechanism. The

sizing for these is such that at this control voltage, inverter made of MP1 and MP2 should starve i.e carry lesser current than they are capable of for their sizes.

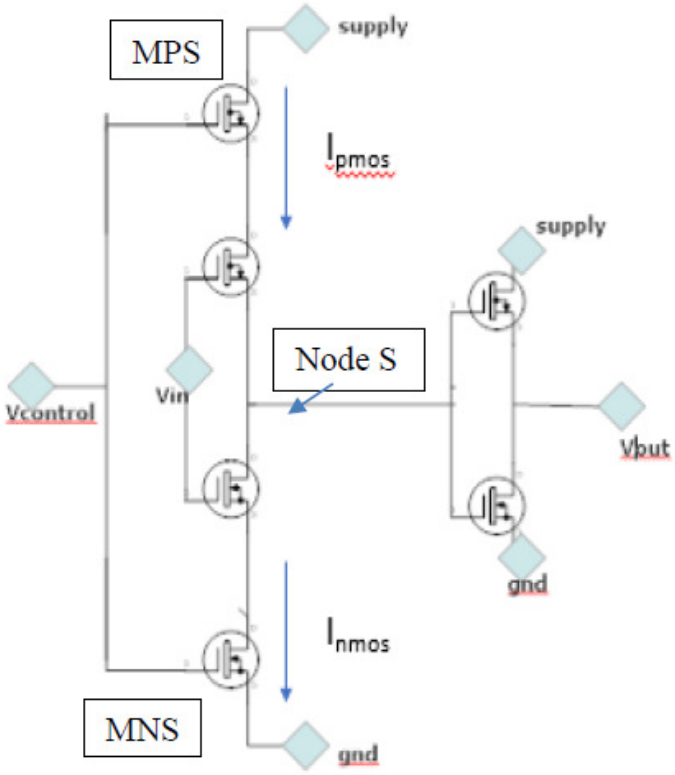

Figure 2: Schematic for delay cell/DCC

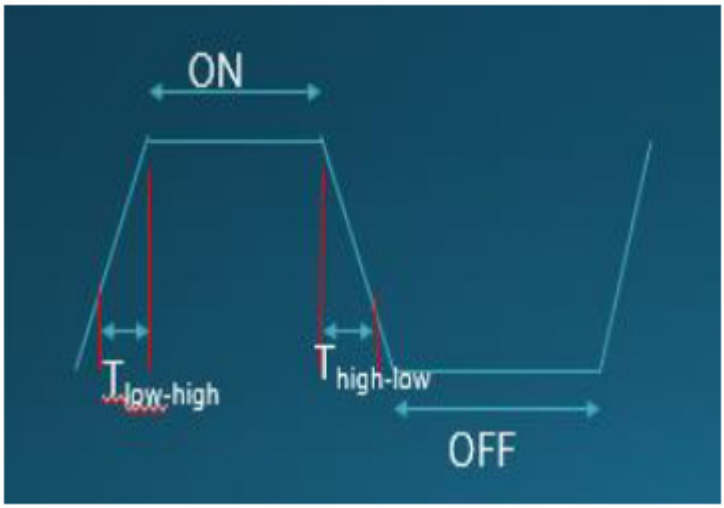

Figure 3. Change in pulse width $\Delta W = t_{high\_low} - t_{low\_high}$

Figure 4 shows the shift in edges of the clock as the control voltage changes from 0.7V to 1.1V leading to change in rise and fall times and hence the pulsewidth as explained before and from Figure 5 it can be observed that the proposed duty cycle inverter works well between 0.7-1.2 V of

Vctrl changing the duty cycle from 31.51% to 83.6%. Figure 5 is plot on how much duty cycle is achieved corresponding to the applied Vctrl when no load is considered.

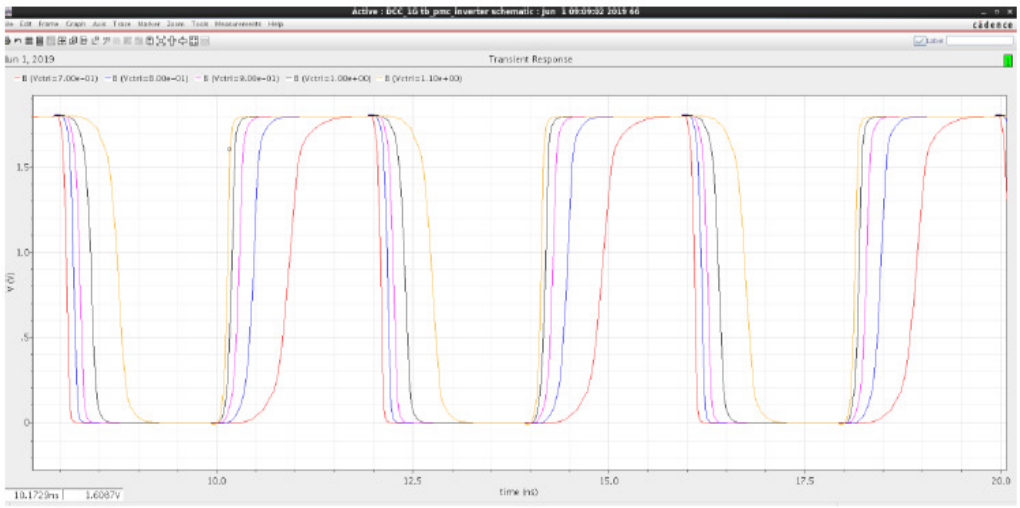

Figure 4. Shift in the edges of clock

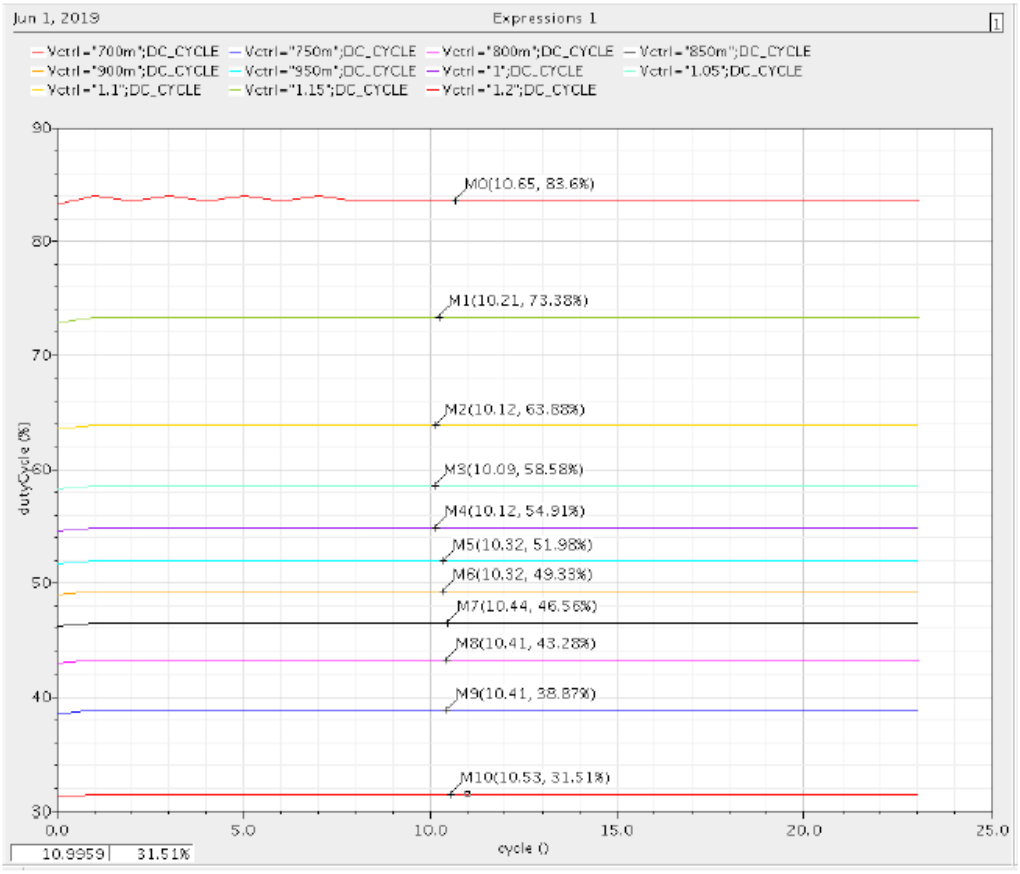

Figure 5. Variation in duty cycle with respect to control voltage.

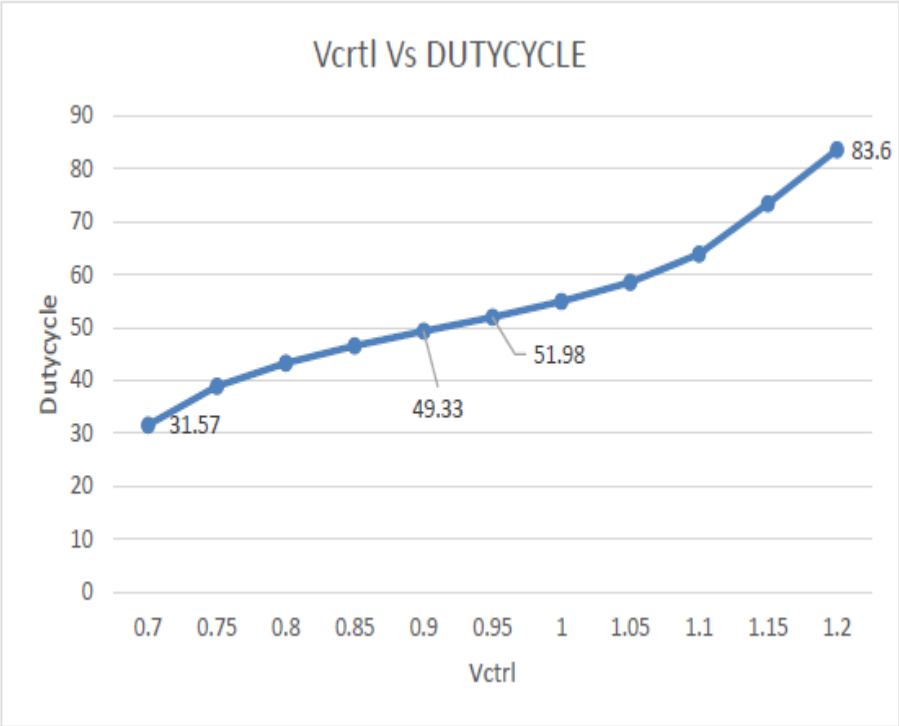

Figure 6. Vctrl Vs. Duty cycle

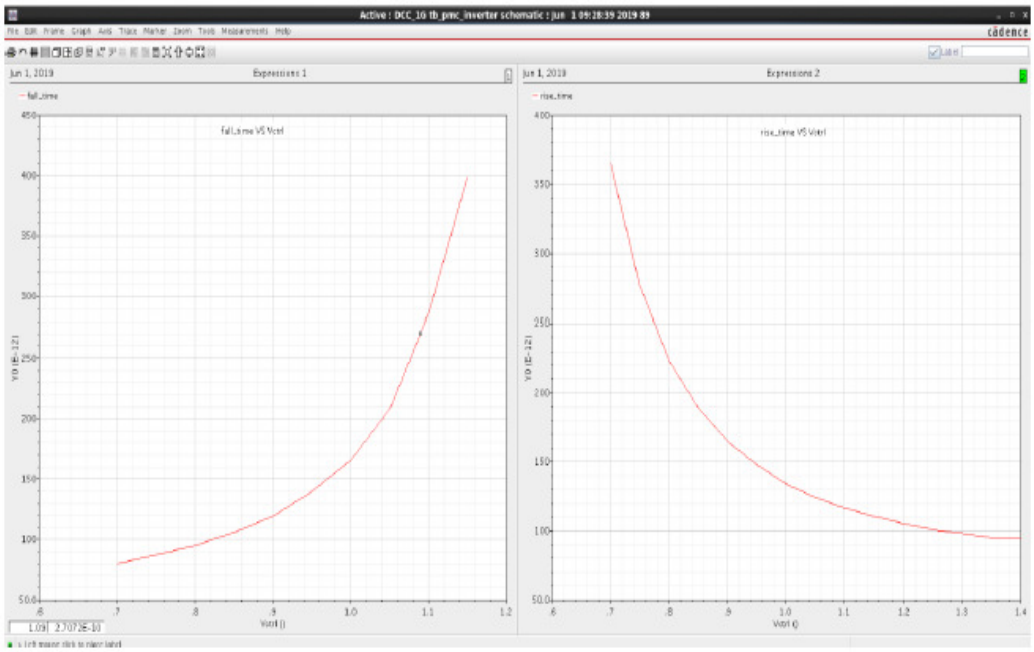

Figure 7. Rise and Fall time with respect to Vctrl

Figure 6 shows the graph for Vctrl Vs. Duty cycle. With increase in Vctrl, the current in MPS (and MP1) decreases leading to increase in charging time and increase the rise time at node 'S'. This leads to falling edge (looking at vout, the output node of second stage) moving to the right and thereby increasing the pulse width and hence increases the duty cycle. Figure 7 shows the rise

and fall time variation with respect to Vctrl. As can be seen from the Figure 7, they vary in opposite direction.

3.2. DUTY CYCLE DETECTOR

The passive integrator is one made of resistors and capacitors. The resistors consume very large area compared to transistors, active integrator can be much faster specially for high speed pulse inputs, whereas passive integrator that is made only of RC filter might become huge load and high speed circuits may not be able to drive it. Passive integrators also take longer time to settle. Hence we used an active integrator in our design. This configuration (Figure 8) below uses non-feedback way of controlling the output common mode. Figure 9 shows the averaged output waveforms of the integrator when the input clocks with duty cycle of 35-65% are being fed.

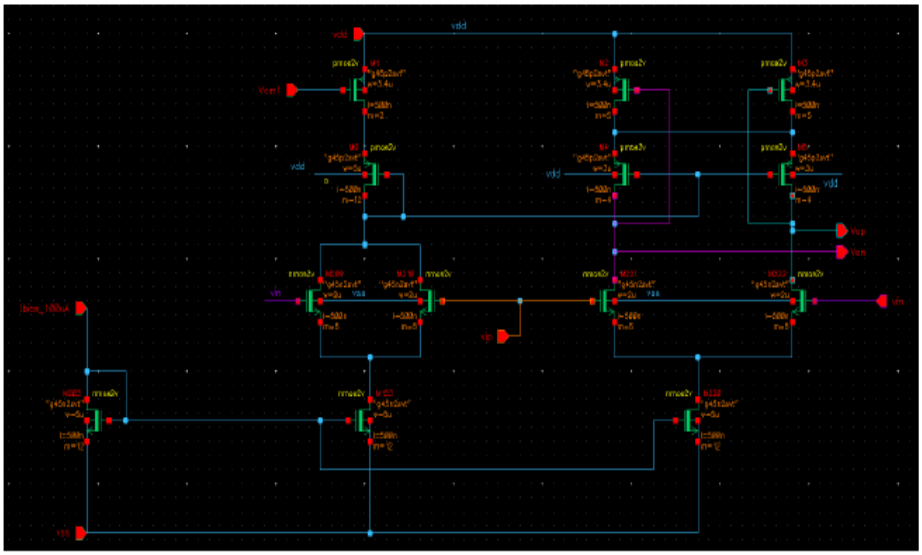

Figure 8. Integrator schematic

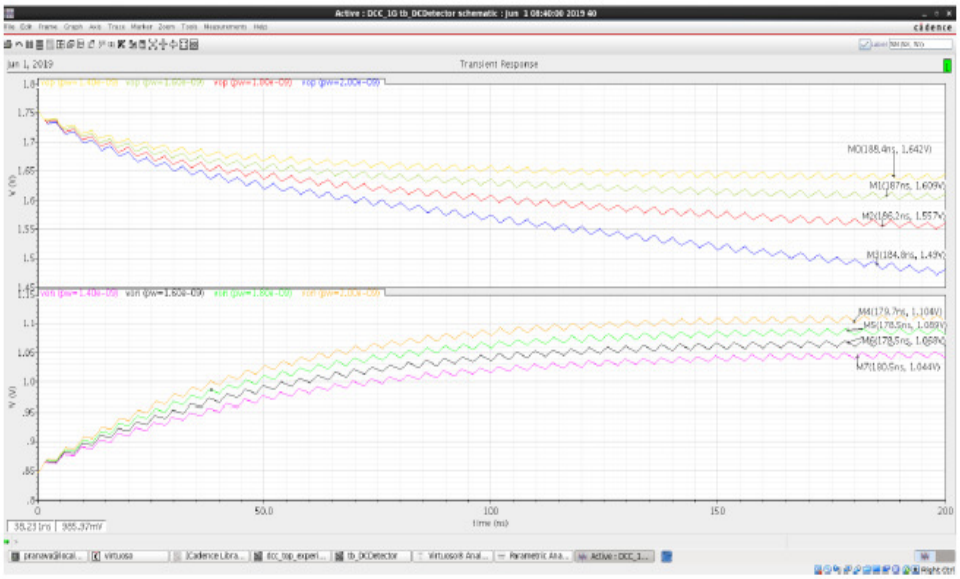

Figure 9. Output of integrator for different input duty cycles

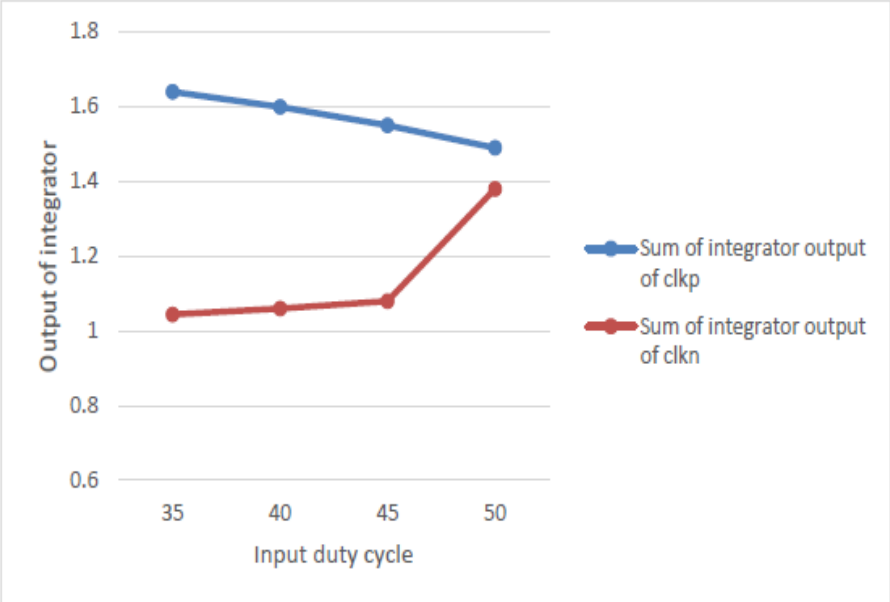

Figure 10. Pivot for integrator Output

The figure 10 shows outputs of the active integrator which are the averaged out values for corresponding two clocks. The plot shows how the average value changes as the input duty cycle changes.

3.3. CONTROL VOLTAGE GENERATOR

Finally, the analog differential voltage given by integrator is given as input to an amplifier where it gets amplified to generate a control voltage which varies the pulse width of the clock by increasing and decreasing the rise and fall times of the clock. The feedback going out from this stage to the corrector stage needs to be DC and should be within the voltage range for which DCC works. We need common mode feedback stage to stabilise the output common mode of this amplifier. We also need to have sufficient capacitance at its output node since the voltage we are feeding back to first stage is DC for abrupt changes in these feedback voltages. Here Common mode feedback based differential amplifier is used as shown in Figure 11. [2] [8]

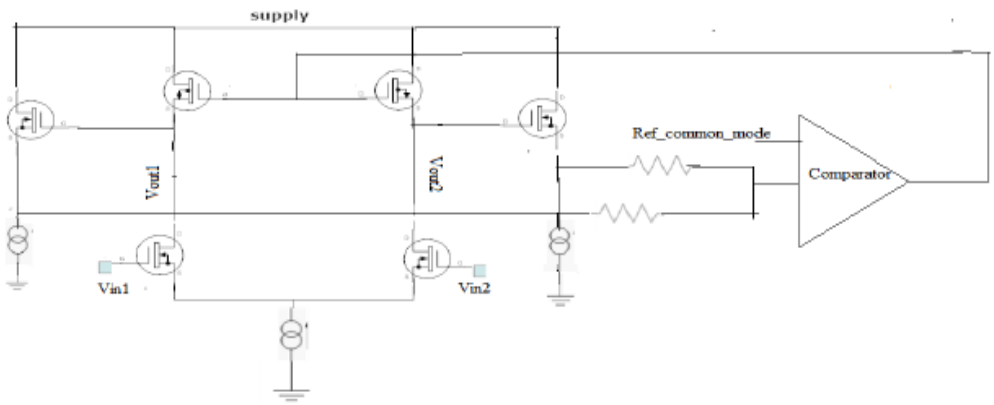

Figure 11. Circuit of CMFB

Design of differential amplifier:
I_D=Drain current, $\mu_n C_{ox}$=51.7u, µpCox=34.7u, Supply Voltage=1.8V
V_{gs}= Gate-source voltage, V_{th}=Threshold voltage=0.4V, Overdrive voltage= 0.2V
$I_D = ½\ \mu_n C_{ox}(W/L)(V_{gs}-V_{th})2$
$100u=1/2\ (51.7u)(W/L)_{5,6}(0.2)^2$
$(W/L)_{5,6}=5$
$V_{gs}-V_{th}$= 0.2V, V^{gs}=0.2+0.4=0.6V
V_g=1.4V
A_v=gm (ro2||ro4)
10=gm(62.5K||62.5K)
gm=0.32m
$gm=(2ID\ \mu nCox(W/L)\ )^{1/2}$
$(W/L)_{1,2}=4$
$I_D = ½\ \mu_p C_{ox}(W/L)(V_{gs}-V_{th})^2$
$(W/L)_{3,4}=1$

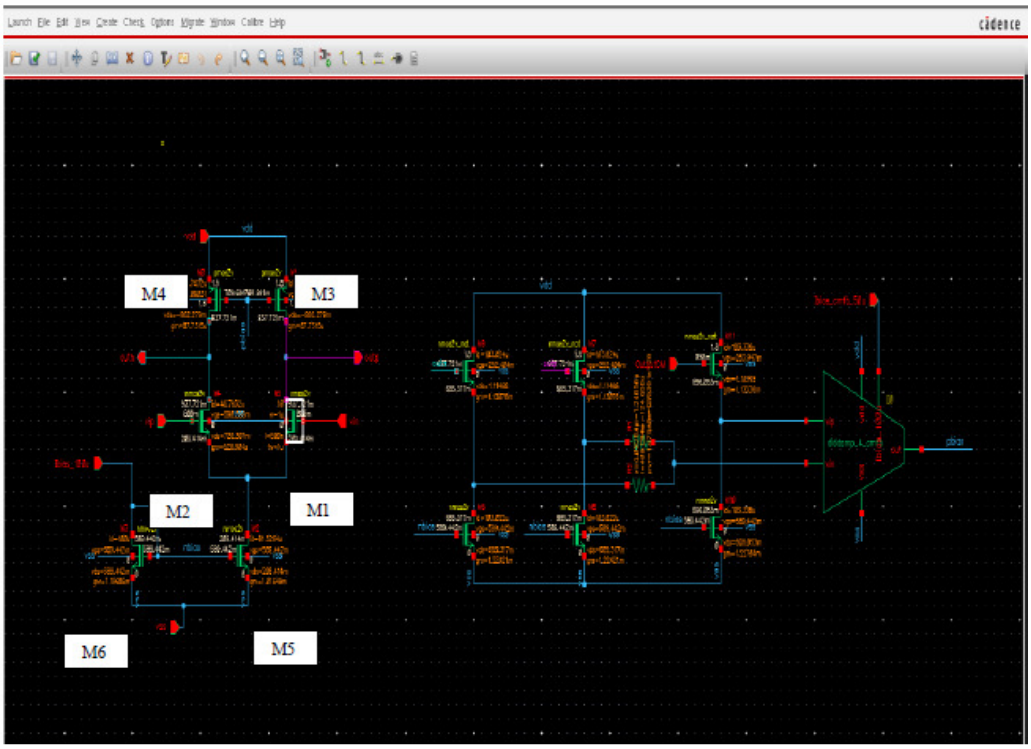

Figure 12. Implemented Schematic

Working of the circuit.

- The integrator produces two signals corresponding to the average of the two complementary input clocks. These signals are fed to the amplifier.
- This stage produces the output proportional to the difference of input voltages.
- The output of the amplifier are the control voltages that are fed back to duty cycle corrector to change the pulse width of the clock till it reaches close to 50%.

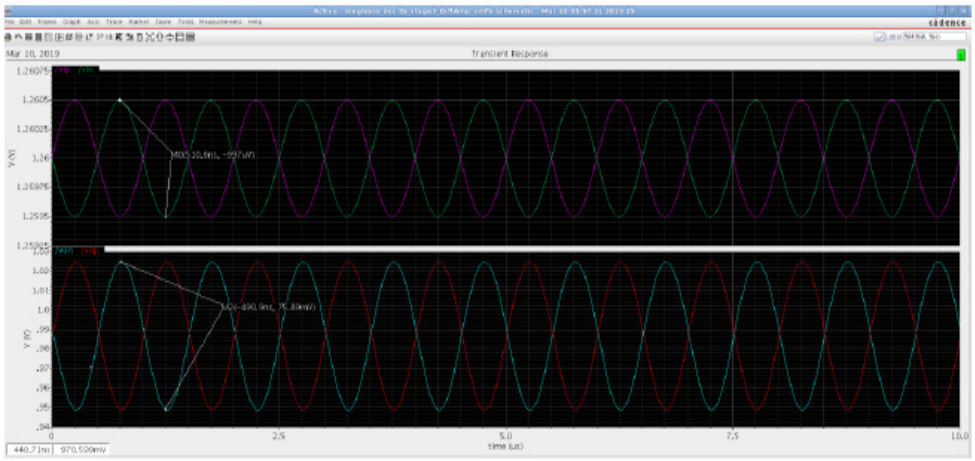

Figure 13. Transient response of the amplifier

Figure 12 shows the implemented schematic and Figure 13 shows the transient response, initially the circuit was designed to have 20dB of gain, and when it was implemented in the top level where the load and other things come into picture, the designed was modified accordingly with respect to the size of mos devices. At final stage the amplifier was able to provide gain of 31.2dB as shown in the figure 14. All these circuits till now were simulated independently by giving the ideal inputs. In the next section all these are combined to get the top level architecture where the circuit works in a loop and behaviour of this structure is discussed in the next section.

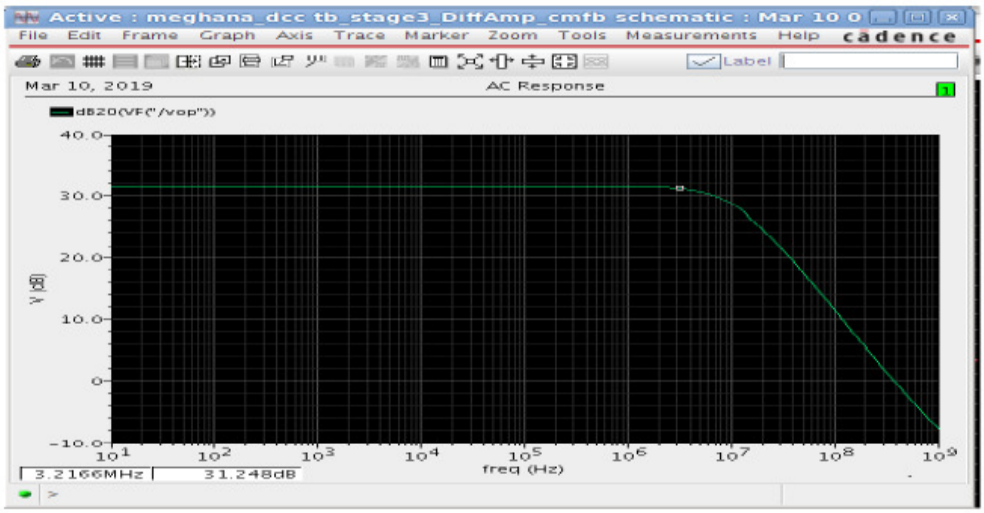

Figure 14. Gain of the amplifier in dB.

3.4. TOP LEVEL IMPLEMENTATION

This section covers the top level implementation of the duty cycle corrector, where all the above three blocks are brought together, the two complementary clocks are fed as input to corrector stage. The number of corrector stages required depends on the frequency of the clock (and the gain of the corrector stage) and we used four such stages in our design. Output of delay stages are fed to the integrator that averages the two values from two clocks and fed to differential amplifier that generates the control voltage which is fed back to the delay stages and process continues till the voltages became same and loop is stabilised as shown in Figure 15. This circuit works at frequency range of 1Mhz to 900Mhz, correcting duty cycle in the range of 35%-65%. The

correction accuracy is dependent on the gain of the amplifier, the correction frequency range is dependent on the settling time of the integrator.

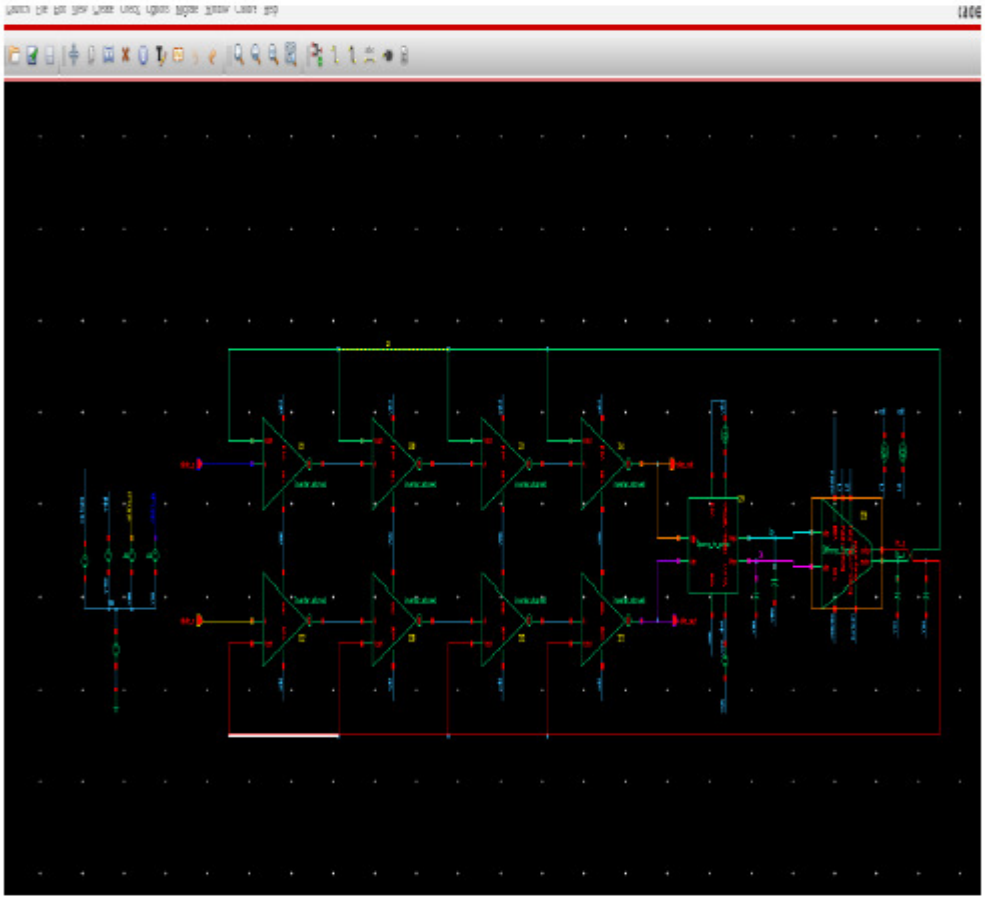

Figure 15. Top level schematic

The circuit is simulated from 35%-65% of duty cycle at 250Mhz, and the output variation can be seen in the Figure 16 below. Ip and In indicate the averaged out values of the two clocks at the integrator output. Vp and Vn denote the control voltage value generated by the last stage that is the amplifier. The loop works until the two values at the integrator output becomes equal, there the value gets settled as can be seen in the Figure 16 below. As you can see in the figure below the integrator value is settled to 1.19V and loop continues to be stable. We can observe how the control voltage is changing in order to vary the pulsewidth of the clock. The Figure 16 shows the variation in the duty cycle for 35% and 65% input respectively where we can see the 35% settles to 50.16% and 65% settles to 48.65%. In Figure 17, dc_p denotes output for 35% input dc_n denotes output for 65% input. Figure 18-20 shows the output duty cycle variation when input is 40%,45%,50%,55%,60% and it is observed that the corrected duty cycle is 50.22, 49.84, 49.4, 49.57 and 48.65 respectively and it is also observed that at the beginning the duty cycle fluctuates up and down during the process of correcting and once it reaches the maximum extent to which it can correct, it becomes stable and constant later.

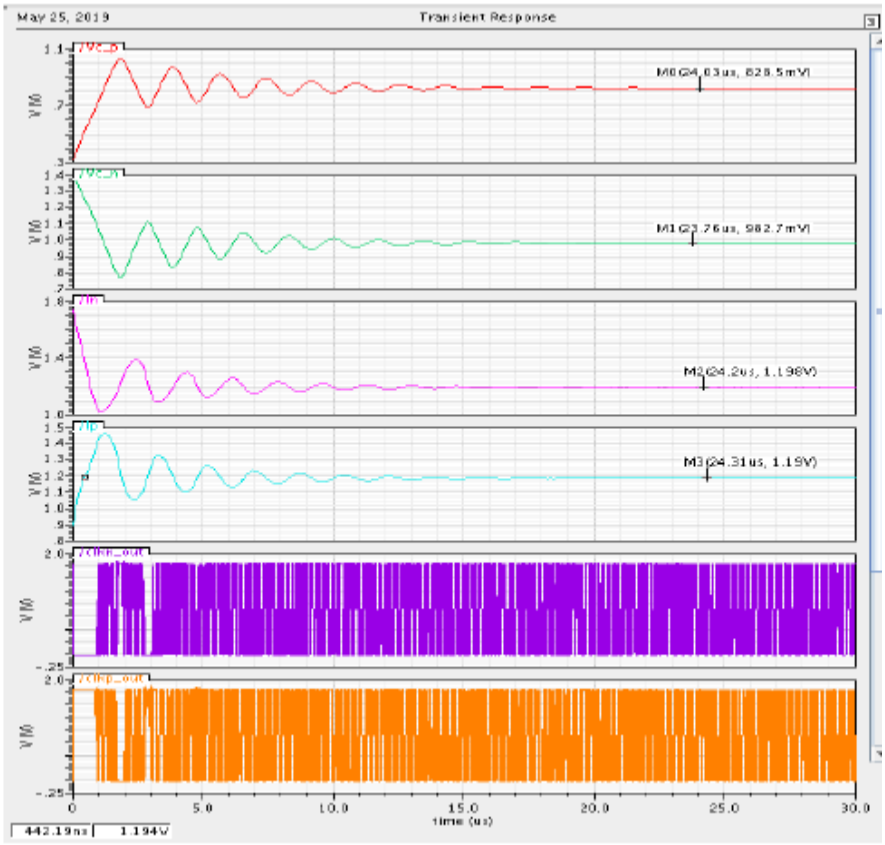

Figure 16. Output waveforms

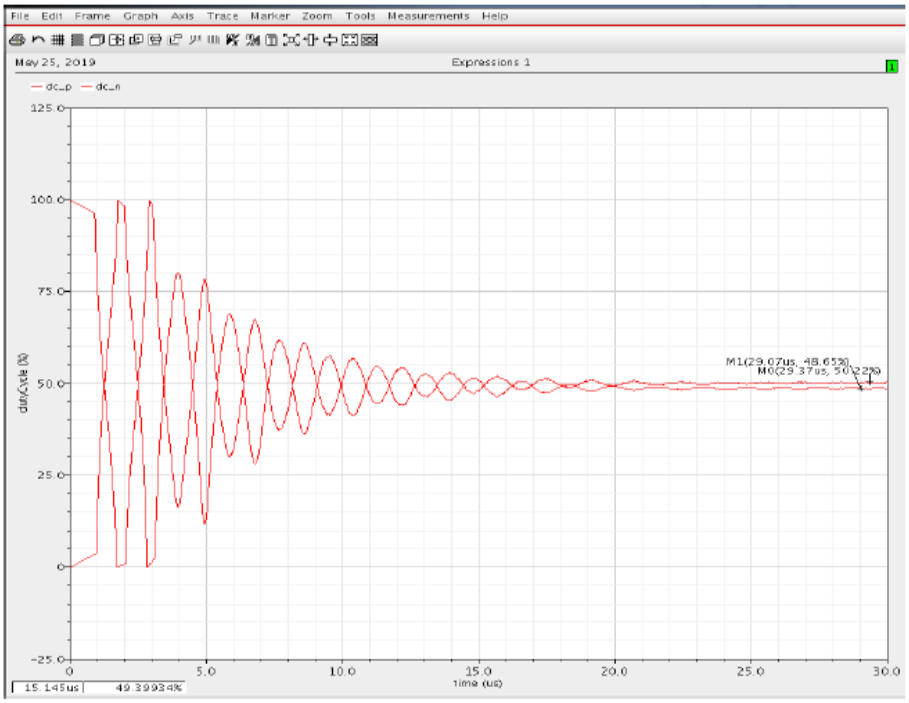

Figure 17. Duty cycle output variation for input of 35% and 65%

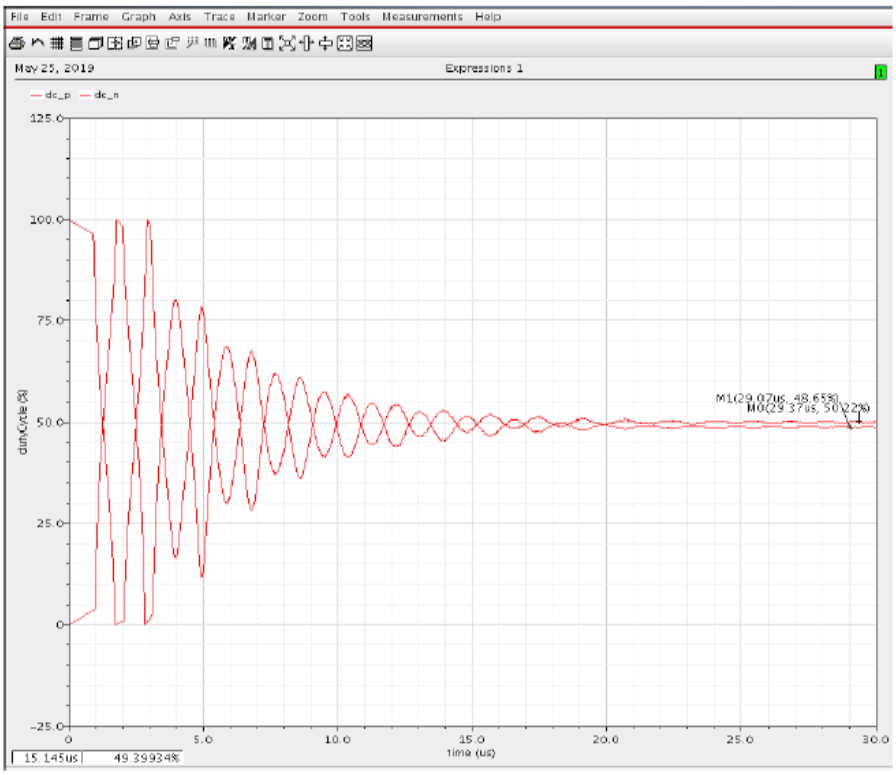

Figure 18. Duty cycle output variation for input of 40% and 60%

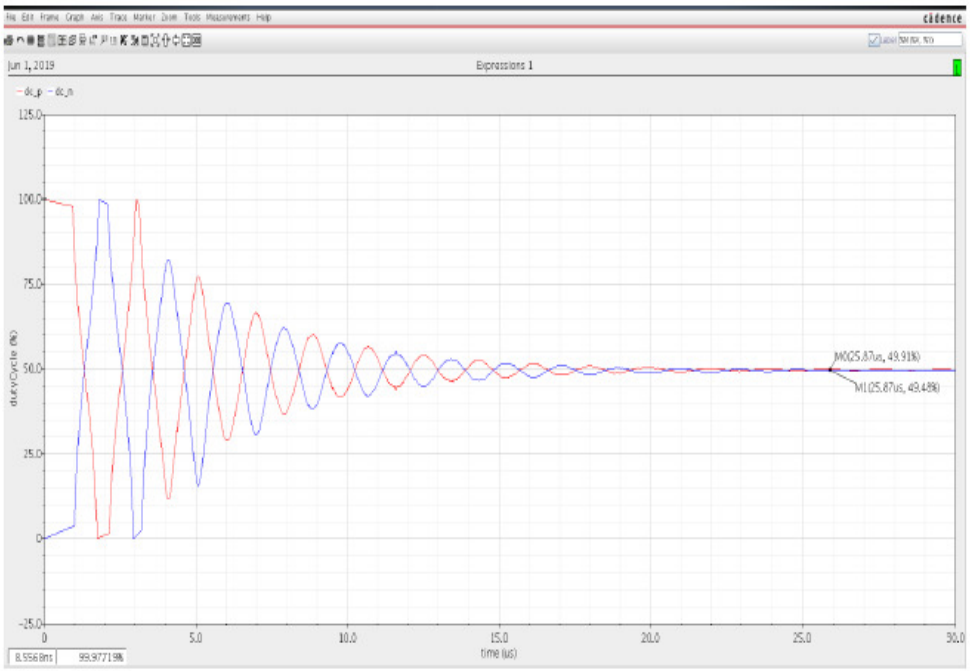

Figure 19. Duty cycle output variation for input of 45% and 55%

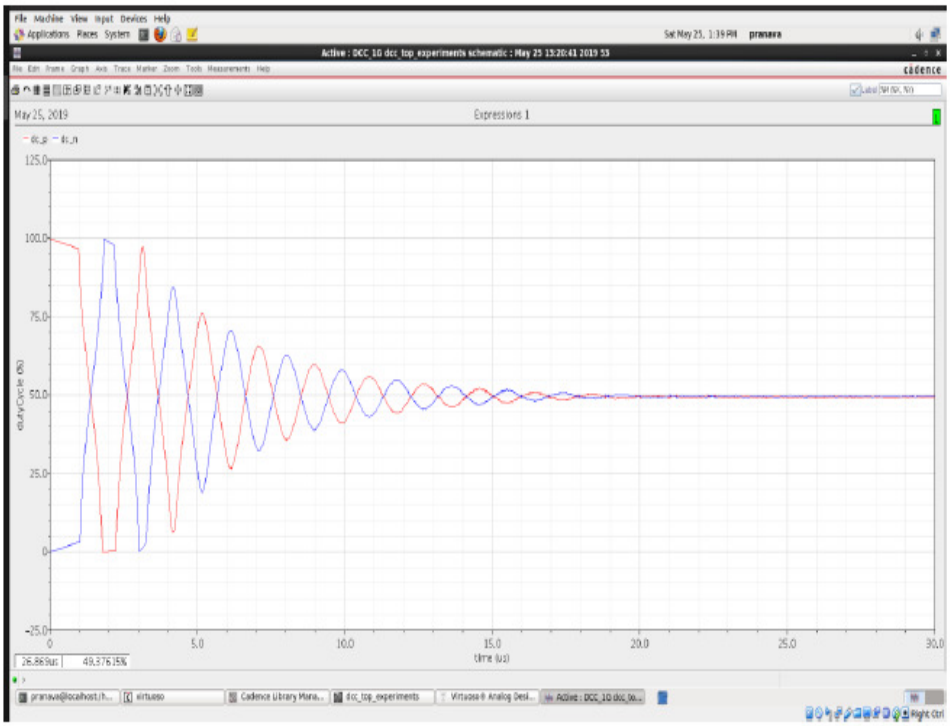

Figure 20. Duty cycle output variation for input of 50%

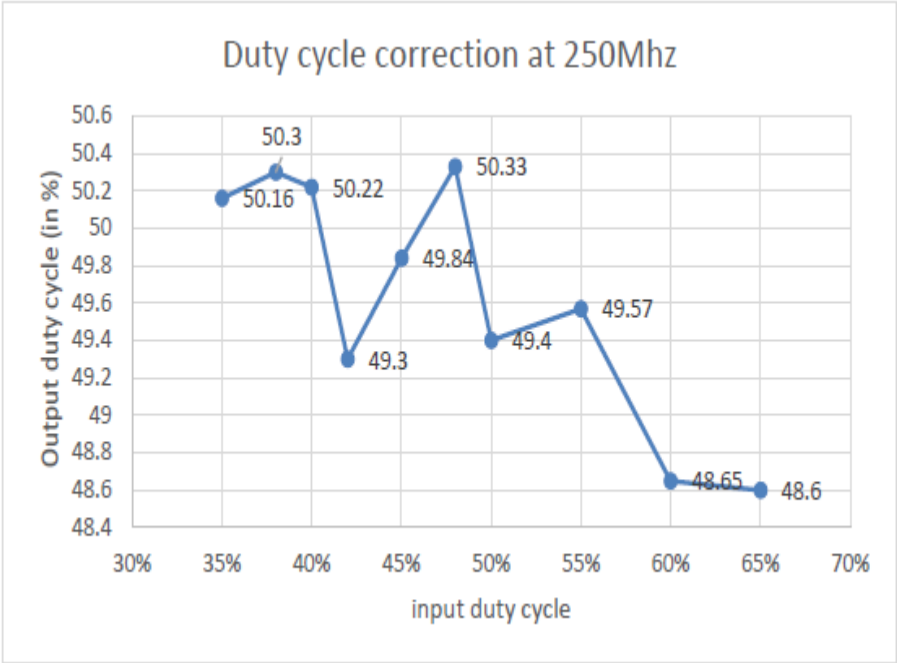

Figure 21. Input Vs. Output duty cycle variation

Above graph in Figure 21 shows the output duty cycle Vs input duty cycle for inputs varying from 35%-65% simulated at 250Mhz, and as it is observed accuracy is within 1.5%. Table 1 contains the summary of the output values at each stage at the end of simulation for different input duty cycles.

Input duty cycle(%)	Integrator Output(V)	Control voltage(v)	Output duty cycle(%)	Rise time (ps)	Fall time (ps)
35	1.19	828.5m	50.16	150.74	177.75
40	1.192	852m	50.22	157.76	171.38
45	1.194	875.7m	49.84	171.68	145.57
50	1.194	906m	49.4	178.4	144.9
55	1.194	936.2m	49.57	194.26	137.6
60	1.192	958.2m	48.65	201.65	124.92
65	1.19	982.7m	48.6	226.6	115.92

Table 1. Parameter analysis

Power of the circuit is calculated by supply voltage * supply current and it is 1.01mW with supply voltage of 1.8V. The circuit is simulated for different frequencies, from 1MHz to 900 MHz. And the duty cycle is corrected in the range of +/- 1.5% of accuracy as shown below in Figure 22. The circuit can be still optimized by increasing the gain of an active integrator, so that it can support even Gigahertz frequencies.

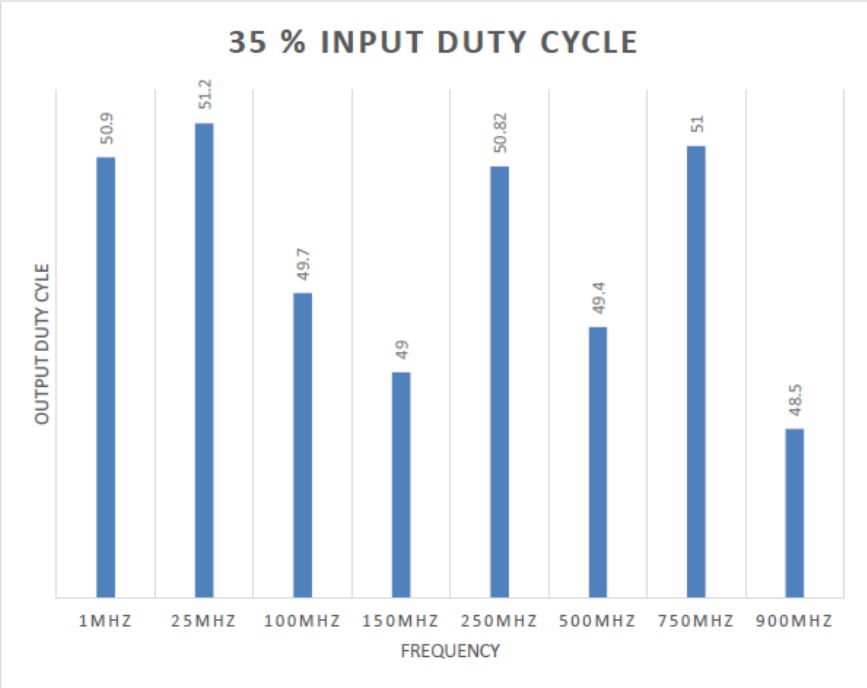

Figure 22. Frequency Vs output duty cycle

4. CONCLUSIONS

From above work it can be summarized that duty cycle corrector is one essential block in high speed circuits. The analog feedback duty cycle corrector is being proposed. It corrects the distorted input clock to achieve approximately 50% of duty cycle. It is able to correct input range of 35% to 65% with Megahertz frequency range. Analog feedback has an advantage of better accuracy and sometimes reduces the complexity. The limitation of this work is the circuit fails to operate at GHz frequencies.

As a scope for future work, the circuit can be still optimized by increasing the gain of an active integrator, so that it can support even Gigahertz frequencies and accuracy can be increased by increasing the gain of amplifier part of control voltage generator.

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