DESIGN OF LOW POWER PHASE LOCKED LOOP (PLL) USING 45NM VLSI TECHNOLOGY

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ABSTRACT

Power has become one of the most important paradigms of design convergence for multi gigahertz communication systems such as optical data links, wireless products, microprocessor & ASIC/SOC designs. POWER consumption has become a bottleneck in microprocessor design. The core of a microprocessor, which includes the largest power density on the microprocessor. In an effort to reduce the power consumption of the circuit, the supply voltage can be reduced leading to reduction of dynamic and static power consumption. Lowering the supply voltage, however, also reduces the performance of the circuit, which is usually unacceptable. One way to overcome this limitation, available in some application domains, is to replicate the circuit block whose supply voltage is being reduced in order to maintain the same throughput .This paper introduces a design aspects for low power phase locked loop using VLSI technology. This phase locked loop is designed using latest 45nm process technology parameters, which in turn offers high speed performance at low power. The main novelty related to the 45nm technology such as the high-k gate oxide ,metal-gate and very low-k interconnect dielectric described. VLSI Technology includes process design, trends, chip fabrication, real circuit parameters, circuit design, electrical characteristics, configuration building blocks, switching circuitry, translation onto silicon, CAD, practical experience in layout design

KEYWORDS

Phase locked loop (PLL), voltage-controlled oscillator (VCO), 45nm technology, VLSI technology, low power.

1. INTRODUCTION

The electronics industry has achieved a phenomenal growth over the last two decades, mainly due to the rapid advances in integration technologies, large-scale

systems design - in short, due to the advent of VLSI [1]. The number of applications of integrated circuits in high-performance computing, telecommunications, and consumer electronics has been rising steadily, and at a very fast pace. Typically, the required computational power (or, in other words, the intelligence) of these applications is the driving force for the fast development of this field.

A new MOS model, called BSIM4, has been introduced in 2000 [2]. A simplified version of this model is supported by Microwind 3.1, and recommended for ultra-deep submicron technology simulation. The role of oscillators is to create a periodic logic or analog signal with a stable and predictable frequency. Oscillators are required to generate the carrying signals for radio frequency transmission, but also for the main clocks of processors. The output is equal to the input, and the phase difference is equal to one fourth of the period ($\pi/2$) according to the phase Detector principles.

The phase-lock-loop (PLL) is commonly used in microprocessors to generate a clock at high frequency (Fout = 2GHz for example) from an external clock at low frequency (Fref = 100MHz for example) [3]. The PLL is also used as a clock recovery circuit to generate a clock signal from a series of bit transmitted in serial without synchronization clock.

The PLL uses a high frequency oscillator with varying speed, a counter, a phase detector and a filter. The PLL includes a feedback loop which lines up the output clock ClkOut with the input clock ClkIn through a phase locking stabilization process. When locked, the high input frequency fout is exactly N* fin as shown in figure.1. A variation of the input frequency fin is transformed by the phase detector into a pulse signal which is converted in turn into variation of the analog signal Vc [3].This signal changes the VCO frequency which is divided by the counter and changes clkDiv according to fin.

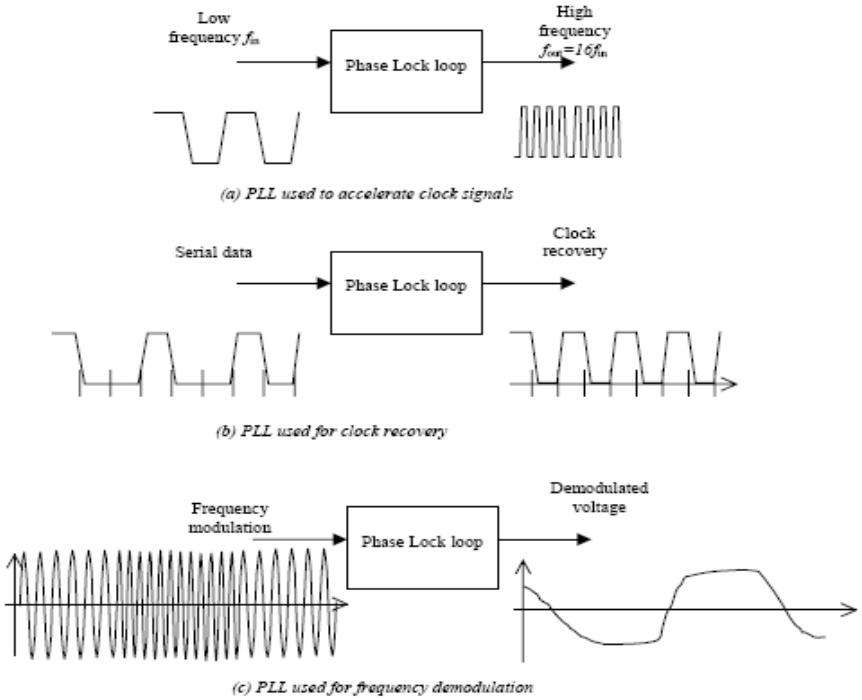

Figure 1. A PLL used for frequency demodulation.

A basic PLL is a feedback system composed of three elements: a phase detector, a loop filter and a voltage controlled oscillator (VCO). The VCO is the most important functional unit in the PLL. Its output frequency determine the effectiveness of PLL. In addition to operating at highest frequency, this unit consumes the most of the power in the system [4].

Obviously, this unit is of particular focus to reduce power consumption. PLL with multiple outputs means to VCO with multiple output. This paper particularly focus on study and design of phase-locked loop with low power consumption using VLSI technology.

The voltage controlled oscillator (VCO) generates a clock with a controllable frequency [4] . The VCO is commonly used for clock generation in phase lock loop circuits . The clock may vary typically by +/-50% of its central frequency. The current-starved inverter chain uses a voltage control Vcontrol to modify the current that flows in the N1, P1 branch as shown in figure.2. The current through N1 is mirrored by N2, N3 and N4. The same current flows in P1. The current through P1 is mirrored by P2, P2, and P4. Consequently, the change in

Vcontrol induces a global change in the inverter currents, and acts directly, the delay.

The Software microwind 3.1used in paper allows us to design and simulate an integrated circuit at physical description level [5]. The package contains a library of common logic and analog ICs to view and simulate. It also includes all the commands for a mask editor as well as original tools never gathered before in a single module such as 2D and 3D process view, Verilog compiler, tutorial on MOS devices. We can gain or access to Circuit Simulation by pressing one single key. The electric extraction of the circuit is automatically performed and the analog simulator produces voltage and current curves immediately.

2. TECHNOLOGY OVERVIEW & DESIGN ISSUES

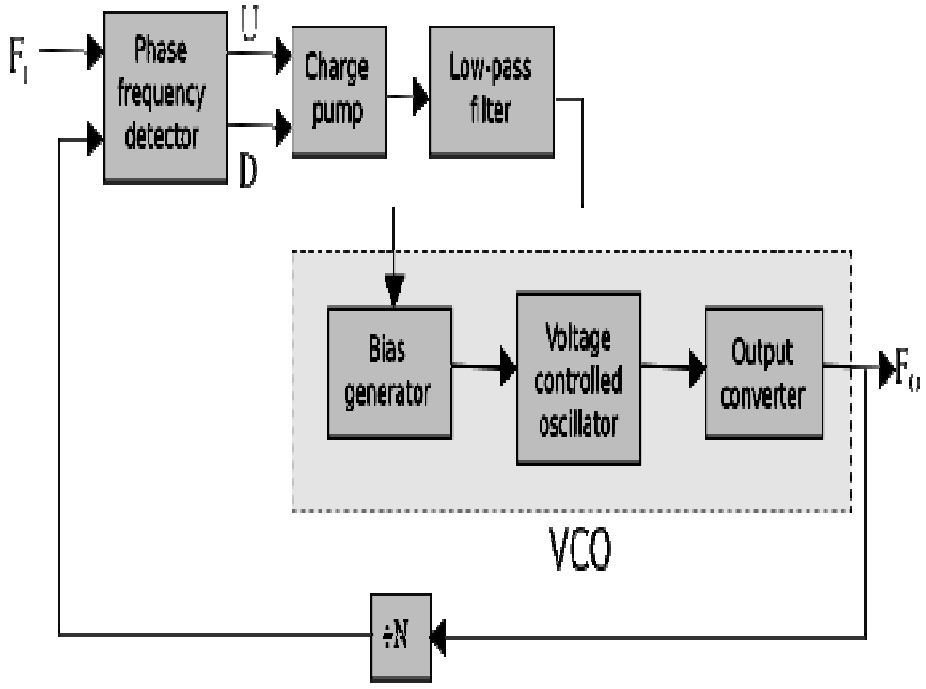

Figure.2 Basic Phase locked loop

Analog PLLs are generally built of a phase detector, low pass filter and voltage-controlled oscillator (VCO) placed in a negative feedback configuration as shown in

fig.2 . There may be a frequency divider in the feedback path or in the reference path, or both, in order to make the PLL's output clock an integer multiple of the reference [6]. A non integer multiple of the reference frequency can be created by replacing the simple divide-by-N counter in the feedback path with a programmable pulse swallowing counter. This technique is usually referred to as a fractional-N synthesizer or fractional-N PLL.

The oscillator generates a periodic output signal. Assume that initially the oscillator is at nearly the same frequency as the reference signal. Then, if the phase from the oscillator falls behind that of the reference, the phase detector causes the charge pump to change the control voltage, so that the oscillator speeds up. Likewise, if the phase creeps ahead of the reference, the phase detector causes the charge pump to change the control voltage to slow down the oscillator. The low-pass filter smooth out the abrupt control inputs from the charge pump. Since initially the oscillator may be far from the reference frequency, practical phase detectors may also respond to frequency differences, so as to increase the lock-in range of allowable inputs.

Depending on the application, either the output of the controlled oscillator, or the control signal to the oscillator, provides the useful output of the PLL system.

A phase locked loop (PLL) with a single voltage controlled oscillator (VCO) is generally configured to lock multiple internal clocks to multiple incoming data signals of different frequencies. Because of low power scalability with lambda based rules, very high levels of integration and high performance, PLL with low power output is to be implement using 45nm deep submicron technology of VLSI [7].

Following are the main objective.

2.1 Low Power

For low power, low leakage transistors will be used and a little variation in frequency will be compromise on [8]. For low power, low leakage transistors is used and compromised on little frequency. Also there will be a shutdown input in proposed circuit which will being the PLL to hold or there can be a pin, which if enabled then will make the PLL frequency to half [9].

2.2 Advanced VCO

The VCO is the most important functional unit in the PLL Its output frequency determines the effectiveness of PLL. In addition to operating at highest frequency this unit consumes the most of the power in the system. Obviously this unit is a particular focus to reduce power consumption.It is objective of this work to demonstrate that gigahertz frequency range and milliwatt power consumption of a monolithic CMOS VCO with good phase noise performance can be achieved.

The phase detector of the PLL is the XOR gate. The XOR gate output produces a regular square oscillation V_{PD} when the clock input circuit and signal input div1n have one quarter of period shift (or 90^0 or /2) $\pi/2$) For other angles, the output is no more regular. At initialization, the average value of XOR output V_{PD} is close to 0. When the phase between clkDiv and ClkIn is around) $\pi/2$, V_{PD} is VDD/2 . Then it is increases up to VDD. The gain of the phase detector is the ratio between V_{PD} and $\Delta\phi$. When the phase difference is larger than π, the slope sign is negative until 2π. When locked, the phase difference should be close to $\pi/2$ [9].

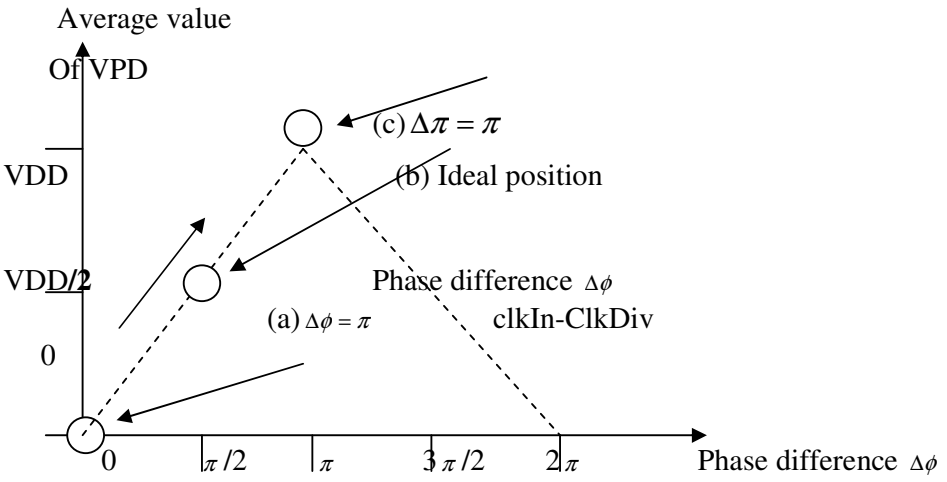

Figure3.The XOR Phase detector

This is shown in figure 3. Obsequently, V_{PD} and the phase difference are linked by expression

$$V_{PD} = \frac{V_{DD.\Delta\phi}}{\pi}$$

The filter of PLL is used to transform the instantaneous phase difference V_{PD} into an analog voltage V_C which is equivalent to the average voltage V_{PD}. The rapid variations of the phase detector output are converted into a slow varying signal V_C by filter, which will later control the voltage controlled oscillator.

The current mirror is one of the most useful basic block inn analog design. It is primarily used to copy currents. The VCO is commonly used for clock generation in phase lock loop circuits. The clock may vary typically by +/- 50percent of its central frequency for which current mirror/current started circuits will be used. Besides this charge pump circuits will also be used to convert digital error pulse to analog error current.

3. SIMULATION SETUP

This paper describes the improvement related to the CMOS 45nm technology and the implementation of this technology in Microwind 3.1. For technology mode 45nm[4], effective gate length is 25nm with metal gate and SiON gate dielectric. There may exist several variants of the 45-nm process technology. One corresponds to the highest possible speed, at the price of a very high leakage current. This technology is called “High speed” as it is dedicated to applications for which the highest speed is the primary objective: fast microprocessors, fast DSP, etc.

The Software Microwind 3.1 used in paper allows us to design and simulate an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. It also includes all the commands for a mask editor as well as original tools never gathered before in a single module such as 2D and 3D process view, Verilog compiler, tutorial on MOS devices. You can gain access to Circuit Simulation by pressing one single key. The electric extraction of your circuit is automatically performed and the analog simulator produces voltage and current curves immediately.

4. EXPERIMENTAL RESULTS

Figure 4. Shows the phase locked loop using 45nm technology. This PLL is designed with microwind 3.1 software using 45 nm design rule. The threshold voltage used is Vhigh equal to 1.00v. This PLL is designed for 7GHz frequency. For low power

low leakage BSIM4 Transistors are used. This PLL includes current mirror, precharge and charge pump circuits with filter, phase detector and VCO.

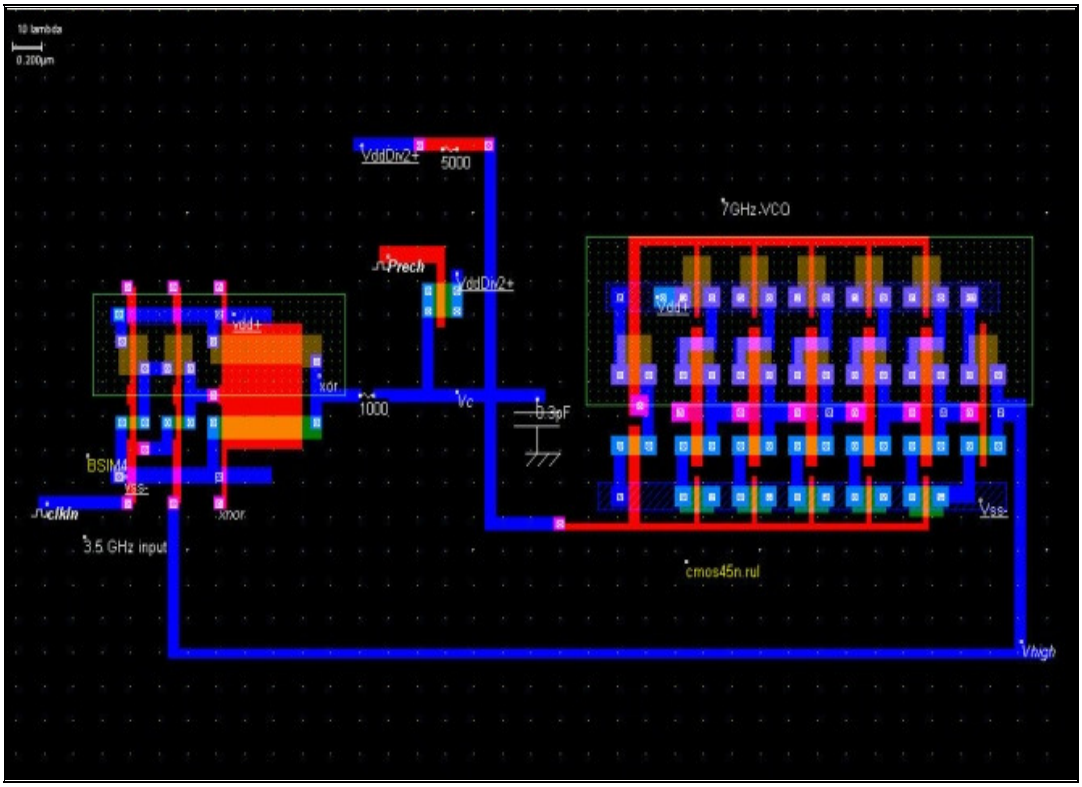

Figure 4. Low power phase locked loop (PLL) using 45nm technology.

The simulation of a low power PLL is shown fallowing figure 5 .This shows the simulation of a high performance PLL circuit ,frequency verses time .The frequency is 7GHz. for which power consumed is 57.231 microwatt.

The main drawback of this type of PLL is the great influence of temperature and VDD supply on the stability of the oscillation. If we change the temperature, the device current changes, and consequently the oscillation frequency are modified. Such oscillators are rarely used for high stability frequency generators.

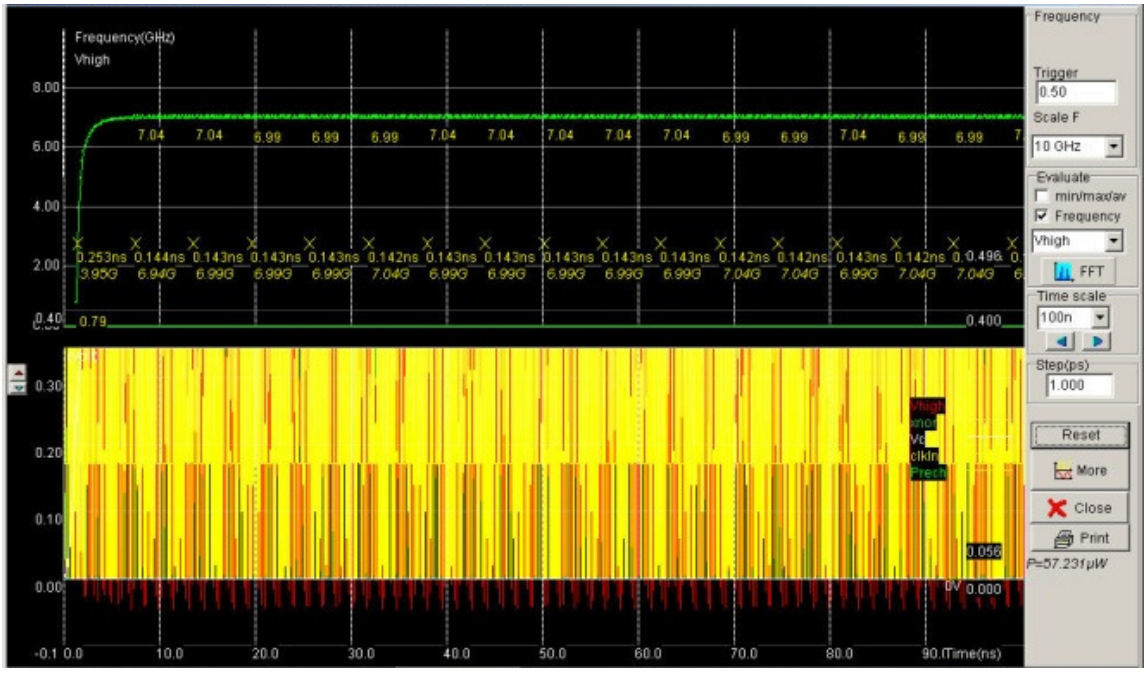

Figure 5. Simulation of low power pll of figure 4.(Frequency versus time).

5. CONCLUSION

The fundamental difficulty of PLL design using deep submicron technology is to achieve low power consumption which may due to uncertainty in the value of threshold or supply voltage.[4].

Since PLLs are widely used in communication application such as frequency synthesis for missile tracking, noise stability is an important factor which can be analyzed with the components of filter.

The Software used in paper allows us to design and simulate an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. It also includes all the commands for a mask editor as well as original tools never gathered before in a single module such as 2D and 3D process view, Verilog compiler, tutorial on MOS devices. You can gain access to Circuit Simulation by pressing one single key. The electric extraction of your circuit is automatically performed and the analog simulator produces voltage and current curves immediately.

The layout of PLL which is developed by us is a modified design of low power high performance VCO. This is a optimum design for use in industries at 45 nanotechnology. In the estimated design, more emphases is given on power consumption, layout design and many more. This report is a brief study of high

performance PLL on 45 nanometer VLSI technology to achieve some objectives as mention above.

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Short Biography

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