EFFICIENT HARDWARE CO-SIMULATION OF DOWN CONVERTOR FOR WIRELESS COMMUNICATION SYSTEMS

Rajesh Mehra[1] and Swapna Devi[2]

[1,2]Department of Electronics & Communication Engineering, Sector-26, NITTTR, Chandigarh, UT, India
[1]rajeshmehra@yahoo.com

ABSTRACT

*In this paper an optimized hardware co-simulation approach is presented to design & implement GSM based digital down convertor for **S**oftware **D**efined **R**adios. The proposed DDC is implemented using optimal equiripple technique to reduce the resource requirement. A computationally efficient polyphase decomposition structure is used to improve the hardware complexity of the overall design. The proposed model is implemented by using embedded multipliers, LUTs and BRAMs of target device to enhance the system performance in terms of speed and area. The DDC model is designed and simulated with Simulink and Xilinx System Generator, synthesized with Xilinx Synthesis Tool (XST) and implemented on Virtex-II Pro based xc2vp30-7ff896 FPGA device. The results show that proposed design can operate at maximum frequency of 160 MHz by consuming power of 0.34004W 25 °C junction temperature. The proposed design is consuming very less resources available on target device to provide cost effective solution for SDR based wireless applications.*

KEYWORDS

ASIC, BRAM, FPGA, GSM, LUT & SDR

1. INTRODUCTION

Today's consumer electronics such as cellular phones and other multi-media and wireless devices often require digital signal processing (DSP) algorithms for several crucial operations in order to increase speed, reduce area and power consumption. The range of user terminals that need to be connected in this communication world, include cell phones, video phones, satellite phones, PDAs, portable computers and other nomadic computing devices. To flourish and succeed in these dynamic environment equipment suppliers must build highly flexible systems that operate across multiple wireless and wired network standards. They must be able to rapidly adopt new business models as they evolve, and they must be able to incorporate new signal processing techniques that allow increased network capacity, increased coverage, increased quality of service, or a combination of all. The answer to the diverse range of requirements is the *software defined radio*. The digital signal processing application by using variable sampling rates can improve the flexibility of a software defined radio. It reduces the need for expensive anti-aliasing analog filters and enables processing of different types of signals with different sampling rates. It allows partitioning of the high-speed processing into parallel multiple lower speed processing tasks which can lead to a significant saving in computational power and cost.

Due to a growing demand for such complex DSP applications, high performance, low-cost Soc implementations of DSP algorithms are receiving increased attention among researchers and design engineers. Although ASICs and DSP chips have been the traditional solution for high performance applications, now the technology and the market demands are looking for changes.

On one hand, high development costs and time-to-market factors associated with ASICs can be prohibitive for certain applications while, on the other hand, programmable DSP processors can be unable to meet desired performance due to their sequential-execution architecture. In this context, embedded FPGAs offer a very attractive solution that balance high flexibility, time-to-market, cost and performance. So this paper focuses on efficient design and implementation of digital down convertor for software radios on an FPGA target device.

2. DIGITAL DOWN CONVERTOR (DDC)

The widespread use of digital representation of signals for transmission and storage has created challenges in the area of digital signal processing [1]. The applications of digital FIR filter and up/down sampling techniques are found everywhere in modem electronic products. For every electronic product, lower circuit complexity is always an important design target since it reduces the cost [2]. There are many applications where the sampling rate must be changed. Interpolators and decimators are utilized to increase or decrease the sampling rate. Up sampler and down sampler are used to change the sampling rate of digital signal in multi rate DSP systems. This rate conversion requirement leads to production of undesired signals associated with aliasing and imaging errors. So some kind of filter should be placed to attenuate these errors [3].

A digital down convertor (DDC) is an important part of SDR based 3G or 4G baseband receivers. It shifts the spectrum of interest from its carrier frequency, i.e. intermediate frequency to baseband [4]. It also performs decimation and matched filtering to remove adjacent channels and maximize the received signal-to-noise ratio (SNR). A DDC is mainly used to down convert or decimate the GSM signal [5]. Typically lowpass filters are used to reduce the bandwidth of a signal prior to reducing the sampling rate. This is done to minimize aliasing due to the reduction in the sampling rate. Down sampler is basic sampling rate alteration device used to decrease the sampling rate by an integer factor [6]-[7]. On the receiver side, digital IF techniques can be used to sample an IF signal and perform channelization and sample rate conversion in the digital domain. Using under sampling techniques, high frequency, IF signals typically more than 100MHz can be quantified. For SDR applications, since different standards have different chip/bit rates, non-integer sample rate conversion is required to convert the number of samples to an integer multiple of the fundamental chip/bit rate of any standard.

There are many advanced signal processing tasks performed in a modern digital receiver using two sub-systems called front end and back end systems. A front-end sub system operates at high-data rate and a back-end operates at low data rate or chip-rate. The front-end high-data rate FPGA DSP implements channelization functions for a multi-carrier system. Each channelizer accesses the digital IF (intermediate frequency), translates a channel to baseband and using a multi-stage multi-rate filter adjusts the sample rate to satisfy Nyquist for the selected band. The back-end processor will typically operate on multiple slower rate sample streams performing functions like rake processing, adaptive rake processing, demodulation, turbo decoding, Viterbi decoding. In a QAM system, carrier recovery, timing recovery and adaptive channel equalization will be required. Virtually all digital receivers perform channel access using a digital down-converter (DDC). A simplified block diagram of digital down convertor is shown in Figure1. The desired channel is translated to baseband using the digital mixer comprising the multipliers *M1, M2* and a direct digital synthesizer (DDS). The sample rate of the signal is then adjusted to match the channel bandwidth [8]-[10]. This is performed using a multi-stage multi-rate filter consisting of the filters $C(z)$,$G(z)$ and $H(z)$.

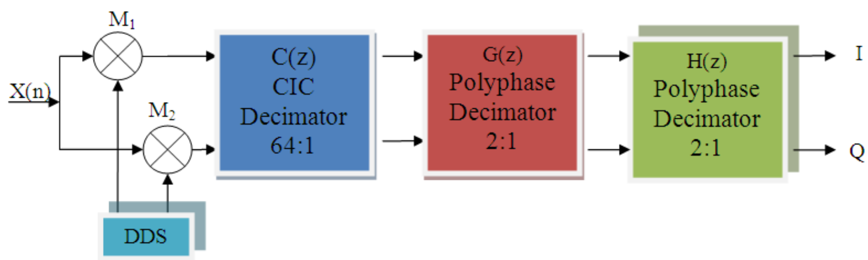

Figure1. Digital down convertor

Modern base station transceivers will often require a large number of DDCs to support multicarrier environments or for coherently down-converting and combining a number of narrow-band channels into one wide-band digital signal. The DDC is typically located at the front-end of the signal processing conditioning chain, close to the A/D, and is usually required to support high sample rate processing in the region of 100 to 200 MSPS. The high data rate, coupled with the large arithmetic workload, is not well suited for DSP microprocessor implementation. Application specific standard products (ASSP) are a common solution. A more flexible, and typically higher-performance alternative, is to implement the DDC using programmable logic like FPGA. Since DDC functions only require a modest amount of FPGA silicon resources, many other receiver functions can be implemented in the same device

3. Proposed DDC Model Design

A model of Digital Down-Converter (DDC) is designed to meet the 3G and 4G specifications using a multi-section CIC decimator and two Equiripple based polyphase decimators [11]-[12] with the help of Simulink and Xilinx System Generator blocks as shown in Figure2. The upper portion enclosed in rectangular block shows the software part and lower portion enclosed in another rectangular block shows the hardware part implemented on target FPGA. The equiripple window based technique is used which results in less number of required coefficients as compared to other window techniques to improve hardware complexity and speed.

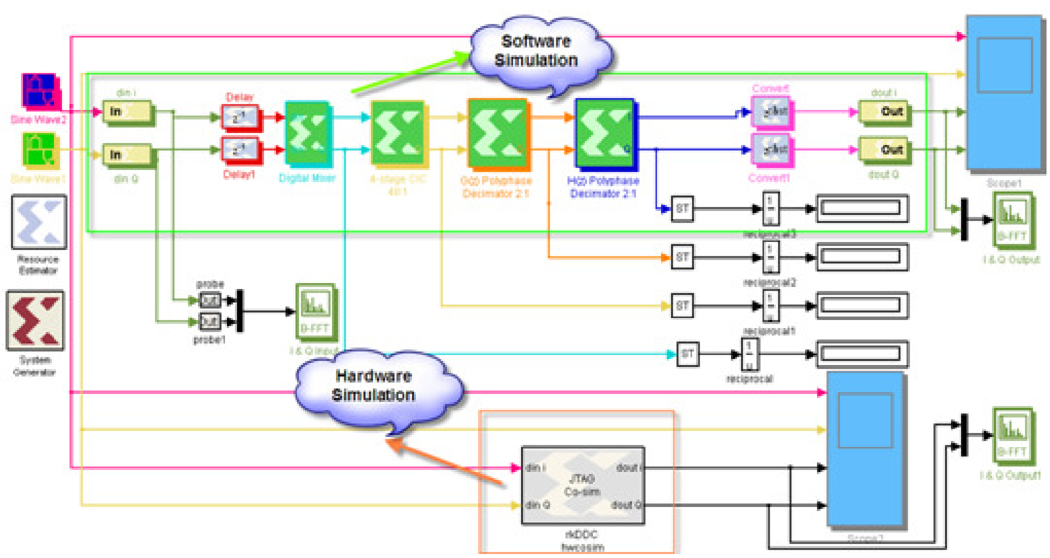

Figure2. Proposed DDC Hardware Co-simulation Model

The functions performed by the developed model are waveform synthesis (DDS), complex multiplication and multirate filtering. The proposed model consists of three major parts namely mixer section, CIC section and decimator section.

3.1 Mixer Section

This section consists of two multipliers M1 and M2 along with direct data synthesizer (DDS) as shown in Figure3. The multipliers M1 and M2 used in proposed DDC model are implemented using the Virtex-II embedded multipliers. The pipelined operation is used to enhance the sample rate in excess of 200 MHz. In this design, with an input sample rate of 52 MHz, a single multiplier could be time-shared to implement the input heterodyne. The DDS is using a phase-dithered look-up table-based synthesizer. The FPGA block memory is used to store one quarter of a cycle of a sinusoid. The dual-port memory enables both the in-phase and quadrature components of the local oscillator to be generated simultaneously using a single block RAM. The single block RAM implementation can generate a 4096-sample full-wave 16-bit precision complex sinusoid. With phase dithering, the synthesizer will generate a mixing signal with a spurious free dynamic range (SFDR).

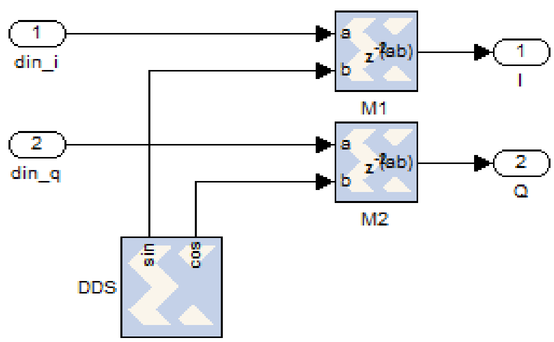

Figure3. Mixer Section

The DDS spectral efficiency is 102dB SFDR. The input and output sample rates are chosen to be 52 MHz and 270.8333 kHz respectively. This corresponds to a sample rate change of 192.

3.2 CIC Section

The baseband channel is highly oversampled so a simple cascade of boxcar filters, implemented as a cascaded integrator comb (CIC) [10] will be employed to initially reduce the sample rate by a factor of 48.

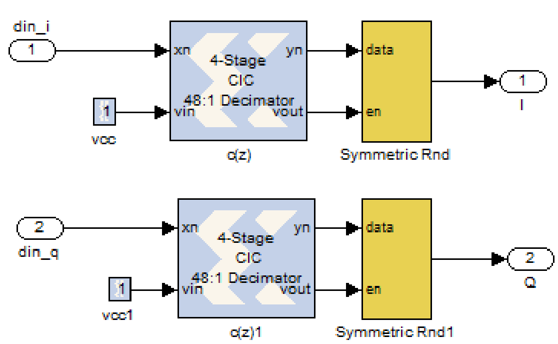

Figure4. CIC Section

The CIC filter $C(z)$ is multiplier less consisting only of integrator and differentiator sections. For this application a cascade of 4 integrators followed by 4 differentiators, with an embedded 48:1 rate change is used as shown in Figure4.

3.3 Polyphase Decimator Section

The CIC filter is followed by a cascade of two 2:1 polyphase decimators shown in Figure5 & 6 respectively to produce the required input-to-output sample rate change of 192:1.

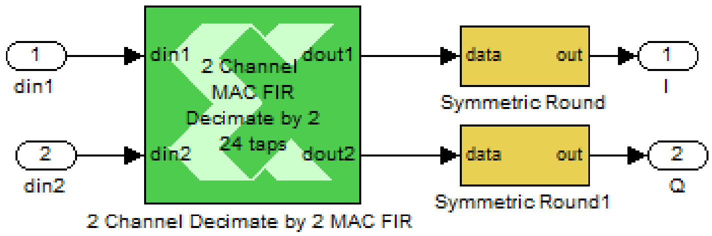

Figure5. Polyphase Decimator $G(z)$

A 24-tap filter is used for the polyphase decimator $G(z)$ while a 96-tap filter is employed for $H(z)$. Here 96 cycles are required to implement this filter.

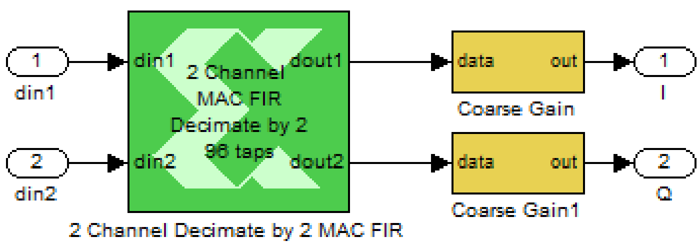

Figure6. Polyphase Decimator $H(z)$

4. HARDWARE IMPLEMENTATION RESULTS & DISCUSSIONS

The proposed DDC is implemented using polyphase decomposition technique to reduce the computational complexity. All required coefficients are divided in two parts by using 2-branch polyphase decomposition. The two branch polyphase structure is shown in Figure7 and can be expressed as:

$$H(z) = E_0(z^2) + z^{-1}E_1(z^2) \tag{1}$$

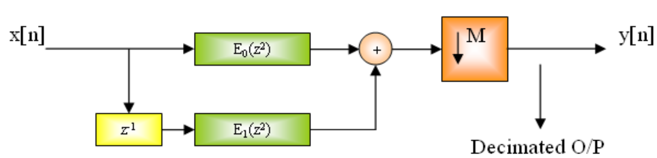

Figure7. Polyphase Structure

The proposed computationally efficient equivalent structure is shown in Figure8. In this structure signal is decimated before filtering which reduces the number of coefficients required to implement the desired filter. This coefficient reduction in turn further reduces the computational complexity of the proposed design.

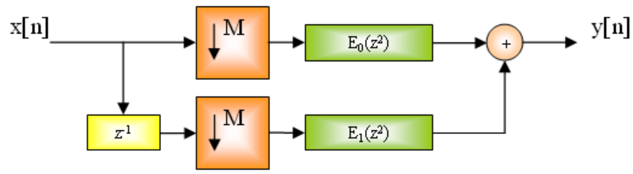

Figure8. Computationally Efficient Structure

The proposed DDC is synthesized and hardware implemented on Virtex-II Pro based xc2vp30-7ff896 target device. The Simulink and System Generator is used to hardware co-simulate the proposed model whose outputs are shown in Figure9.

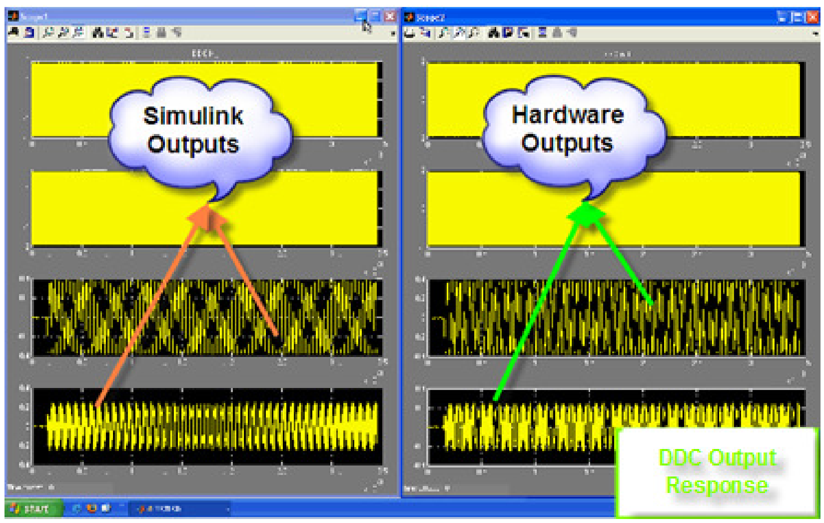

Figure9. Hardware Co-simulation Based DDC Response

The proposed DDC can operate at maximum frequency of 160 MHz by consuming very less resources available on the target device.

Table1. Resource Utilization

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	1638	13696	11%
Number of Slice Flip Flops	2388	27392	8%
Number of 4 input LUTs	1934	27392	7%
Number of bonded IOBs	69	556	12%
Number of BRAMs	9	136	6%
Number of MULT18X18s	4	136	2%
Number of GCLKs	1	16	6%

Table2. Power Consumption

Name	Value	Used	Total Available	Utilization (%)
Clocks	0.06233 (W)	1	---	---
Logic	0.04667 (W)	1979	27392	7.2
Signals	0.12398 (W)	5314	---	---
IOs	0.00077 (W)	69	588	11.7
BRAMs	0.00000 (W)	9	136	6.6
MULTs	0.00202 (W)	4	136	2.9
Total Quiescent Power	**0.10313 (W)**			
Total Dynamic Power	**0.23691 (W)**			
Total Power	**0.34004 (W)**			
Junction Temp	**25.0 (degrees C)**			

5. CONCLUSION

In this paper, an optimized System Generator based hardware co-simulation technique is presented to implement GSM based digital down convertor for software defined radios. Equiripple based polyphase decomposition technique is used to optimize the proposed DDC design in terms of speed and area. The proposed design can operate at maximum frequency of 160 MHz by consuming power of 0.34004 W at 25 °C junction temperature. The proposed model is consuming very less resources on Virtex-II Pro based xc2vp30-7ff896 target device to provide cost effective solution for SDR based 3G & 4G wireless communication applications.

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Authors

Rajesh Mehra: *Mr. Rajesh Mehra is currently Assistant Professor at National Institute of Technical Teachers' Training & Research, Chandigarh, India. He is pursuing his PhD from Panjab University, Chandigarh, India. He has completed his M.E. from NITTTR, Chandigarh, India, B.Tech. from NIT, Jalandhar, India. Mr. Mehra has 14 years academic experience. He has authored more than 25 research papers in national, international conferences and reputed journals. Mr. Mehra's interest areas are VLSI Design, Embedded System Design, Advanced Digital Signal Processing and Wireless & Mobile Communication. Mr. Mehra is life member of ISTE.*

Swapna Devi: *Ph.D in Engineering from Tezpur University, Assam, (2008), she did her M.E. degree from Regional Engineering College (presently NIT), Rourkela, Orissa, in 1997 and B. Tech degree in Electronics & Communication Engineering, NERIST, Arunachal Pradesh, in 1994. Dr. Swapna Devi is currently Associate Professor at National Institute of Technical Teachers' Training & Research, Chandigarh, India. Dr. Swapna has 11 years academic experience. She has authored more than 100 research papers in national, international conferences and reputed journals. Dr. Swapna's interest areas are Medical Image Processing, Soft Computing and Neural Networks. Dr. Swapna Devi is a life member of ISTE, member of IEEE and IETE.*