A High-Swing OTA with wide Linearity for design of self-tunable linear resistor

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ABSTRACT

Low power consumption, long battery life and portability are essential requirements of modern health monitoring products. Operational Transconductance Amplifier (OTA) operating in subthreshold region is an basic building block for low power health monitoring products design. An modified design of OTA which incorporates better linearity and increased output impedance has been discussed in this paper. The proposed OTA uses High-swing improved-Wilson current mirror for low power and low-frequency applications. The achieved linearity is about ± 1.9 volt and unity gain bandwidth (UGB) of 342.30 KHz at power supply of 0.9 volt which makes OTA to consume power in range of nanowatts. The proposed low voltage OTA implementation in design of self- tunable linear resistor has been presented in this paper. The circuit implementation has been done using standard 0.18 micron technology provided by TSMC on BSIM 3v3 level-53 model parameter and verified results through use of ELDO Simulator.

KEYWORDS

Bulk-input, Wilson mirror, Linear range, MOS resistor

1. Introduction

Device sizing is the latest trend in VLSI. Scaling down the channel length in CMOS technology facilitates the submicrometer devices on single IC. Battery operated devices in medical electronics like Ambulatory Brain Computer Interface (ABCI) systems, insulin pumps, hearing aids essentially require low power designs using submicron devices.

Such rapid increase use of battery-operated portable equipment is realized with VLSI (very large scale integrated) technologies. As the technology of biomedical instrumentation amplifier is moving towards portability, lower power consumption is highly desirable for devices which monitors patient whole day.

Small amplitude and low frequency range are special features of biological signals like ECG. In order to process these signals low pass filters are used with sufficient large time constant, typically for a capacitor value of less than 5pF which in turn require very high resistance. For example, in ECG signal detection, low-pass filter required must have cut-off frequency less than 300 Hz for which use of low-power continuous-time OTA-based filters are preferred [1]. However, major limitation of conventional OTAs is its limited linear range. As device sizes are scaling down, traditional saturation-based OTAs are facing design challenges to overcome poor linearity and limited output impedance. Various techniques for extending linear range have been proposed

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among which one is based on source-degeneration and multitanh principle [2]. An alternative method forces to employ diodes as source degeneration elements to extend the linear range [3], but using stacked diodes in series as degeneration elements increases the need of supply voltage. In [4], the OTA uses 21-transistor operating in subthreshold mode gives a linear range of about 700 mV. Since the OTA is a current source device, the output impedance of the device must be high. This work uses the OTA circuit proposed in [5] as reference. The current mirror part of this OTA has been replaced with High-swing improved-Wilson current mirror circuit. The simulation of modified OTA proved considerable improvements in linearity (upto 1.9 volt) as well as sufficient increase in output impedance.

The proposed work has been organized into four sections. Section 2 covers detailed description on working of proposed OTA; based on principle of bulk-driven MOS transistors. Section 3 is detailed on implementation of modified OTA in design electronically tunable linear resistor using MOS. The simulation results and conclusion has been discussed in section 4 and 5 respectively.

2. Proposed OTA

2.1 The referred OTA

The OTA is a transconductance type device, which means that the input voltage controls an output current by means of the device transconductance, labeled g_m . This makes the OTA a voltage controlled current source (VCCS). In the past few years, engineers have improved the linearity of MOS transconductor circuits. Such improvement has been primarily in the area of above-threshold, high-power, high-frequency, continuous time filters. The architecture of OTA is shown in Fig. 1 which provides a linearity of 1.7 volt by combination of four techniques. Firstly, the well terminals of the differential-pair transistors W_1 and W_2 is used as amplifier inputs. Secondly, feedback techniques like source degeneration via S_1 and S_2 transistors whereas gate degeneration via GM_1 and GM_2 provide further improvement. Finally, B_1 and B_2 used as bump transistors. The bump-linearization technique is used to overcome parasitic effects which occur at low input voltage, generally less than 1 volt.

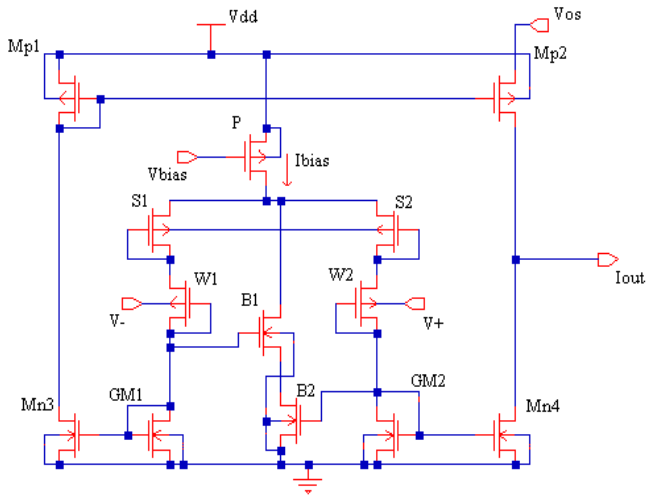

Figure1. Basic OTA [5]

The P transistor act as bias current source and the remaining transistor M_{p1}, M_{p2}, M_{n3} and M_{n4} are configured as simple current mirrors. Besides, there is an offset voltage adjustment which sets V_{OS} around 5 mV less than V_{DD}. To improve OTA performance, simple current mirror used is replaced by complex mirroring, that is, High-swing improved-Wilson current mirror. This technique not only removes the offset voltage adjustment but increases output resistance compared to case of simple current mirror.

The current equation for subthreshold MOS is given as

$$I = I_0 e^{-kV_{gs}/V_T} e^{-(1-k)V_{ws}/V_T} \tag{1}$$

for well-input MOS

$$I \propto e^{-(V_s - gV_w)/V_T} \tag{2}$$

$$\frac{I_{OUT}}{I_B} = \frac{I_d}{I_T} = \frac{I^+ - I^-}{I^+ + I^-} = \frac{e^{-(V_{s2} - gV_{w2})/V_T} - e^{-(V_{s1} - gV_{w1})/V_T}}{e^{-(V_{s2} - gV_{w2})/V_T} + e^{-(V_{s1} - gV_{w1})/V_T}} \tag{3}$$

Solving

$$\frac{I_{OUT}}{I_B} = \frac{e^{gV_d/V_T} - 1}{e^{gV_d/V_T} + 1} = \tanh\left(\frac{gV_d}{2V_T}\right) \tag{4}$$

where $V_d = V_{w2} - V_{w1} = V^+ - V^-$

i.e. $I_{OUT} = I_B \tanh\left(\frac{V_d}{V_L}\right)$ (5)

where I_{out} is the output current, I_B is the bias current of P transistor , V_L is the linear range of OTA expressed as $V_L = 2V_T / g$, where g is the overall reduced transconductance of OTA.

Analyzing the left half-circuit of Fig. 1, the overall transconductance g is reduced by a feedback factor $\left(1 + 1/k_p + 1/k_n\right)$,

i.e. $g = \frac{1-k}{1 + 1/k_p + 1/k_n}$ (6)

where $1/k_p$ and $1/k_n$ are the loop gain of source degeneration and gate degeneration transistor respectively. From $\tanh$ series expansion $\tanh\frac{x}{2} = \frac{x}{2} - \frac{x^3}{24} + ---$; it can be observed that if V_L is made sufficiently high then cubic order term in the $\tanh$ series expansion can be easily neglected thereby reducing distortions of non-linearity.

2.2 High-swing improved-Wilson current Mirror

A current mirror is characterized by the current level it produces, the small-signal ac output resistance and voltage drop across it. The simple current mirror uses the principle that if gate-to-source potentials of two identical MOS transistors are equal then their channel currents are equal.

In late 1967, George Wilson proposed a modified current mirror just by adding one extra transistor which increases output impedance to appreciable amount and named the circuit as Wilson current mirror. The Wilson current mirror implemented using three nMOS transistors is shown in Fig. 2 (a). The architecture consists of simple current mirror and a current to voltage converter connected in the feedback loop. If there is any increase in output current due to output voltage variation, the simple current mirror transistors senses this variation and feed back the current to input node thereby reducing gate voltage of output transistor followed by reduction in original current increase. But these current mirror suffered systematic gain error along with unequal voltages across input and output transistors. To compensate systematic gain error, Barrie Gilbert; added a fourth transistor in diode connected form in the input branch and later this circuit became famous by name improved Wilson current mirror [6] as shown in Fig. 2 (b).

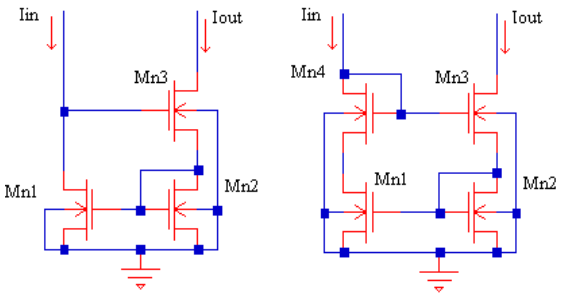

Figure2. (a) Wilson current mirror, (b) Modified Wilson current mirror

These circuits require an input voltage of two diode drops and output compliance voltage incorporates a diode drop plus saturation voltage. Such diode drop made Wilson mirror unattractive for low-power design units. To overcome this, a new Wilson topology was introduced [7], which sense the output current at low input voltage of a diode drop plus a saturation voltage whereas output senses only two saturation voltage. As seen from architecture, the diode connected transistor on input side biased by current source I_b, causes the input voltage to decrease much lower than gate voltage needed as in case of simple mirrors to sink input current. This makes it a low voltage high-swing improved-Wilson current mirror as shown in Fig. 3. The mirror achieves high output resistance by using negative feedback and is directly proportional to the magnitude of the loop-gain of the feedback action from the output current to the gate of output transistor M_{n3}. The transistor M_{n1} and M_{n2} samples the I_{OUT} and compares it with I_{in}. In combination with current source load I_{in}, transistor M_{n1} act as a common source amplifier used to maintain gate voltage of M_{n3} to avoid mismatching of I_{OUT} to I_{in}. Neglecting 2^{nd} order effects, the output resistance r_{out} is approximated as

$$r_{out} \approx g_{m1} r_{o1} r_{o3} \tag{7}$$

where, g_{m1} and r_{o1} are transconductance and output resistance of M_{n1} whereas r_{o3} is output resistance of M_{n3}.

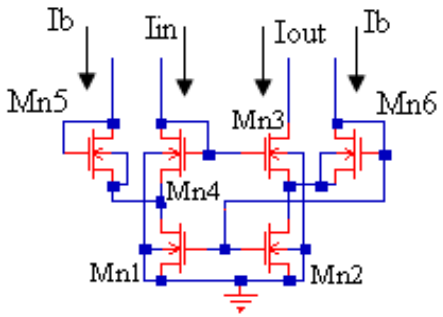

Figure 3. High-swing improved Wilson current mirror

2.3 Modified OTA

The proposed architecture of OTA using high-swing improved-Wilson current mirror is shown in Fig. 4. The architecture works on low supply thereby introducing appreciable reduction in power consumption. A bias current generator circuit is attached to OTA which generates current in the range of nanoamperes.

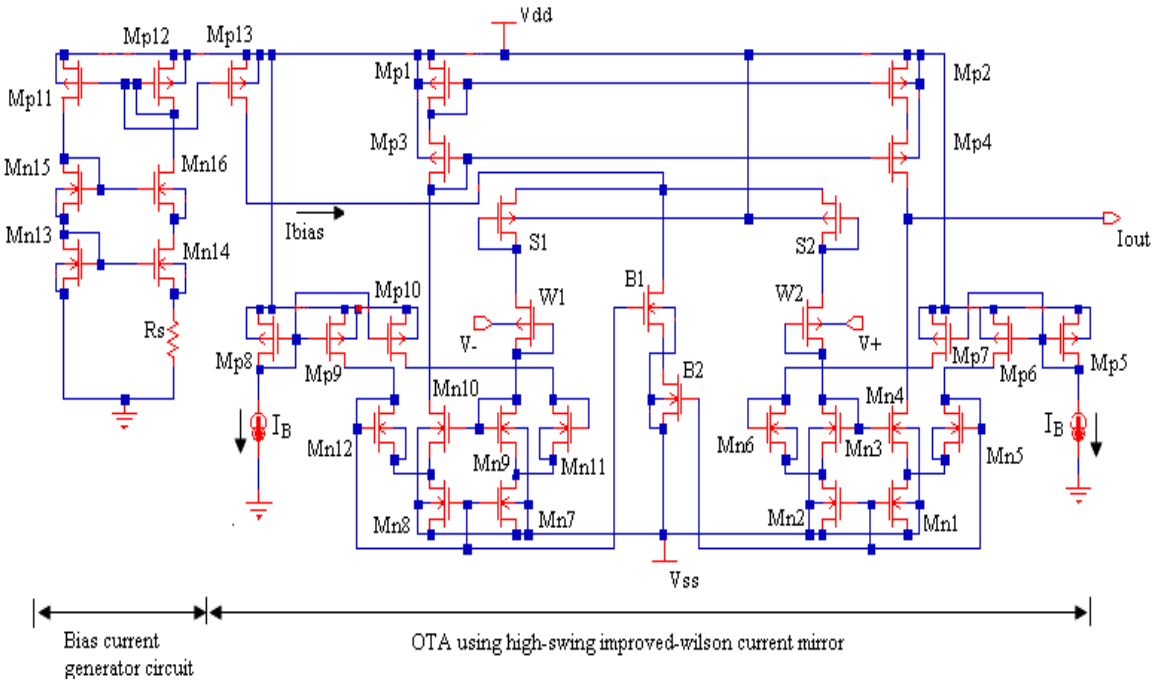

Figure 4. Proposed OTA using High-swing improved Wilson current mirror

Transistors $M_{n13} - M_{n16}$ and $M_{p11} - M_{p12}$ along with R_s comprises current generator circuit. As the source-to-gate voltage of M_{P11} and M_{P12} are equal their corresponding currents are equal, i.e.

$I_{D11} = I_{D12}$ (neglecting channel length modulation). Furthermore, it can be noted that $I_{D13} = I_{D11}$ and $I_{D14} = I_{D13}$.

The equation for drain current of MOS transistor is given by

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_{Tn}\right)^2 \quad (8)$$

Solving for V_{GS}

$$V_{GS} = \sqrt{\frac{2I_D}{\mu_n C_{ox}(W/L)}} + V_{Tn} \quad (9)$$

In Fig. 3

$$V_{GS,n13} = V_{GS,n14} + I_{D,n14}R_S \quad (10)$$

From (10)

$$\sqrt{\frac{2I_{D,n13}}{\mu_n C_{ox}(W/L)_{Mn13}}} = \sqrt{\frac{2I_{D,n14}}{\mu_n C_{ox}(W/L)_{Mn14}}} + I_{D,n14}R_S \quad (11)$$

Rearranging above expression and solving for $I_{D,p12}$ by equating equivalent currents, the $I_{D,p12}$ is given as

$$I_{D,p12} = \frac{2}{\mu_n C_{ox}(W/L)_{Mn13}}\frac{1}{{R_S}^2}\left(1 - \sqrt{\frac{(W/L)_{Mn13}}{(W/L)_{Mn14}}}\right)^2 \quad (12)$$

The output current I_{bias}, that is, $I_{D,p13}$ is now the function of $I_{D,p12}$. By adjusting the aspect ratio of M_{p13} relative to M_{p12}, desired I_{bias} can be obtained. The W/L ratio of M_{p13} is kept four times lower than M_{p12}, which results in output current $I_{D,p13} = I_{bias} = I_{D,p12}/4$.

3. Self-tunable linear resistor using MOS

Electronically tunable linear resistors are highly versatile circuit elements. MOS transistors are generally used for resistor modeling as when it is operated under triode mode behaves as a resistor controlled by its gate terminal voltage. MOS being a four terminal device offers two control parameters that is gate and bulk terminal to control resistor value. Through electronic tuning of gate terminal voltage of MOS transistor, correspondingly electronic control on resistance can be achieved. In the past, MOS resistors with approximately linear I-V characteristics were obtained by operating the transistor in the ohmic (triode) region of strong inversion to exploit the resistive nature of the channel. Generally, these approaches were limited by the small ohmic region and its intrinsic non-linearities. Various techniques have been proposed to minimize nonlinear effects associated with operating the MOS transistor in the ohmic strong inversion regime with good results [8]-[9]. In regard to this, a MOS resistor is used that does not require triode operation [10].

MOS transistor M_R shown in Fig. 5, act as a self-tunable resistor when get tuned by capacitance C connected at its gate terminal.

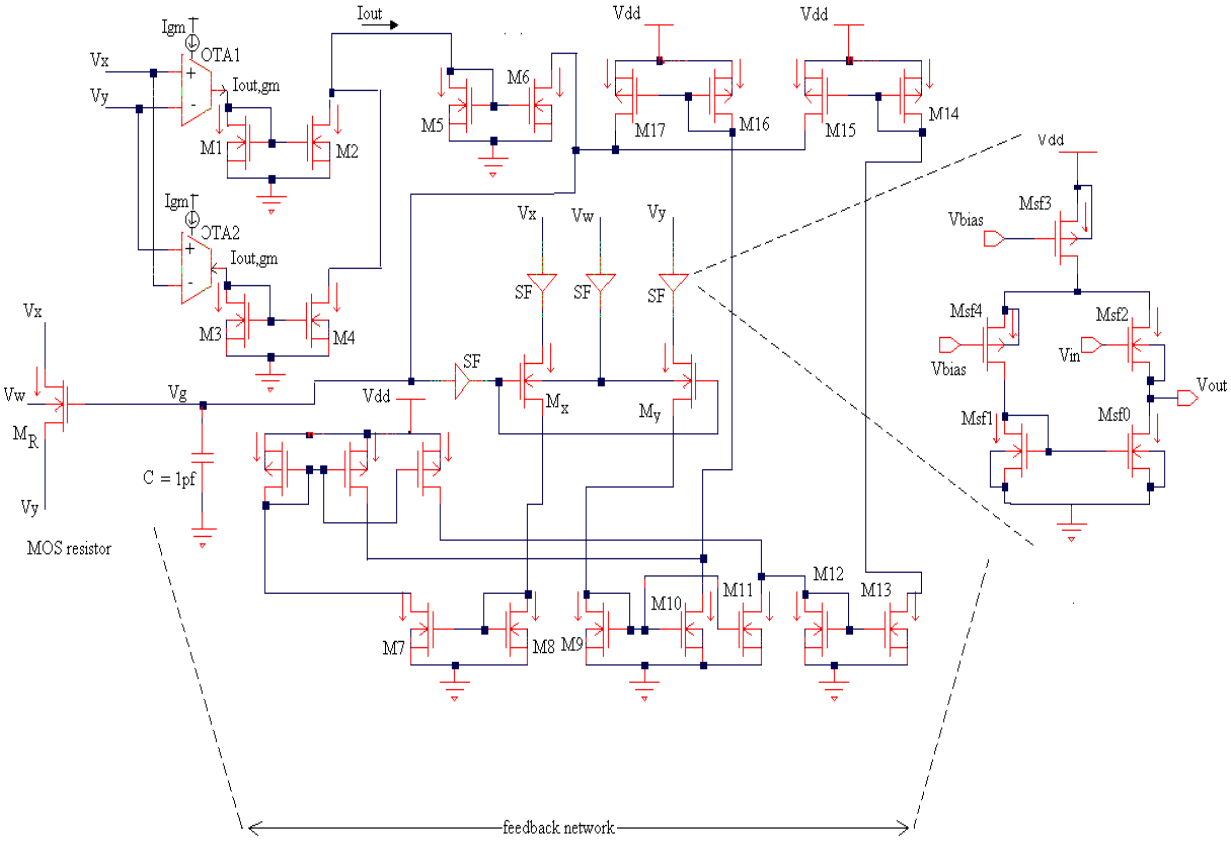

Figure 5. Electronically self-tuned linear resistor using MOS

To maintain resistor characteristics, a feedback network is configured at its gate terminal. The two OTAs, OTA1 and OTA2 have same inputs V_X and V_Y connected to their input terminals in alternative fashion and are biased by the same current source I_{GM}. The potential difference $V_X - V_Y$ across the MOS device M_R is sensed and converted into a current $I_{OUT,GM}$ using a wide linear range low power OTA for which the output current equation is of the form

$$I_{OUT,GM} = G_M \left(V_X - V_Y \right) \tag{13}$$

Where, $G_M \left(= I_{GM} / V_L \right)$ is the transconductance of OTA while I_{GM} and V_L are the biasing current and linear range of the OTA respectively. These OTAs are configured in conjunction with diode connected transistors M1 and M3 to produce two half-wave rectified currents that are proportional to $|V_{XY}|$, voltage across the source-drain terminals of M_R. The rectified output currents are

mirrored via M2 and M4 to create a full wave rectified current. The saturation currents I_{Xsat} and I_{Ysat} of M_R are proportionally replicated by sensing V_G, V_W, V_X and V_Y on the gate, well, source and drain terminals of M_R buffered via source followers and applying potentials V_{GX} and V_{GY} across the gate-source terminals of transistors M_X and M_Y. Transistors M7-M13 serve to compute $I_{Xsat} - I_{Ysat}$ or $I_{Ysat} - I_{Xsat}$ and transistors M14-M17 compare $|I_{Xsat} - I_{Ysat}|$ with a mirrored version of output current using M6. Any difference between these two currents causes the capacitor C to charge or discharge tuning the gate bias voltage V_G which equilibrates at a point where the two are nearly equal via negative feedback action.

To overcome loading effect on terminals of MOS transistor M_R , source follower is employed shown within dotted lines marked as SF in Fig. 5. The source follower has the capability to source and sink large output currents. Its primary use is to buffer signals and provide low output impedance to drive resistive loads while, at the same time handle large output voltage swing and obtain low harmonic distortion. Traditional source have load drive capability limited to the quiescent current in the buffer. In addition traditional source followers require too much power for many applications. To reduce power dissipation (and area) required to reach a given output resistance, composite source follower is used. The composite source follower comprises a current source, PMOS (Msf3) configured to provide a (relatively) constant current to the rest of the circuit, a source follower NMOS (Msf0, Msf2) configured to receive an input signal, a folded cascade device PMOS (Msf4) connected to sense the drain current of the source follower, and a current mirror device NMOS (Msf1) connected to multiply the sensed drain current for application to an output load connected at the source follower output. It provides a four-fold increase in transconductance which offer perfect tracking of input by output having no level shift problem as compared to common voltage buffers. Being less complex circuitry, it is most effetely used in field of low power architectures.

4. Simulation Results

The simulations were performed under normal condition (room temperature) on TSMC 0.18 micron technology using ELDO Spice Simulator. The bias current generator circuit generates I_{bias} of 65nA at $R_S = 10K\Omega$. The supply voltage is kept at 0.9 volt. Fig. 6 shows the transfer characteristics of proposed OTA with enhance linearity to about $\pm$ 1.9 volt with no offset voltage adjustment. Fig. 7 shows the ac response of OTA under no load condition. The achieved phase margin is 55.332 degree and UGB of 342.30 KHz. Its low UGB supports it for use in biomedical applications.

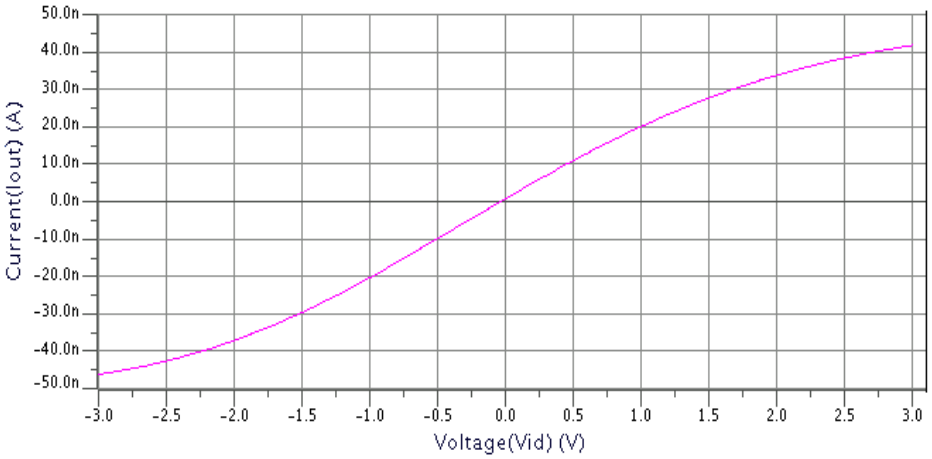

Figure 6. Transfer characteristic of proposed OTA

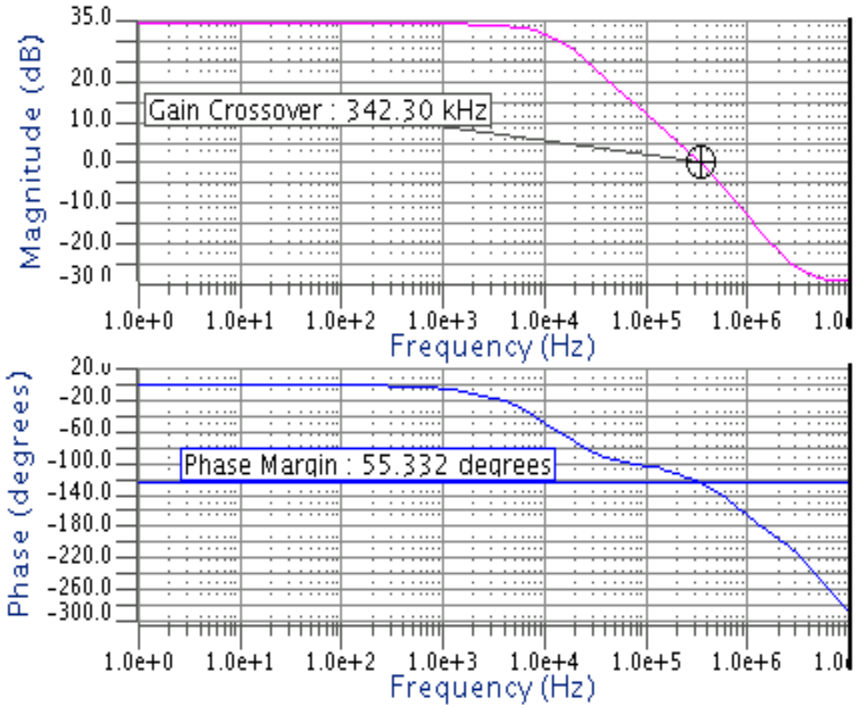

Figure 7. AC response of proposed OTA

When configured as follower integrator using 1 pf of load shown in Fig. 8, it tracks the input perfectly with slight variation at low input voltage, that is, below 0.4 volt. The transfer characteristic of MOS acting as linear resistor is shown in Fig. 9. The value of resistor is varied in accordance to tuning the OTA bias current I_{gm} of OTA used in design.

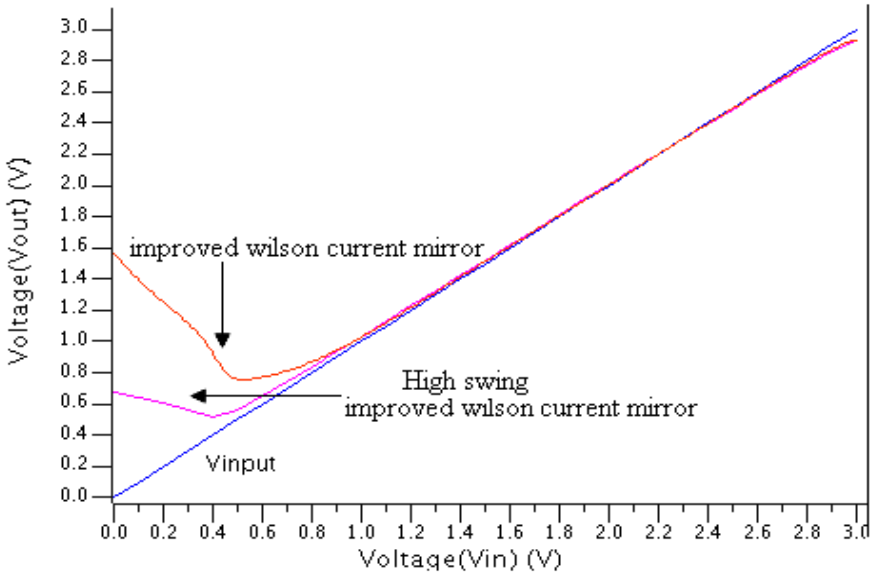

Figure 8. Follower integrator DC characteristics at 1pF load

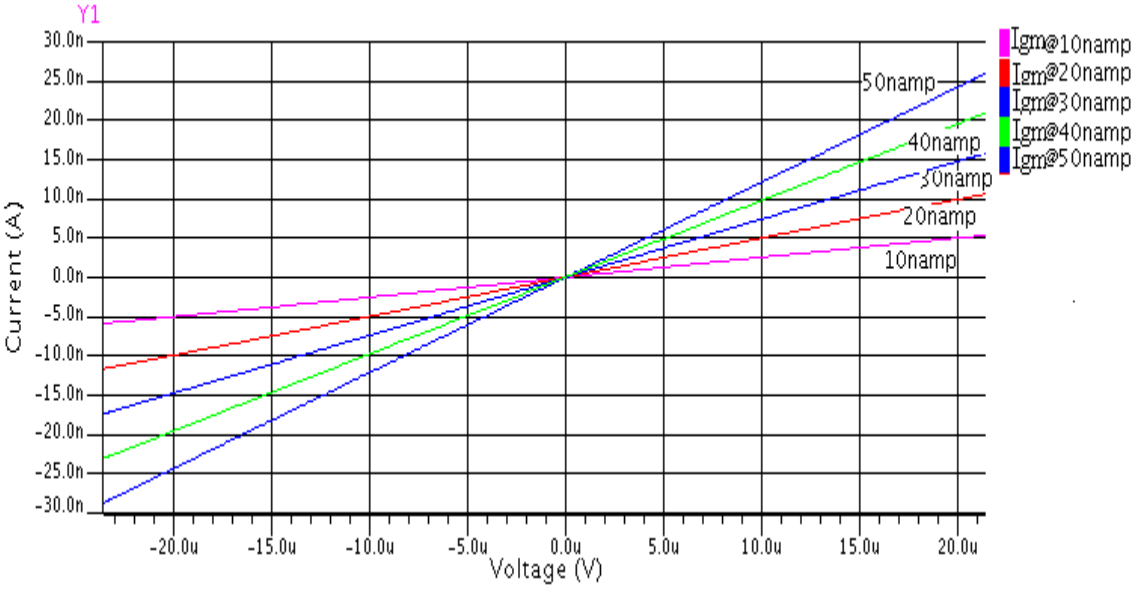

Figure 9. Transfer characteristic of self-tunable linear resistor using MOS

5. Conclusion

This paper explored the approach of low-voltage OTA design using the bulk-driven technique and enhancement of output impedance using high-swing improved-Wilson current mirror. The design of such low voltage, high performance OTA circuit on TSMC 0.18 micron technology satisfies the required parameters for its implementation not only in power-saving devices but also in biomedical portable devices. Further its application in design of tunable MOS resistor find application in variable gain amplifiers, oscillators, balanced resistive bridges and analog filters.

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