Physical Scaling Limits of FinFET Structure: A Simulation Study

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Abstract

In this work an attempt has been made to analyze the scaling limits of Double Gate (DG) underlap and Triple Gate (TG) overlap FinFET structure using 2D and 3D computer simulations respectively. To analyze the scaling limits of FinFET structure, simulations are performed using three variables: fin-thickness, fin-height and gate-length. From 2D simulation of DG FinFET, it is found that the gate-length (L) and fin-thickness (T_{fin}) ratio plays a key role while deciding the performance of the device. Drain Induced Barrier Lowering (DIBL) and Subthreshold Swing (SS) increase abruptly when (L/T_{fin}) ratio goes below 1.5. So, there will be a trade-off in between SCEs and on- current of the device since on-off current ratio is found to be high at small dimensions. From 3D simulation study on TG FinFET, It is found that both fin-thickness (T_{fin}) and fin-height (H_{fin}) can control the SCEs. However, T_{fin} is found to be more dominant parameter than H_{fin} while deciding the SCEs. DIBL and SS increase as (L_{eff}/T_{fin}) ratio decreases. The (L_{eff}/T_{fin}) ratio can be reduced below 1.5 unlike DG FinFET for the same SCEs. However, as this ratio approaches to 1, the SCEs can go beyond acceptable limits for TG FinFET structure. The relative ratio of H_{fin} and T_{fin} should be maximum at a given T_{fin} and L_{eff} to get maximum on-current per unit width. However, increasing H_{fin} degrades the fin stability and degrades SCEs.

Keywords

Double Gate, Triple Gate, Underlap, Overlap, FinFET, High performance (HP), ITRS

1.Introduction

As technologies are scaled down in deep sub-half micron regime, the conventional bulk MOSFET faces several challenges like higher DIBL, poor subthreshold swing collectively known as SCEs [1]. Moreover, the gate oxide thickness has been reached to its physical limit with the scaling i.e. below 1nm [2] and increasing gate leakage current is one of the most challenging tasks for future scaling. It seems impossible to further scale down the gate oxide beyond the inter-atomic distance. Future transistor scaling into the 21st century requires new solutions such as high-k gated dielectric materials and shallow, ultra low resistivity junctions need to be developed [3]. To sustain scaling for the next decade, non-conventional solutions are essentially required. Fully depleted Silicon-On-Insulator MOSFETs have received considerable attention in recent years because of their various advantages such as improved isolation, reduced subthreshold slope and parasitic capacitances and increased drive current. Today, SOI CMOS has entered the mainstream technology due to their improved performance and the availability of low cost SOI wafers. However, for the present generation FDSOI MOSFETs, the problems of increased SCE, poor carrier mobility due to high channel doping and high gate leakage current remain [4]. To overcome these limitations, several innovative multiple gates SOI structures such as Double Gate (DG) MOSFET [5], fully depleted lean channel transistor (DELTA) [6] FinFET [7-10], "Gate All Around" (GAA) MOSFET [11] and Pi-gate MOSFET [12] have been

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proposed by various researchers. It is expected that sustained scaling during the next decade will see the evolution from the single gate (SG) conventional device to the multiple gate MOSFETs (MuGFETs) [4]. Double gate FinFET is a promising candidate because of its quasiplanar structure [8], excellent roll-off characteristics, drive current and it is close to its root, the conventional MOSFET in terms of layout and fabrication [7, 8]. FinFET structure shows less short channel effects than bulk MOSFET because of its self-aligned double gate [13] structure and hence good electrostatic integrity. FinFETs have been demonstrated with both overlap and underlap regions structures [14, 15]. FinFETs with graded or abrupt gate overlaps gives a higher I_{off} as the technologies are scaled down in deep sub-half micron regime [16], because of this, the underlap structure with optimized doping profile in the underlap regions received a considerable attention in the recent years [16, 17, 18]. The rest of the paper is organized as follows - In section-2, device structure under investigation is presented, and section-3 describes the results followed by conclusion in section-4.

2.Device Structure

Fig. 1 shows the DG FinFET structure realized using Setaurus TCAD tool suite [19]. Table I shows the critical device parameters used to fabricate DG underlap FinFET structure given by ITRS [2] for high performance multigate devices for the year of 2015. Based on this specification DG FinFET underlap structure are fabricated and a comparison has been made to analyze the scaling limits. Spacer underlap length (L_{UN}) and source/drain exertion regions (L_{ext}) are kept at 10nm each in order to obtain a good On-off current ratio. Gaussian doping profile is used in underlap regions.

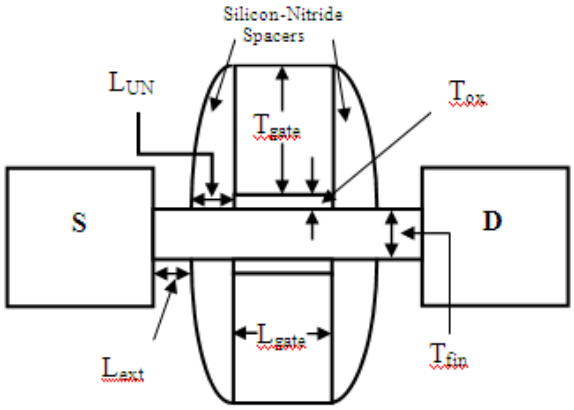

Fig.1 2D Double Gate (DG) FINFET Structure

Table 1
ITRS Projections For High Performance Mg Devices In The Year 2015 [2]

Device Parameters used for DG FinFET	ITRS 2009 Projection
Lg: Physical Gate	17 nm
EOT: equivalent oxide thickness	0.77 nm
V_{dd}: Power supply voltage	0.81 V
Body Thickness	8 nm

The Gaussian profile is selected in order to obtain a fall in doping concentration from 10^{20} cm^{-3} at the source/drain to 10^{16} cm^{-3} at the gate edges. The doping density of source, drain and source/drain extensions are kept at 10^{20} cm^{-3} while channel is doped with a doping concentration of 10^{15} cm^{-3} in order to achieve high mobility in the channel [20]. Workfuction of gate material is adjusted to 4.51 eV in order to analyze the effects of gate dielectric constant variation. Table II shows the critical device parameters used to fabricate TG overlap FinFET structure. Some parameters follows the ITRS specification and some are user define. The Gaussian profile was selected for doping in source, drain and overlap regions. The simulations are performed using the Sentaurus design suite [19] with the drift-diffusion mobility, density-gradient quantum correction modes being turned on for 2D. Hydrodynamic model is used in addition to drift-diffusion mobility and density-gradient quantum correction modes for 3D.

Table 2
Device Parameters Used For TG FinFET

Device Parameters	**Values**
Lg: Physical Gate-length	47 nm
L_{eff}: Effective Gate-length	37 nm
Source and Drain overlaps	5 nm each
EOT: equivalent oxide thickness	1.5 nm
V_{dd}: Power supply voltage	1V
Lateral steepness of profile	3.2 nm/decade
Gate Workfunction	4.46 eV
T_{fin}	5-30 nm
H_{fin}	5-30 nm

3.Results and Discussion

3.1 Effects of gate-length variation on DG FinFET structure

Fig. 3 depicts threshold voltage variation with the gate-length. DG underlap FinFET shows a well known effect “Threshold voltage roll-off”. The distance between drain and source reduces with the gate-length and hence the channel potential is now more pronounced to the drain electric field. So, the gate potential required to invert the channel is reduced because of the drain electric field encroachment on the channel region increases with decreased gate-length.

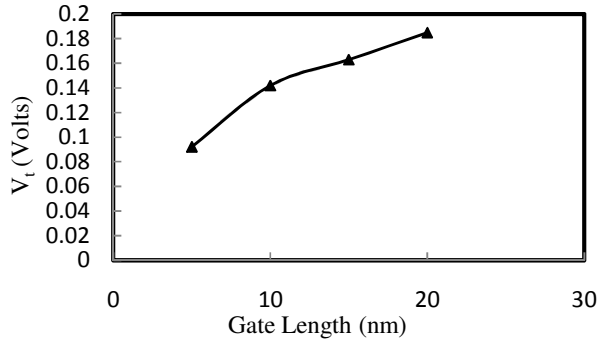

Fig. 2 Threshold voltage variation with gate-length

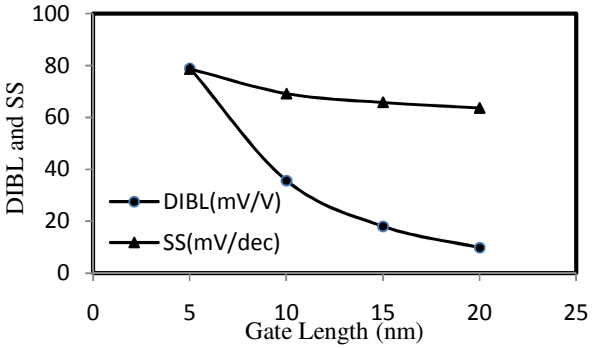

Fig. 3 Short Channel Effects variation with gate-length

Fig.3 depicts Short Channel Effects (SCEs) variation with the gate-length. DIBL increases very sharply with decreased gate-length. The drain electric field encroachment on channel region increases at shorter gate-lengths. Subthreshold swing also increases with decreased gate-length. The gate now has less control over channel in subthreshold region because of the channel barrier potential is now controlled by the drain potential also.

3.2 Effects of fin-thickness variation on DG FinFET structure

Fig. 4 shows the threshold voltage variation with the fin-thickness. Threshold voltage reduces with increased fin-thickness. At shorter channel lengths, the surface potential depends not only on capacitive coupling between the gate and the channel region but also on the capacitance of source/fin and drain/fin junction. As the fin-thickness increases, the width of the source/fin and drain/fin depletion region increases, which decreases the source/fin and drain/fin junction capacitances, as a result the gate to surface potential coupling increases [24] and hence the threshold voltage decreases with the increased film thickness.

Fig.5 shows Short Channel Effects (SCEs) variation with fin-thickness. Fin-thickness plays a very important role while deciding SCEs. DIBL increases with increased fin-thickness. Drain electric field lowers the barrier of channel in case of thick silicon film devices because of reduced source/fin and drain/fin junction capacitances. Subthreshold swing also increases with

fin-thickness. The reason behind this is the gate control over channel region degrades with increased channel volume at constant drain and source proximity.

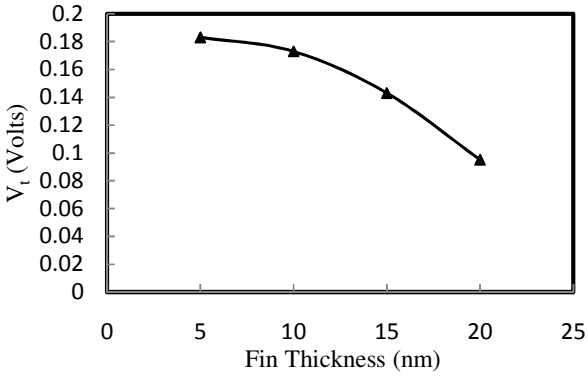

Fig. 4 Threshold voltage variation with fin-thickness

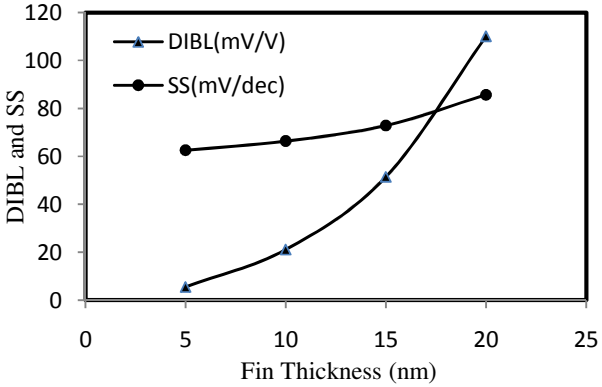

Fig. 5 Short Channel Effects variation with fin-thickness

3.3 Scaling limits of DG FinFET structure

Fig. 6 shows the effect of the ratio of gate-length (L) and fin-thickness (T_{fin}) on DIBL. This ratio limits the scaling of DG FinFET structure. DIBL and subthreshold swing (SS) increases abruptly when the L/T_{fin} ratio fall below1.5. This ratio is a most important factor which decides the short channel effects. For DG FinFET structure fin-thickness could be a dominating factor which decides the scaling capabilities.

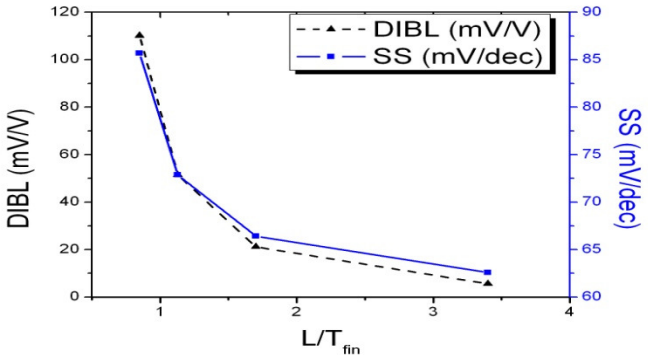

Fig. 6 Short Channel Effects variation with (L/T_{fin}) ratio

3.4 Effects of fin-thickness variation on TG FinFET structure

Fig. 7 depicts the threshold voltage variation with the fin-thickness. Threshold voltage reduces with fin-thickness. The drain electric field lowers the channel barrier as we increases fin-thickness because the channel area under the buried oxide (BOX) increases and hence drain electric field induce more inversion charge at the bottom of silicon fin. There is a sharp rise in the threshold voltage from 10nm to 5nm fin-thickness. It may be due to quantum mechanical effects because below 10nm quantum effects dominates and cannot be neglected [25].

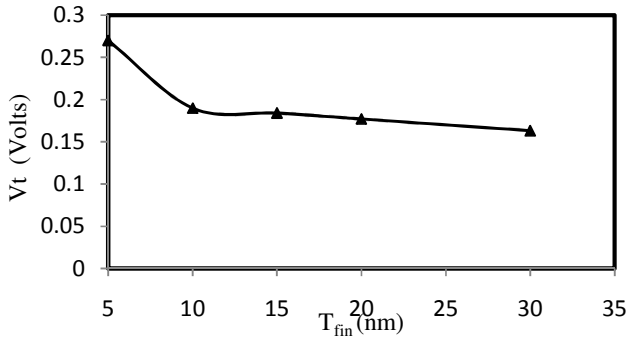

Fig. 7 Threshold voltage variation with the fin-thickness at 30nm of H_{fin}

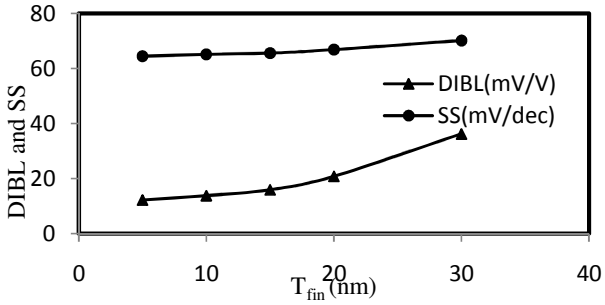

Fig. 8 Short Channel Effects variation with fin-thickness at 30nm of H_{fin}

Fig. 8 shows SCEs variation with the fin-thickness. DIBL increases with fin-thickness. The drain electric field lowers the channel barrier as we increases fin-thickness because the channel area under the BOX increases and hence drain electric field coupling with the channel increases. Subthreshold swing also increases with fin-thickness. The reason is same as explained above. The major portion of subthreshold current flows through the bottom layer of silicon fin because of DIBL.

3.5 Effects of fin-heights variation on TG FinFET structure

Fig.9 depicts the threshold voltage variation with the fin-height. Threshold voltage reduces with fin-height. At shorter channel lengths, the surface potential depends not only on capacitive coupling between the gate and the channel region but also on the capacitance of source/fin and drain/fin junction. As the fin-height increases, the width of the source/fin and drain/fin depletion region increases, which decreases the source/fin and drain/fin junction capacitances, as a result the gate to surface potential coupling increases and hence the threshold voltage decreases with increased fin- height.

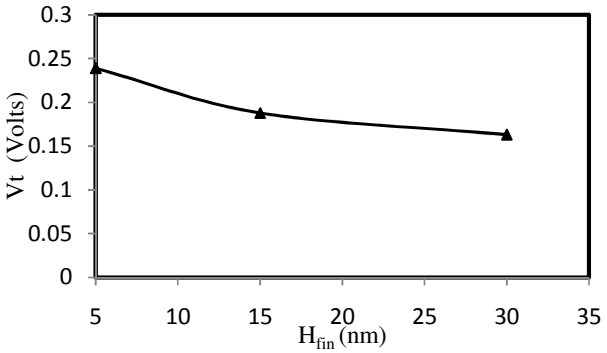

Fig. 9 Threshold voltage variation with the fin-height at 30nm of T_{fin}

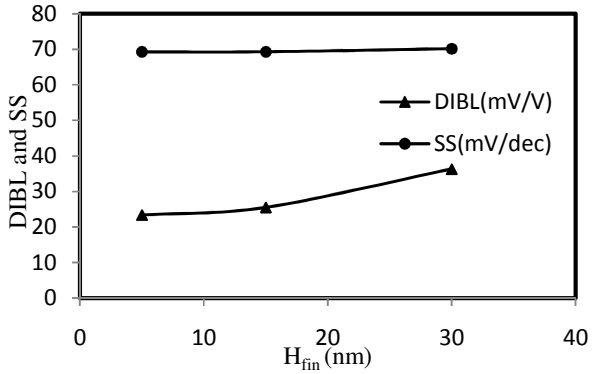

Fig. 10 Short Channel Effects variation with fin-height at 30nm of T_{fin}

Fig. 10 shows SCEs variation with the fin-height. DIBL increases with the fin-height. The drain electric field lowers the channel barrier as we increases fin-height. Subthreshold swing also increases with fin-height. Gate loses its control over the channel with increased fin-height.

3.6 Scaling limits of TG FinFET structure

Fig. 11 shows the effects of the ratio of effective gate-length (L_{eff}) and fin-thickness (T_{fin}) on SCEs. DIBL and subthreshold swing (SS) increases as (L_{eff}/T_{fin}) ratio decreases. This ratio can be reduced to less than 1.5 unlike DG FinFET for the same SCEs. However, as this ratio approaches to 1 value the SCEs can go beyond acceptable limits. So, the scaling capabilities of TG FinFET structure is more than that of DG FinFET structure.

Fig. 12 shows the effects of the ratio of effective gate-length (L_{eff}) and fin-height (H_{fin}) on SCEs. DIBL and subthreshold swing (SS) increases as (L_{eff}/T_{fin}) ratio decreases, however, the increment is less than that with the ratio (H_{eff}/T_{fin}). The reason behind this is that the fin-thickness is more prone to the SCEs than the fin-height. Fin-height can be increased to achieve higher on-current than that of fin-thickness with an acceptable value of SCEs.

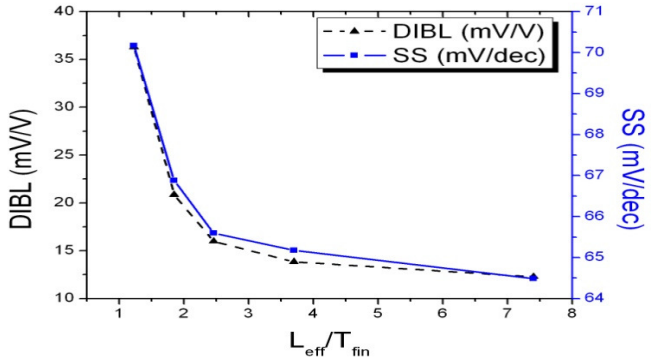

Fig. 11 Effects of (L_{eff}/T_{fin}) ratio variation on SCEs at 30nm of H_{fin}

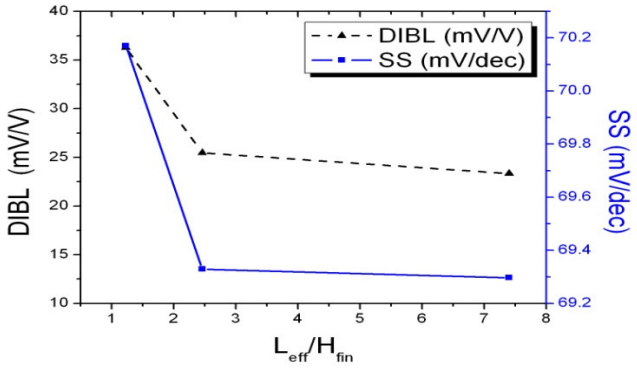

Fig. 12 Effects of (L_{eff}/H_{fin}) ratio variation on SCEs at 30nm of T_{fin}

4.Conclusions

In this work, the scaling capabilities of DG and TG FinFET devices are analyzed using 2D and 3D simulation respectively. The (L_{eff}/T_{fin}) ratio limits the scaling capabilities FinFET structure. This ratio is found to be less in case of TG FinFET structure for acceptable SCEs. Simulation

results shows that TG FinFET structure is more scalable than that of DG FinFET structure. The relative ratio of H_{fin} and T_{fin} should be maximum at a given T_{fin} and L_{eff} to get maximum on-current per unit width. However, increasing H_{fin} degrades the fin stability, increases the difficulty of gate patterning and degrades SCEs. Carefully optimization of T_{fin} and H_{fin} is essentially required to get a good performance for scaled FinFET structure at a given gate length.

5.Acknowledgement

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6.References

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