Design of a high frequency low voltage CMOS operational amplifier

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ABSTRACT

A method is presented in this paper for the design of a high frequency CMOS operational amplifier (Op-Amp) which operates at 3V power supply using tsmc 0.18 micron CMOS technology. The OPAMP designed is a two-stage CMOS OPAMP followed by an output buffer. This Operational Transconductance Amplifier (OTA) employs a Miller capacitor and is compensated with a current buffer compensation technique. The unique behaviour of the MOS transistors in saturation region not only allows a designer to work at a low voltage, but also at a high frequency. Designing of two-stage op-amps is a multi-dimensional-optimization problem where optimization of one or more parameters may easily result into degradation of others. The OPAMP is designed to exhibit a unity gain frequency of 2.02GHz and exhibits a gain of 49.02dB with a 60.5^0 phase margin. As compared to the conventional approach, the proposed compensation method results in a higher unity gain frequency under the same load condition. Design has been carried out in Tanner tools. Simulation results are verified using S-edit and W-edit.

KEYWORDS

CMOS Analog Circuit, Operational amplifier, Current Buffer Compensation, High Frequency, Low Voltage

1. INTRODUCTION

Over the last few years, the electronics industry has exploded. The largest segment of total worldwide sales is dominated by the MOS market. Composed primarily of memory, micro and logic sales, the total combined MOS revenue contributed approx 75% of total worldwide sales, illustrating the strength of CMOS technology [10]. CMOS technology continues to mature with minimum feature sizes now. Due to relatively simple circuit configurations and flexibility of design, CMOS technology has an edge over NMOS technology and is gaining rapid acceptance as the future technology for linear analog integrated circuits, especially in the telecommunication field.

Operational amplifiers (usually referred to as OPAMPs) are key elements in analog processing systems. OPAMP can be said to be the main bottleneck in an analog circuit. Ideally they perform the function of a voltage controlled current source, with an infinite voltage gain. Operational amplifiers are an integral part of many analog and mixed-signal systems. OPAMPs with vastly different levels of complexity are used to comprehend functions ranging from dc bias generation to high-speed amplification or filtering. The design of OPAMPs continues to pose a challenge as the supply voltage and transistor channel lengths scale down with each generation of CMOS technologies [4].

Designing high-performance analog integrated circuits is becoming increasingly exigent with the relentless trend toward reduced supply voltages. At large supply voltages, there is a tradeoff

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among speed, power, and gain, amid other performance parameters. Often these parameters present contradictory choices for the op-amp architecture. Speed and accuracy are two most important properties of analog circuits, however optimizing circuits for both aspects leads to contradictory demands. The realization of a CMOS OPAMP that combines a considerable dc gain with high unity gain frequency has been a difficult problem. There have been several circuit approaches to evade this problem. The simulation results have been obtained by tsmc 0.18 micron CMOS technology. Design has been carried out in Tanner tool. Simulation results are verified using S-edit and W-edit.

The generic block diagram of the circuit is shown in the figure 1.

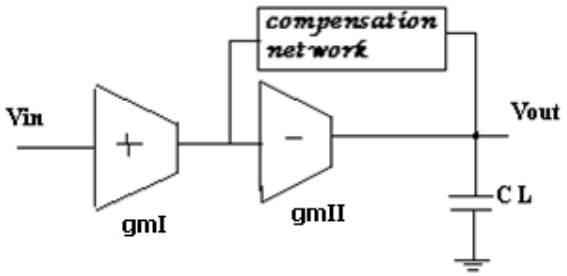

Figure 1: Block diagram of a Miller compensated two-staged operational amplifier

2. RELATED WORK

The two-stage CMOS OPAMP is a widely used analog building block in many OPAMP design literatures which is a simple and robust topology providing good values for most of its electrical parameters. Despite its popularity, only uncompleted design procedures were proposed for this OTA which arbitrarily reduces the degree of freedom in the design equations, hence preventing the possibility to meet optimized performance [7, 12]. Of course, there are electrical parameters which can be improved with appropriate circuit arrangements. For instance, a high drive capability can be achieved by employing class AB instead of class A topologies [13-15]. A two-stage CMOS OPAMP design procedure suitable for pencil-and-paper analysis is given by Palmisano, Palumbo and Pennisi [3].This procedure is allowed to use the limited range of compensation capacitor (condition for compensation is, $C_C >> Cgs_5$). Here C_C is the compensation capacitor and Cgs_5 is a parasitic capacitor of MOSFET in the OPAMP second stage. Mahattanakul and Chutichatuporn [18] have improved the design procedure that allows the C_C a wider range, which would provide a higher degree of freedom in the trade-off between noise and power consumption. Pugliese, Cappuccino and Cocorullo [19] proposed a design procedure for settling time minimisation in multistage OPAMPs with low power and high accuracy level. Design procedures reported in literatures have not given much attention to the improvement of the unity gain frequency of OPAMPs. There are several limitations which come into the forefront in the existing approaches when an OPAMP is needed to operated at a high frequency. In the approach by R.K Baruah [24], although the designed OPAMP worked at a low power and low voltage, but it presented a very low unity gain frequency. Although the simulation [26]done in HSPICE shows an operation at a low power supply and consumes lesser power, but still the increase that is observed in the unity gain frequency cannot be considered to be noteworthy. The research work [27] insists the incorporation of pseudo-cascode compensation instead of Miller compensation to increase the unity gain frequency up to 450MHz. But it is seen that this approach degrades the phase margin with the increase of unity

gain frequency. The multi-stage design [28] improves the settling time and gain but leads to the decrease of the phase margin and unity gain frequency. Again, as the supply voltage decreases, it also becomes increasingly difficult to keep the transistors in saturation with the voltage headroom available [25].Also, settling the time parameter of an OPAMP has to be worked with. Moreover, in these procedures, the effect of capacitive load on unity gain frequency, speed, power and noise balancing altogether is not considered. In this work, an OPAMP has been designed which exhibits high unity gain frequency for optimised balancing of phase margin, gain, speed, power, noise and load. A method is proposed to set a higher unity gain frequency of the OPAMP working at a lower supply voltage. This allows the value of each circuit element of the amplifier (i.e transistor aspect ratios, bias current and compensation capacitor) to be univocally related to the required electrical parameters.

3. THE VARIOUS STAGES INCORPORATED IN THE DESIGN

Simultaneously optimizing all parameters in a design has become obligatory now-a-days. In the past few years, various new-fangled topologies have evolved and have been employed in various applications. Here we have chosen a simple differential pair amplifier (high noise immune) for input amplifier, common source amplifier (high gain) for output amplifier, a current mirror circuit (free from voltage sources; utilizing single current reference source) as a biasing circuit, and a current buffer compensation circuit in conjunction with a Miller capacitance in series with one another.

The topology of the circuit designed is that of a standard CMOS op-amp. It comprised of three subsections of circuits, namely differential gain stage, second gain stage and bias strings. Examining the subsections further will provide valuable insight into the operation of this amplifier.

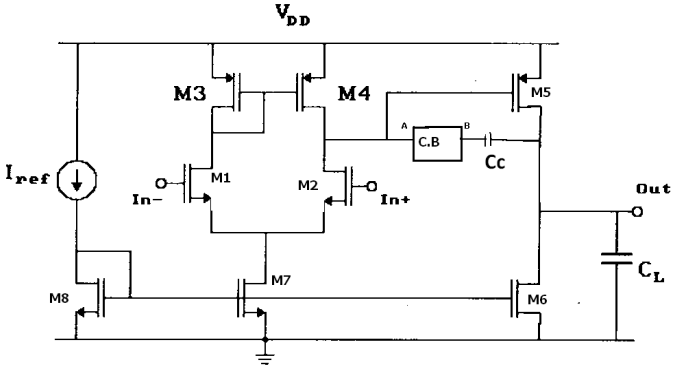

Figure 2: Two stage OPAMP with the compensation block

3.1. Differential Gain Stage

The first subsection of interest is the differential gain stage which is comprised of transistors M1 to M4. Transistors M1 and M2 are standard N channel MOSFET (NMOS) transistors which form the basic input stage of the amplifier. The gate of M1 is the inverting input and the gate of M2 is the non-inverting input. A differential input signal applied across the two input terminals will be amplified according to the gain of the differential stage. The transconductance of this stage is simply the transconductance of M1 or M2. M3 and M4 are the active load transistors of the differential amplifier. The current mirror active load used in this circuit has three distinct advantages. First, the use of active load devices creates a large output resistance in a relatively

small amount of die area. The current mirror topology performs the differential to single-ended conversion of the input signal, and finally, the load also helps with common mode rejection ratio.

3.2. Second Gain Stage

The purpose of the second gain stage, as the name implies, is to provide additional gain in the amplifier. Consisting of transistors M5 and M6, this stage takes the output from the drain of M2 and amplifies it through M5 which is in the standard common source configuration. Again, similar to the differential gain stage, this stage employs an active device, M6, to serve as the load resistance for M5. The transconductance of this stage is the transconductance of M6.

3.3. Bias String

The biasing of the operational amplifier is achieved with only three transistors along with a current source. Transistor M8 and the current source supply a voltage between the gate and source of M7 and M6. Transistors M6 and M7 sink a certain amount of current based on their gate to source voltage which is controlled by the bias string. M8 is diode connected to ensure it operate in the saturation region. Proper biasing of the other transistors in the circuit (M1 – M5) is controlled by the node voltages present in the circuit itself. Most importantly, M5 is biased by the gate to source voltage (V_{GS}) set up by the V_{GS} of the current mirror load as are the transistors M1 and M2.

4. THE DESIGN APPROACH

Few decades ago voltage biasing was primarily in use, but now-a-days, it is the current biasing which is dominating, due to its various advantages. MOS devices when operate in saturation region, their current is almost constant (neglecting lambda effect). A voltage generally produces flow of electron in a material (metal and semiconductor). Same way when a current flows through a material it produces voltage across it. This concept is the core of current mirror circuits. In this current mirror circuit, I_{ref} is a current source which is considered to be an ideal current source.

This work presents a design that illuminates the speed and gain recompense of two a two-stage OPAMP along with high unity gain frequency. This work deals with ingenious design criterion for two-stage CMOS transconductance operational amplifiers. A novel and simple design procedure is presented, which allows electrical parameters to be univocally related to the value of each circuit element and biasing value. This design yields an accurate performance optimization eliminating unnecessary circuit constraints. Bandwidth optimization strategies are also discussed. SPICE simulations based on the proposed procedures are given which closely consent the expected results.

At the very onset of the design, the differential amplifier bias current (I_{ss}) is selected considering the gain, CMRR, power dissipation, noise, unity gain frequency and slew rate matching considerations. The small signal gain of the differential amplifier is given by—

$$A_1 = g_{m1}(r_{01} || r_{02})$$

Where, g_{mI} is the transconductance of the first stage. In addition to selecting I_{ss}, the V_{GS} of the transistors are also determined, which is an iterative process verifying the characteristics. The next step in the design is the selection of the second-stage biasing current. The considerations that were applied in the selection of the differential biasing current are also applied in the

selection of the second-stage biasing current. With both inputs to the OPAMP at the same potential, the same current flows in M3 and M4. The result is that, the drain of M4 is at the same potential as its gate. The sizes of M5 and M6 are calculated based on the current that flows to it. The next step is to select the compensation network for the OPAMP.

Two-stage CMOS operational amplifiers adopt Miller compensation to achieve stability in closed-loop conditions. To steer clear of closed-loop wavering, compensation is necessary in OPAMP design [1],[7]. For two-stage OPAMP, the simplest compensation skill is to connect a capacitor across the high gain stage. This results in the pole splitting phenomena which improves the closed loop stability significantly. Nevertheless, due to the feed forward path through Miller Capacitor, a right half plane zero is also created, which can be nullified by using current buffer compensation in conjunction with the compensation capacitor. Unfortunately, this compensation is responsible for a right half-plane zero in the open-loop gain, which is due to the forward path through the compensation capacitor to the output. An uncompensated right half-plane zero radically reduces the maximum achievable gain-bandwidth product, since it makes a negative phase contribution to the open-loop gain at a relatively high frequency. As a consequence, in the design of two-stage operational amplifiers, compensation of the right half-plane zero is mandatory. After compensation of the right half plane zero, the maximum achievable gain -bandwidth product is limited by the phase margin, Ø, we must properly set the ratio of the second pole, W_{p2} to the gain bandwidth product, W_{GBW} which is equal to the tangent K of the phase margin.

$$K = \tan(\emptyset) = \frac{W_{p2}}{W_{GBW}} \qquad 1$$

Again, it is also seen that W_{GBW} depends on the transconductance of the first stage, g_{mI} and on the compensation capacitance C_C and is related by the equation-

$$W_{GBW} = \frac{g_{mI}}{C_c} \qquad 2$$

There are diverse techniques for compensation of the right half plane zero in two-stage CMOS OPAMP that have been proposed. The simplest was the simple RC Miller compensation technique. The main purpose was to break the forward path through the compensation capacitor by using a nulling resistor in series with the compensation capacitor, which was the most popular compensation technique. It could also be implemented using only a MOS transistor biased in the triode region. In contrast, techniques employing buffers show complicated performance due to additional poles and zeroes introduced by the output and input finite resistance in the voltage and current buffers respectively. Both voltage and current buffers can be adopted for compensation of right-half plane zero [23]. But, the current buffer compensation proves to be more efficient when performance at high frequency is to be considered.

4.1. Enhancement in frequency using Current buffer

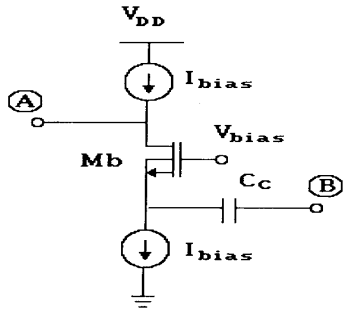

Figure 3: Current buffer compensation block

The current buffer compensation block, when used in the two-stage operational amplifier circuit as a compensation technique in place of the nulling resistor compensation, seems to be very efficient for gain-bandwidth performance. The compensation technique of current buffer approach uses a current buffer to break the forward path through compensation branch [6]. Considering an ideal current buffer in the compensation branch in place of the nulling resistor, the second pole frequency [9], [11] is-

$$. W_{p2} = \frac{g_{mII}}{\left\{C_L\left(1+\frac{C_{01}}{C_C}\right)\right\}} \qquad 3$$

This leads to a compensation capacitor [9] and can be expressed as-

$$C_C = \left(\frac{g_{mI}}{2g_{mII}}\right)K\left[1+sqrt\left\{1+\frac{4g_{mII}C_L}{Kg_{mI}C_{01}}\right\}\right]C_{01}$$

$$or \qquad C_{C=}\left(\frac{g_{mI}}{2g_{mII}}\right)KC_{01}+sqrt\left\{\left(\frac{g_{mI}}{g_{mII}}\right)KC_{01}C_L\right\}$$

Where, g_{mII} is the transconductance of the second stage, C_L is the load capacitor; C_{01} is the equivalent capacitance on the output of the first stage. Substituting (2) & (3) in (1), approximating, and solving for C_C, we get,

$$C_{C=}\left(\frac{g_{mI}}{2g_{mII}}\right)KC_L$$

Various authors have worked on settling time modelling in OPAMPs (Yavari, Magari and Shoaei [22]; Yavari and Shoaei[16]) Yavari developed an accurate model for both positive and negative slew rate of OPAMP. Two distinct periods determine the settling time: the slewing period and the linear settling period. During the slewing period, the variation rate of the output is limited to a maximum value (slew rate). This is originated in the charging of a capacitive node with a limited current. During the linear settling period the output voltage settles to its final value in a small-signal linear fashion. In this work, the model of the settling time developed by Turchetti [20] has been used because of its simplicity.

As per this model,

$$T_{set} = T_{s1}+T_{s2}$$

Where,

$$T_{s1} = \frac{V_1}{SR} - \frac{1}{\omega_u}$$

And

$$T_{s2} = \frac{2}{\omega_{nd}} ln \frac{SR}{XV_1\sqrt{\omega_{nd}\omega_u}}$$

Here, T_{set} is the total settling time defined as the time required for the output response to remain within error tolerance voltage (X). T_{s1} is the slewing period of the settling time, T_{s2} is the linear settling period, ω_{nd} is the non-dominating frequency of two pole amplifier, ω_u is the unity gain frequency, SR is the slew rate and V_1 is the amplitude of applied step input. Yang and Allstot [21] gave a relationship between the error tolerance voltage (X) and the damping factor (k) for a two pole system.

$$X = \exp\left[\frac{-k\pi}{\sqrt{1-k^2}}\right]$$

For a two pole system, pole separation defined by parameter Q is half of the inverse of the damping factor

$$Q = \frac{1}{2k}$$

Further Q can be expressed as: (Johns and Martin [17]) where β is feedback factor and will be unity to analyse the settling behaviour of the OPAMP.

$$Q = \sqrt{\frac{\beta\omega_u}{\omega_{nd}}}$$

The slew rate performance of the amplifier depends on the slews on both the output node of the differential amplifier stage and the output node of the second stage (i.e. the output node of the OTA) to which we refer as internal and external slew rate respectively. These slew rates are related to the quiescent current $I_{D1,2}$ and I_{D6} according to[3]—

$$SR_{INT} = \frac{2I_{D1,2}}{C_C}$$

$$SR_{EXT} = I_{D6} - \frac{2I_{D1,2}}{C_L}$$

In order to satisfy slew rate performance, we can set SR_{INT}= SR_{EXT}= SR (targeted) and get

$$I_{D1,2} = \frac{SR \times C_C}{2} \qquad 4$$

$$I_{D6} = SR(C_C + C_L)$$

From equation (4), the aspect ratio of transistor M1 and M2 are calculated as

$$\left(\frac{W}{L}\right)_{1,2} = \frac{g_{m1,2}^2}{4K_N I_{D1,2}}$$

Where,

$$K_{N,P} = \frac{\mu_{N,P} C_{OX}}{2}$$

Solving the proposed circuit for small-signal equivalent model, we get-

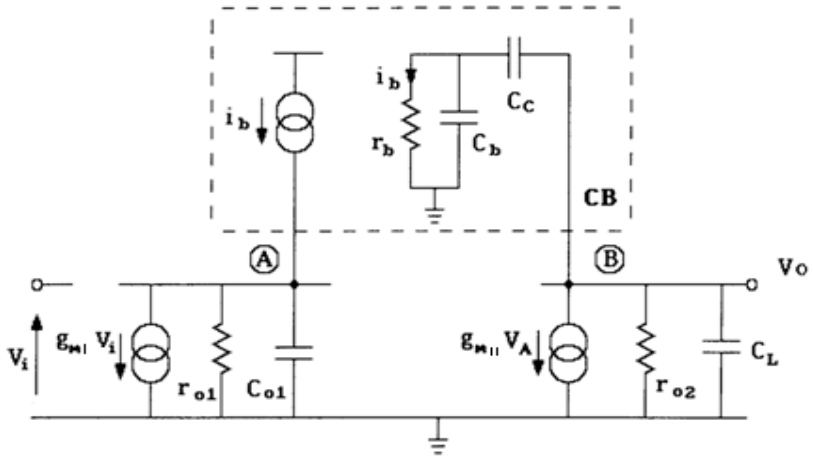

Figure 4: Small signal model of two-stage OPAMP using current buffer compensation.

Analyzing the circuit, the parameters of the small signal model are calculated to be---

$$g_{mI} = g_{m1,2}$$

$$g_{mII} = g_{m6}$$

$$r_{01} = r_{ds2} || r_{ds4}$$

$$r_{02} = r_{ds5} || r_{ds6}$$

$$C_{01} = C_{gd2} + C_{gd4} + C_{gs5} + C_{db2} + C_{db4}$$

$$C_{02} = C_{gd6} + C_{db5} + C_{db6} + C_L$$

From the small-signal equivalent model, the gain of the operational amplifier can be calculated using the following equation—

$$A_0 = g_{m1}r_{o1} \times g_{mII}r_{o2}$$

or

$$A_0 = (g_{m1}g_{m5})/\{(g_{ds2} + g_{ds4})(g_{ds5} + g_{ds6})\}$$

5. SIMULATION RESULTS

In order to corroborate the proposed compensation strategy, the two-stage OPAMP in the figure was designed using the model parameter of tsmc0.18 micron CMOS process. The design parameters along with the electrical parameters yielded are as given in the table1. This circuit operates efficiently in a closed loop feedback system, while high bandwidth makes it suitable for high speed applications. The circuit operating conditions includes the room temperature as the operating temperature with a power supply of 3V and a load of 10fF.

For the frequency response plot, an ac signal of 1V is swept with 5 points per decade from a frequency of 10KHz to 4GHz. Fig.5 illustrates the frequency response which shows a dc gain in dB versus frequency in Hz(in log scale) and phase margin of OPAMP in open loop. The dc gain is found to be 49.02dB and phase margin 60.5^0 which is good enough for an OPAMP operating at a high frequency. A unity gain frequency of 2.02GHz is excellent for an OPAMP when all the other parameters are also set at an optimised value.

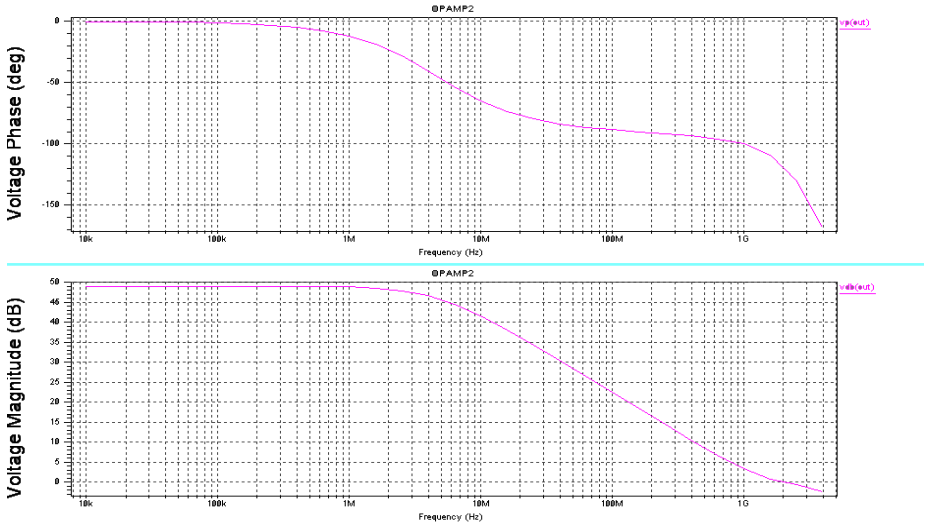

Figure 5: Frequency response of the OPAMP

The slew rate simulation is carried out performing a transient analysis using a pulse waveform of 1mV for a pulse period of 0.5nsec. The slew rate (+ve and –ve) are found to be 1.41V/µs and 1.42V/µs respectively, which is quite good as compared to other low power, low voltage OPAMPs. The slew rate response is as shown below---

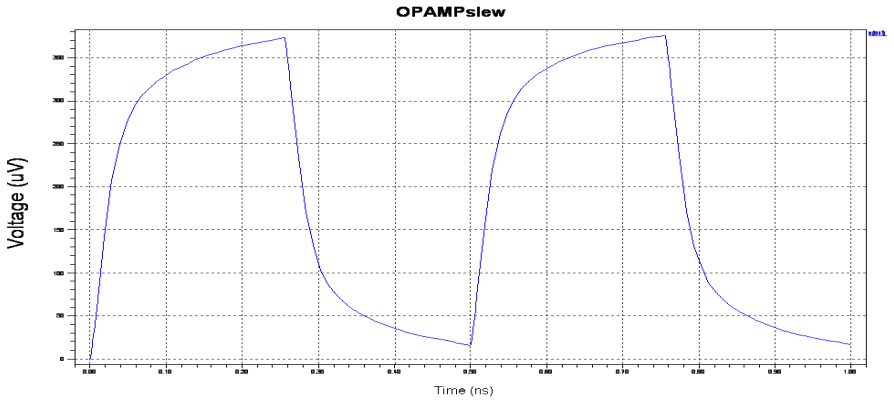

Figure 6: Slew rate (+ve and –ve) of OPAMP

The graph of output noise of the OPAMP is given below, yielding an output noise of 1.64µV/sqrt(Hz).

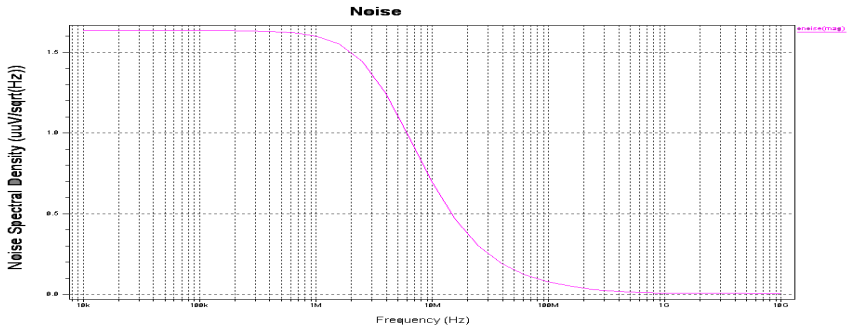

Figure 7: Output noise characteristics

The graph evaluating power supply rejection ratio (PSRR) in dB is shown in the following figure 8. PSRR measures the influence of power supply ripple on the OPAMP output voltage. It is the ratio of voltage gain from the input to output (open loop) to that from the supply to the output. PSRR can be calculated by putting the OPAMP in the unity gain configuration with the input shorted. The Miller compensation capacitance allows the power supply ripple at the output to be large enough. The PSRR (+ve) of the OPAMP in this design is calculated to be 154dB .

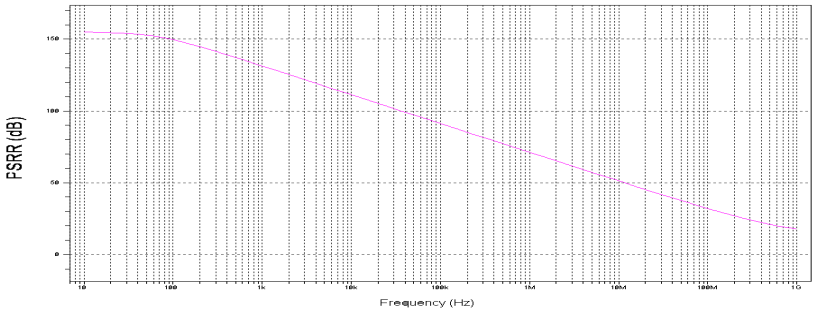

Figure 8: PSRR of the OPAMP

The design parameters		The electrical parameters yielded	
M1	15/0.2 µm/ µm	g_{mI}, g_{mII}	806µ, 537µ
M2	15/0.2 µm/ µm	Phase margin, Ø	60.5^0
M3	3.2/0.4µm/ µm	C_{01}	24.8fF
M4	3.2/0.4µm/ µm	Unity gain frequency, f_T	2.02GHz
M5	6.2/0.2µm/ µm	DC Gain	49.02dB
M6	1.2/0.2µm/ µm	PSRR(+ve)	154dB
M7	0.8/0.2µm/ µm	Settling time	0.5nsec
M8	0.4/0.2µm/ µm	Slew rate (+ve,-ve)	1.41V/µs; 1.42V/µs
Mb	3.2/0.2µm/ µm	Common mode gain	0.54957dB
I_{ref}	50µA	CMRR	39dB
Vdd	3V	Noise	1.64µV/sqrt(Hz)
C_L	10fF	Power consumption	39.6µW

Table 1: The geometrical dimensions incorporated and the electrical parameters yielded

6. CONCLUSIONS

An optimized compensation strategy for two-stage CMOS OTA has been proposed for a high frequency OPAMP design. It is based on compensation of right half plane zero. A simple looking OPAMP design problem becomes a harder one when it comes to optimizing all the parameters at a time. A careful analysis of circuit and deep insight into the circuit topologies and device operations leads to good implementation and desired results. The gain bandwidth product which is a constant puts challenges to the designers in designing the circuits for high DC gain and high bandwidth applications. Here, the gain has been increased by employing thin and long transistors into the design at output stage and wide transistors in input stage. These two techniques are able to increase the gain up to a great extent by increasing the output resistance and input transconductance respectively. Here the improvement in unity gain bandwidth has been done by increasing the bias current which decreases the DC gain and increases power dissipation little bit, still provides a good alternative control for an operational amplifier to operate at a high frequency. Introduction of each stage in multi-stage OPAMPs exhibits an additional pole into the system which can create problems in stability. Thus a proper compensation technique has to be employed in the system internally or externally. For this reason, the current buffer compensation technique in conjunction with Miller compensation technique has been employed.

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