A NEW APPROACH TO DESIGN LOW POWER CMOS FLASH A/D CONVERTER

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ABSTRACT

In the present paper, a 4-bit flash analog to digital converter for low power SoC application is presented. CMOS inverter has been used as a comparator and by adjusting the ratio of channel width and length, the switching threshold of the CMOS inverter is varied to detect the input analog signal. The simulation results show that this proposed 4-bit flash ADC consumes about 12.4 mW at 200M sample/s with 3.3V supply voltage in TSMC 0.35 µm process. Compared with the traditional flash ADC, this proposed method can reduce about 78% in power consumption.

KEYWORDS

CMOS Inverter, XOR gate based encoder, Flash ADC.

1. INTRODUCTION

With the rapid growth of modern communications and signal processing systems, handheld wireless computers and consumer electronics are becoming increasingly popular. Mixed-signal integrated circuits have a tendency in the design of system-on-chip (SOC) in recent years. SOC designs have made possible substantial cost and form factor reductions, in part since they integrate crucial analog interface circuits, such as ADCs with digital computing and signal processing circuits on the same die. The interfaces only occupy a small fraction of the chip die and for SOC designs, the technology selection and system design choices are mainly driven by digital circuit requirements. To limit energy in a reasonable size battery, minimum power dissipation in the mixed-signal integrated circuits is necessary [1]-[5].The analog-to-digital converter (ADC) is the key components in modern electronics and becomes a part of the SOC products because it bridges the gap between the analog physical world and digital logic world. In the digital domain, low-power, low-voltage requirements are becoming important issues as the channel length of MOSFET shrinks below 0.35µm values [6]. Of all types of ADCs the flash ADC has not only high data conversion rate required for applications such as video and communication systems, but also it becomes the part of other types of ADCs viz. pipeline and multi bit sigma delta ADCs as well as no idle time for continuous data conversion [7]. However, the use of large no of analog comparators in flash ADC makes it a complex chip design and causes high power dissipation [8]-[10]. Furthermore both its area and power become a critical issue as the resolution is increased [11]-[13]. However along with speed both size and power are

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important design parameters for an ADC especially for SOC applications. In [1], bisection method is used to design low power CMOS flash ADC. In [2], multiple-section method is used to design low power CMOS flash ADC. In [7], Interpolation technique is proposed to reduce the no of preamplifiers, hence reducing the power dissipation in flash ADC. In [12], the focus is on low voltage and high speed design. In [13], an average termination circuit is proposed to reduce the no of over-range amplifiers, hence reducing the power consumption. In [15], the TIQ technique has been used to design a flash ADC. In [18], the entire ADC is implemented using current-mode logic (CML) blocks. In [19], a capacitive interpolation technique is employed for low power design which eliminates the need of resistor ladder. The present work is an attempt in this direction. In this paper, it is aimed to design a flash ADC with low power consumption by using CMOS inverter as a comparator rather than analog comparator. The results show that the circuit size and power dissipation can be efficiently reduced by this design.

2. MODIFIED FLASH ADC

A traditional n-bit flash ADC architecture uses 2^n resistors and 2^{n-1} comparators to convert an analog signal to digital. This architecture has drawbacks like large input signal driving, high reference accuracy, high driving reference voltage and circuit complexity [10], [14]. CMOS inverters have been reported to be used in ADC designs [14]-[15]. In this work, this novel idea of employing CMOS inverters instead of analog comparators is considered for a flash ADC. CMOS is a combination of an n-MOSFET (NMOS) and a p-MOSFET (PMOS). CMOS inverter switching threshold (V_{th}) is a point at which input is equal to output voltage ($V_{in}=V_{out}$) and in this region both PMOS and NMOS always operate in saturation region. If the input arrives at a particular threshold voltage, then the output state changes. V_{th} can be obtained as [14]-[15]

$$V_{th} = \frac{V_{DD} + V_{tp} + V_{tn}\left(K_n/K_p\right)^{\frac{1}{2}}}{1+\left(K_n/K_p\right)^{\frac{1}{2}}} \tag{1}$$

where,

$$k_n = k_n^{'}\frac{W_n}{L_n} \tag{2}$$

$$k_p = k_p^{'}\frac{W_p}{L_p} \tag{3}$$

where $k_n^{'}$ and $k_p^{'}$ are constant transconductance parameters. V_{tn} and V_{tp} are the threshold voltage values of NMOS and PMOS respectively. As the voltages are constant, V_{th} depends on k_n and k_p values which decide the transition point of CMOS inverter [16]. If the ratio of k_n and k_p is decreased, the transited threshold voltage becomes high, otherwise, the transited inverter threshold voltage becomes low. k_n and k_p can be controlled by adjusting the width (W) and length (L) of NMOS and PMOS respectively. Based on this concept, various width/length ratio of CMOS inverters are designed to change their threshold voltages. Each CMOS inverter thus has a specified threshold depending upon this ratio. The W/L ratios are defined as $Z_n=W_n/L_n$ and $Z_p=W_p/L_p$. By changing the ratio of Z_n and Z_p, we can obtain various transit threshold voltages of CMOS inverters to quantize the input level. All inputs of CMOS inverter are tied together to detect the analog input level. If the input arrives at a particular threshold voltage, then the output state changes. The basic architecture of the proposed flash ADC is shown in Figure 1. In a 4-bit ADC, 15 CMOS inverters are tied in parallel to detect the input signal level. The inverter output is array from MSB to LSB. For LSB bit, the Z_n/ Z_p value should become small to increase the threshold voltage and for MSB bit, the Z_n/ Z_p value should become large to decrease the threshold voltage [14].

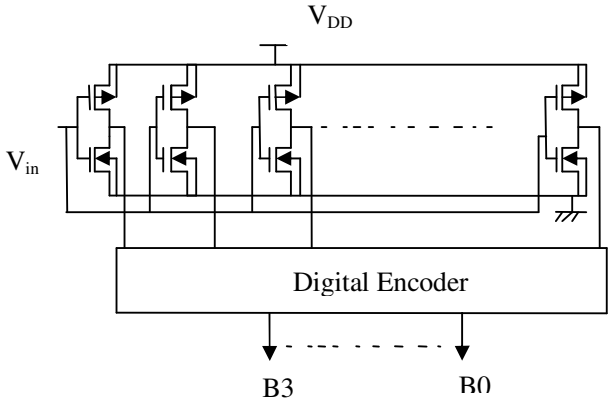

Figure 1. The architecture of proposed ADC

The function of the inverter is similar to the comparator used in a conventional flash ADC. The proposed technique does not require resistors and analog comparator. Hence, circuit complexity and size are greatly reduced because the input signal is detected by changing the width/length ratio of CMOS inverter. Since CMOS inverter only dissipates the power during the state transition, the power consumption becomes very low and the inverter does not require high driving current because the inverter has very high input impedance. From the above detailed information, one can achieve 15 bits to present the detected result for analog input signal. These 15 bits are encoded into 4-bit digital output code with the help of XOR gate encoder [14], [18]. If the inverter array outputs are A15 to A1, we encode it with B3 to B0 where A15 and B3 are MSBs respectively. It is found that B3 is equal to A8 and B2 can be obtained with XOR of A4, A8 and A12. Further, it is found that B2 is a sub term of B1, and B1 is also the sub term of B0. The logic function can be given by

$$B3 = A8 \tag{4}$$

$$B2 = A4 \oplus A8 \oplus A12 \tag{5}$$

$$B1 = B2 \oplus A2 \oplus A6 \oplus A10 \oplus A14 \tag{6}$$

$$B0 = B1 \oplus A1 \oplus A3 \oplus A5 \oplus A7 \oplus A9 \oplus A11 \oplus A13 \oplus A15 \tag{7}$$

First, we implement B2 with two XOR gates, then B1 is realized with the result of B2 & four XOR gates, and B1 is achieved with B1 and eight XOR gates. Thus the encoder is designed using 14 XOR gates.

3. SIMULATION RESULTS AND DISCUSSION

Firstly, a 4-bit flash ADC based on the Figure 1 architecture is designed in TSMC 0.35µm technology [13], [16]. The 4-bit ADC is realized using all digital circuitry and uses 15 CMOS inverters. Table 1 gives the features of the designed 4-bit flash ADC. The input ramp signal whose detectable voltage range is from 0.5V to 1.9 V in this design and supply voltage is 3.3V.

Table 1. Features of 4-bit ADC

Supply Voltage	3.3 V
Process	0.35 µm
Resolution	4-bit
Input Range	0.5V~1.9V
Max Speed	200MS/s
Transistor Count	72
Accuracy (DNL)	0.2LSB/-0.9LSB
Power Dissipation	12.4mW

The 15 transition points of each inverter and its Z_n/Z_p ratio are listed in Table 2.

Table 2. The transition point of 15 inverters in a flash ADC

Inverter	Z_n/Z_p	V_{th} (V)
Inv1	330.00	0.50
Inv2	41.79	0.60
Inv3	13.20	0.70
Inv4	7.39	0.80
Inv5	4.00	0.90
Inv6	2.48	1.00
Inv7	1.55	1.10
Inv8	1.08	1.20
Inv9	0.75	1.30
Inv10	0.534	1.40
Inv11	0.374	1.50
Inv12	0.26	1.60
Inv13	0.178	1.70
Inv14	0.122	1.80
Inv15	0.078	1.90

The detected step for input signal is about 0.1V by the change of the ratio of Z_n/Z_p of each inverter in experiments using (1).The DC transfer curves of 15 CMOS inverter are shown in Figure 2.

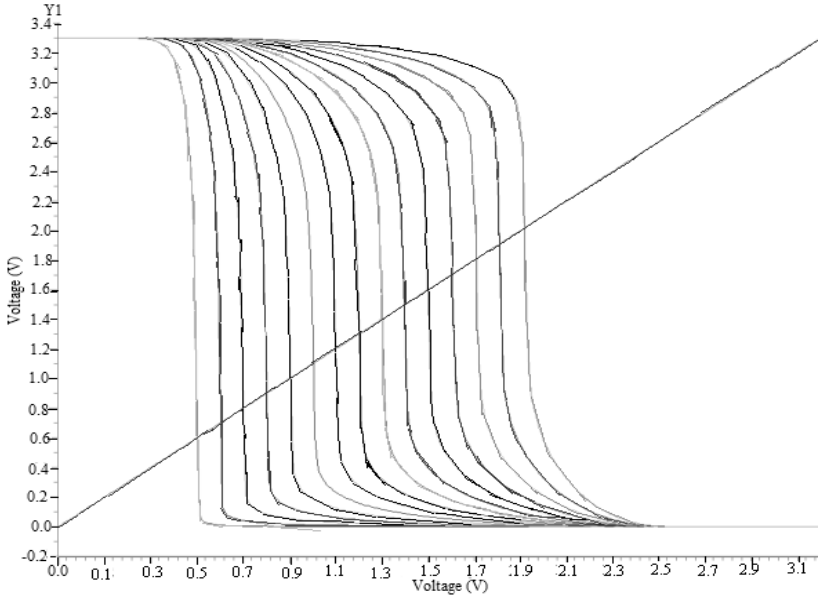

Figure 2. DC transfer curve of 15 CMOS inverters in the designed 4-bit ADC

The input a linear ramp is also shown. SPICE simulations are carried out. Due to sub-channel effect and process variation, the Z_n/Z_p ratio must be adjusted to obtain a fixed step size. The outputs obtained at the inverters are given to the digital encoder using (4)-(7). Then the expected output digital binary code is achieved corresponding to the specified input voltage. Table 3 shows the relationship of analog input voltage and the output digital binary code. The 4-bit ADC core is simulated and the results are shown in Figure 3. The input signal is ramp waveform and the output is digital binary code as required. The maximum frequency of 200 MHz is achieved in 4-bit flash ADC design. Differential non linearity (DNL) of an ADC is defined as a measure of separation between two adjacent codes measured at each vertical step in LSB. For a good design its value should be less than 1LSB [2], [19], [20]. Integral non linearity (INL) of the ADC is the maximum difference between the actual and ideal finite resolution characteristics measured vertically in LSB. For a good design its value should be less than 0.5LSB [20]. It is shown in Table 1 that the accuracy in terms of DNL is 0.2LSB/-0.9LSB and INL is 0.1LSB/-0.3LSB. Power dissipation of the ADC is 12.4 mW. Finally, the performance of the designed 4-bit ADC is compared for various parameters with results obtained in traditional flash ADC are presented in Table 4. Most of the flash ADCs use analog comparator to detect the input signal level. The power dissipation in proposed 4-bit flash ADC is 78% lesser than that of traditional flash ADC. Figure of Merit for the ADCs is taken as product of power and number of transistor count. Figure of merit of the proposed 4-bit ADC is 1.58 and is lowest compared to the traditional flash ADC as shown in Table 4. Therefore the proposed ADC is cost effective. As the CMOS inverter has high input impedance, hence our ADC design requires low input driving current and dissipates small power.

Table 3. Input range and outputs of 4-bit flash ADC core

Input Signal (V_{in})	Output Encoded Bits			
	B3	B2	B1	B0
0.40V≤Vi< 0.51 V	0	0	0	0
0.51V≤Vi< 0.61 V	0	0	0	1
0.61V≤Vi< 0.71 V	0	0	1	0
0.71V≤Vi< 0.80V	0	0	1	1
0.80V≤Vi< 0.91V	0	1	0	0
0.91V≤Vi< 1.01 V	0	1	0	1
1.01V≤Vi< 1.11V	0	1	1	0
1.11V≤ Vi< 1.21V	0	1	1	1
1.21V≤Vi< 1.31V	1	0	0	0
1.31V≤Vi< 1.41V	1	0	0	1
1.41V≤Vi< 1.50V	1	0	1	0
1.50V≤Vi< 1.62 V	1	0	1	1
1.62V<Vi< 1.72V	1	1	0	0
1.72V≤ Vi< 1.82V	1	1	0	1
1.82V≤ Vi< 1.92V	1	1	1	0
1.92V≤ Vi< 2.03V	1	1	1	1

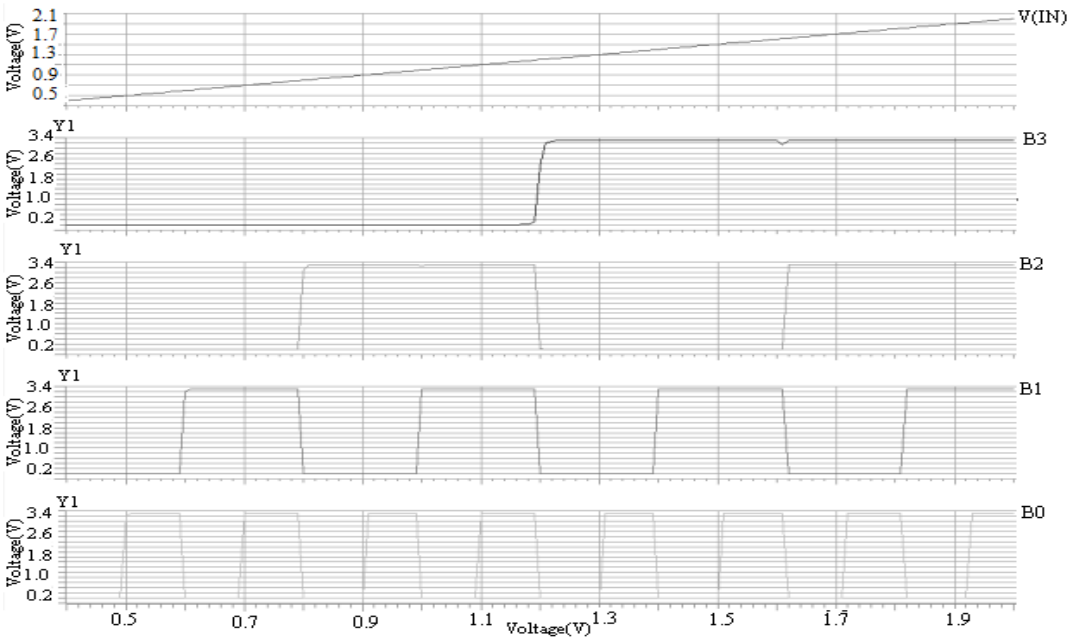

Figure 3. The simulation result of 4-bit ADC core

Table 4. Comparison of proposed flash ADC with traditional flash ADC

Features	Traditional	Proposed
Power Supply	3.3 V	3.3V
Process	0.35µm	0.35µm
Resolution	4-bit	4-bit
Sampling Freq	1 GS/s	200 MS/s
DNL	0.2LSB/-0.3LSB	0.2LSB/-0.9LSB
INL	0.2LSB/-0.3LSB	0.2LSB/-0.5LSB
Transistor count	445	128
Power Dissipation	56.5 mW	12.4 mW

4. CONCLUSIONS

Low power architecture for a 4-bit CMOS inverter based flash ADC is presented using TSMC 0.35µm technology. The proposed ADC design can achieve very low power dissipation and compared with the traditional flash ADC, this proposed method can reduce about 78% in power consumption as well as uses smaller silicon area. The DNL of the proposed ADC is within 0.2LSB/-0.9LSB and INL is within 0.2LSB/-0.5LSB. Figure of merit of the proposed 4-bit ADC is 1.58 and is lower compared to the traditional flash ADC, hence the proposed ADC is cost

effective. The proposed ADC chip so designed can be used for capacitive pressure sensor, video systems as well as it can be used in a low power two-step ADC, pipelined ADC and multi-bit sigma delta ADC.

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