

Performance analysis of DWT based OFDM over FFT based OFDM and implementing on FPGA

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ABSTRACT

Growth in technology has led to unprecedented demand for high speed architectures for complex signal processing applications. In 4G wireless communication systems, bandwidth is a precious commodity, and service providers are continuously met with the challenge of accommodating more users with in a limited allocated bandwidth. To increase data rate of wireless medium with higher performance, OFDM (orthogonal frequency division multiplexing) is used. Recently DWT (Discrete wavelet transforms) is adopted in place of FFT (Fast Fourier transform) for frequency translation. Modulation schemes such as 16-QAM, 32-QAM, 64-QAM and 128-QAM (Quadrature amplitude modulation) have been used in the developed OFDM system for both DWT and FFT based model. In this paper we propose a DWT-IDWT based OFDM transmitter and receiver that achieve better performance in terms SNR and BER for AWGN channel. It proves all the wavelet families better over the IFFT-FFT implementation. The OFDM model is developed using Simulink, various test cases have been considered to verify its performance. The DWT-OFDM using Lifting Scheme architecture is implemented on FPGA optimizing hardware, speed & cost. The wavelet filter used for this is Daubechies (9, 7) with N=2. The RTL code is written in Verilog-HDL and simulated in Modelsim. The design is then synthesized in Xilinx and implemented on Virtex5 FPGA board and the results were validated using ChipScope.

Keywords: FFT, DWT, OFDM, BER, Lifting scheme, Simulink

1. INTRODUCTION

A combination of modulation and multiplexing constitutes to Orthogonal Frequency Division Multiplexing Independent signals that are sub-set of a main signal are multiplexed in OFDM and also the signal itself is first split into independent channels, modulated by data and then re-multiplexed to create OFDM carrier. Orthogonality of subcarriers is the main concept in OFDM. The property of orthogonality allows simultaneous transmission of a lot of sub-carriers in a tight frequency space without interference from each other. This acts as an undue advantage in OFDM. Therefore, OFDM is becoming the chosen modulation technique for wireless communication.

With the help of OFDM, sufficient robustness can be achieved to provide large data rates to radio channel impairments. In an OFDM scheme, a large number of orthogonal, overlapping narrow band sub-channels or sub-carriers transmitted in parallel by dividing the available transmission bandwidth. Compact spectral utilization with utmost efficiency is achieved with the help of minimally separated sub-carriers. Main attraction of OFDM lies with how the system handles the multipath interference at the receiver end.

OFDM is multicarrier modulation (MCM) technique [1] which provides an efficient means to handle high speed data streams on a multipath fading environment that causes ISI. Normally OFDM is implemented using FFT and IFFT's. To decrease the BW waste [4] brought by adding cyclic prefix, wavelet based OFDM is employed. Due to use of wavelet transform the transmission power is reduced. The spectral containment of the channels is better since it does not use cyclic prefix. One type of wavelet transform is Discrete Wavelet transforms have been considered as alternative platforms for replacing IFFT and FFT. [1],[2],[3]. It employs Low Pass Filter (LPF) and High Pass Filter (HPF) operating as Quadrature Mirror Filters satisfying perfect reconstruction and orthonormal properties. The purpose of this paper is to perform the simulation study of FFT and DWT OFDM systems with respect to BER for AWGN channel for various modulation schemes. In DWT OFDM system, zero padding and vector transposing is done to transmit the modulated signal [1]. The DWT has been introduced as a highly efficient and flexible method for sub band decomposition of signals. The proposed architecture, based on new and fast lifting scheme approach for (9, 7) filter in DWT, reduces the hardware complexity and memory accesses. Moreover, it has the ability of performing progressive computations by minimizing the buffering between the decomposition levels. The architecture has regular structure, simple control flow, small embedded buffers and low power consumption. Lifting scheme requires fewer computations so the computational complexity is reduced.

The remainder of the paper is organized as follows. Section 2 explains FFT OFDM & DWT OFDM model, Section 3 on software reference model, section 4 discusses simulation results for various modulation and BER for FFT and DWT (Haar) OFDM systems, section 5 on Lifting based DWT architecture, section 6 on results & discussion, finally the paper is concluded in section 7.

2. OFDM SYSTEMS

2.1. FFT based OFDM System

An OFDM trans-receiver is shown in Figure (1).The inverse transform block can either be IDWT/IFFT and forward transform block can be DWT/FFT. The data generator used is a sine wave of bit stream d . It is processed using QPSK or M-ary QAM modulator to map the input data into symbols X_m . These symbols are now sent through IFFT block to perform IFFT operation to generate N parallel data streams. Its output in discrete time domain is given by,

$$X_{k(n)} = \frac{1}{\sqrt{N}} \sum_{i=0}^{N-1} X_m(i) \exp(j2\pi ni/N) \dots\dots\dots (1)$$

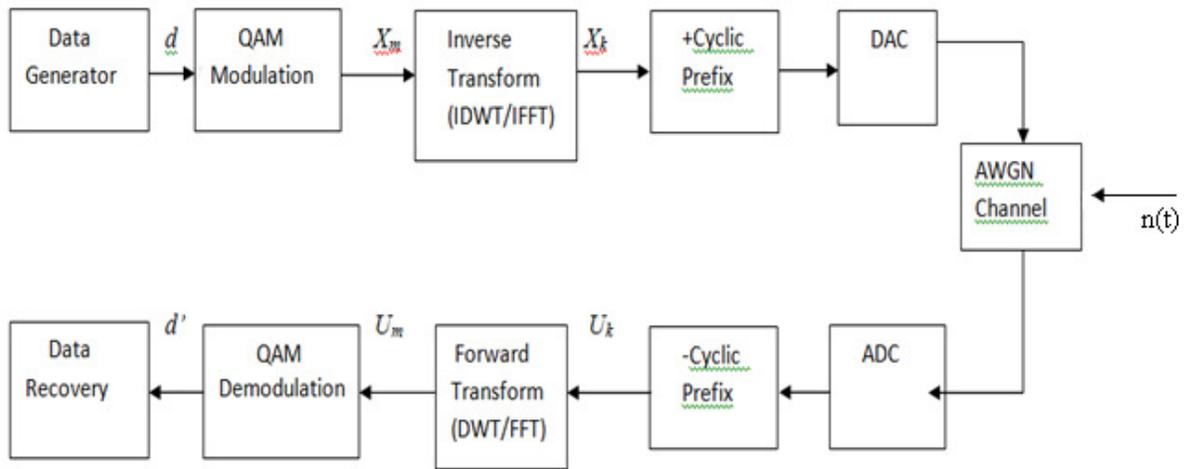


Figure. 1: An OFDM transceiver with inverse and forward transform blocks for implementation of FFT/ DWT-OFDM.

The transformed output (X_k) is now appended with cyclic prefix. The cyclic prefix (CP) is added before transmission, to mitigate ISI effect. It is usually 25% of the last part of the original OFDM symbol and this data is passed through AWGN channel with proper input power set. At the receiver, the reverse operation is done to obtain the original data back. The CP is removed and processed in the FFT block and finally passed through demodulator for data recovery. The output of the FFT in frequency domain is given by,

$$U_{m(i)} = \sum_{n=0}^{N-1} U_{k(n)} \exp(-j2\pi ni/N) \dots \dots \dots (2)$$

2.2 DWT based OFDM System

In the trans-receiver model shown in Figure.1, at the transmitter, the input sine wave maps on the data to modulator (16-QAM), thereby converting data d_k into symbols X_{mi} . Each X_{mi} is first converted to serial representation having a vector XX which will next be transposed into CA . Then, the signal is up-sampled (zero padding) and filtered by the LPF coefficients or approximated coefficients. Since our aim is to have low frequency signals, the modulated signals XX perform circular convolution with LPF filter whereas the HPF filter also perform the convolution with zeroes padding signals CD respectively. Note that the HPF filter contains detailed coefficients or wavelet coefficients. This data is given as an input to IDWT block wherein a particular wavelet (Haar) is chosen for simulation and is found to have a better performance when compared to FFT OFDM. At the receiver, DWT and demodulator (16-QAM) are used to recover back the data.

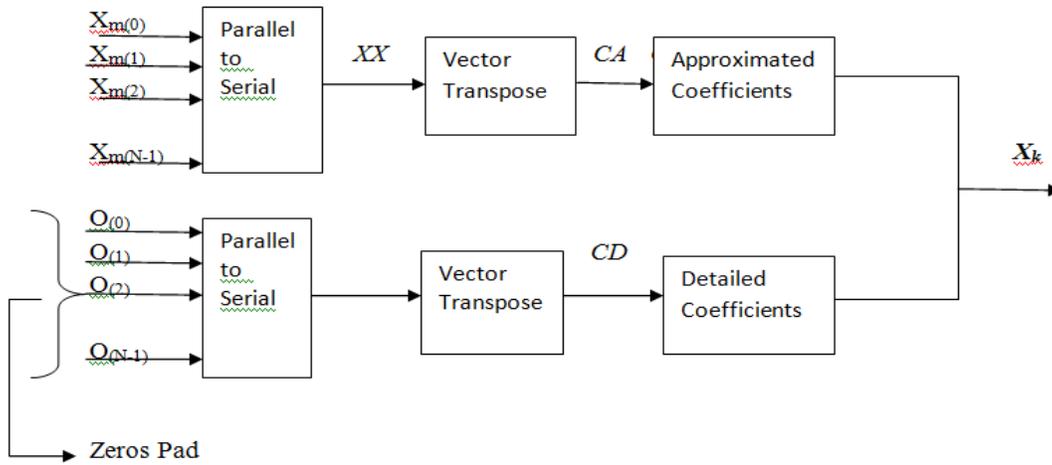


Fig. 2: DWT Transmitter

At the receiver, DWT and (16-QAM) demodulator are used to recover back the original data as shown in Figure.3

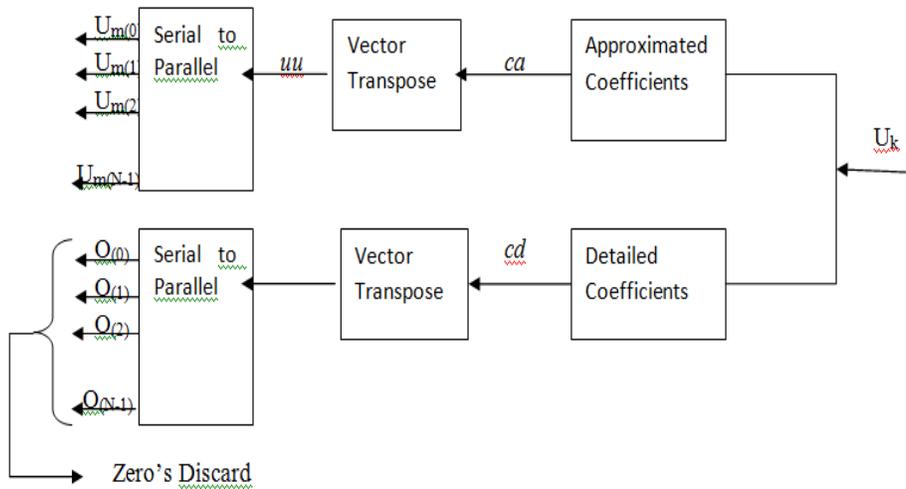


Figure. 3: DWT Receiver

3. SOFTWARE REFERENCE MODEL

The simulink model for DWT/FFT OFDM system for 64 sub-carriers is shown in figure 4.

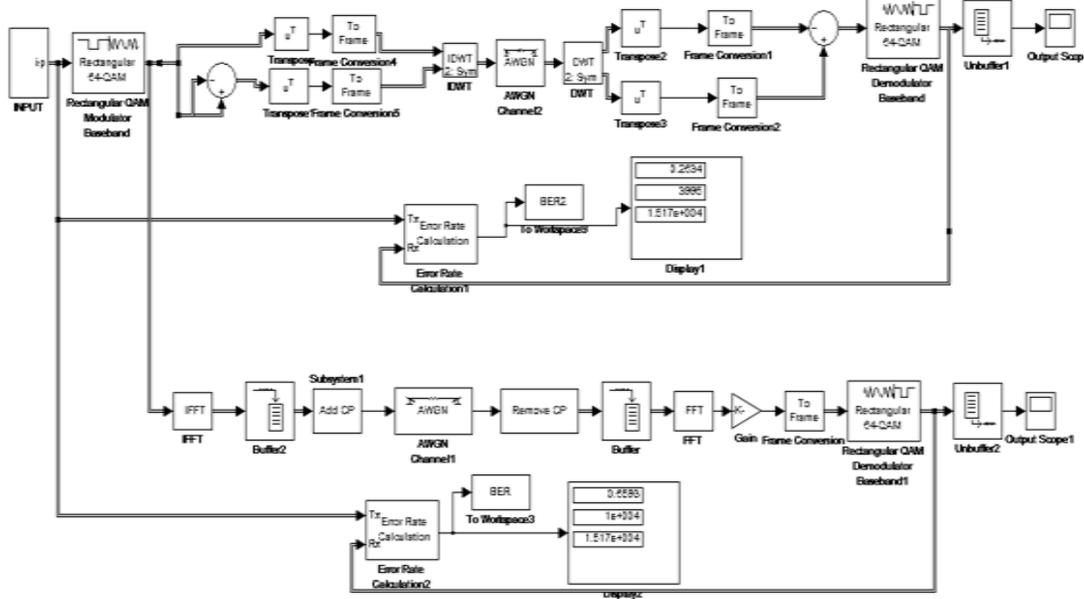


Figure. 4: Simulink diagram for DWT/FFT OFDM Systems

4. SIMULATION RESULTS

Simulation parameters:

No. of subcarriers (FFT and DWT): 64

Modulation: 16-QAM

Channel: AWGN

Table 1:BER for various modulation schemes for FFT and DWT OFDM systems of different wavelets at 20dB SNR

Modulation scheme	FFT	Haar	Db-3	Db-4
16-QAM	0.00005499	0.000012	0.9758	0.999
32-QAM	0.00682600	0.003742	0.9994	0.9842
64-QAM	0.08712000	0.060610	0.9992	0.969
128-QAM	0.2461000	0.201000	1.0000	1.000

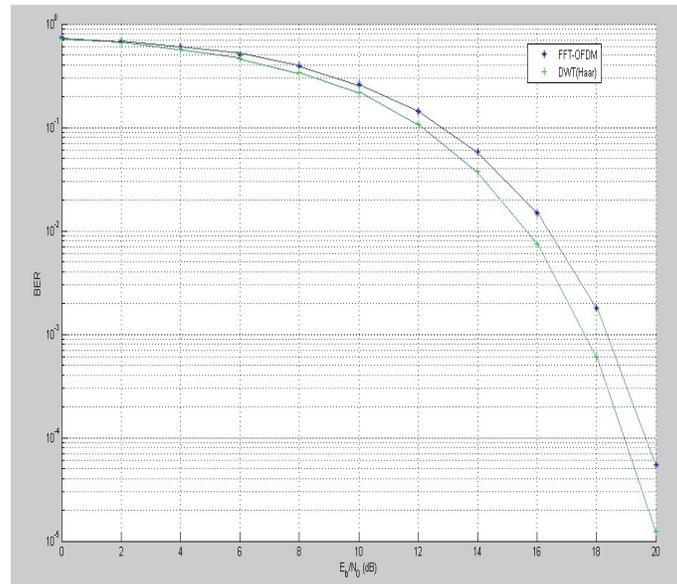


Figure. 5: BER plot for 16-QAM FFT/DWT OFDM systems.

From the BER plot above, it is seen that DWT (Haar) outperformed FFT-OFDM system by nearly 1.5db for 16-QAM modulation scheme for the same BER of 0.001.

5. Lifting based DWT Architecture:

Daubechies (9,7) wavelet filter[11],[13],[15] with $N=2$ is used for architecture development. Lifting scheme is used for the development of architecture. Here $N=2$ means, we will be having two stages of lifting scheme i.e predict1, update1 and in second stage predict2, update2. The main feature of the lifting-based wavelet transform is to break-up the high pass and the low pass wavelet filters into a sequence of smaller filters. The lifting scheme requires fewer computations so the computational complexity is reduced. The lifting-based wavelet transform basically consists of three steps, which are called split, lifting, and scaling, respectively, as shown in Figure 6.

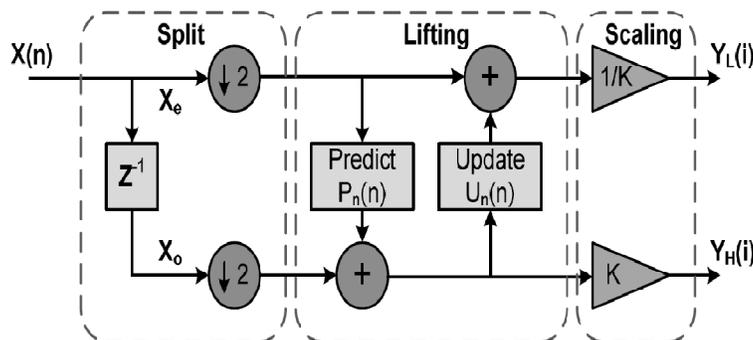


Figure 6: The lifting scheme implementation of 1D-DWT [12]

The basic idea of lifting scheme is first to compute a trivial wavelet (or lazy wavelet transform) by splitting the original 1-D signal into odd and even indexed sub sequences,

and then modifying these values using alternating prediction and updating steps. The lifting scheme algorithm can be described as follow:

i. Split step: The original signal, $X(n)$, is split into odd and even samples (lazy wavelet transforms).

ii. Lifting step: This step is executed as N sub-steps (depending on the type of the filter), where the odd and even samples are filtered by the prediction and update filters, $Pn(n)$ and $Un(n)$.

iii. Normalization or Scaling step: After N lifting steps, a scaling coefficients K and 1/K are applied respectively to the odd and even samples in order to obtain the low pass band (YL(i)), and the high-pass sub-band (YH(i)). Figure. 7 illustrates how the lifting scheme can be implemented using these steps. The diagram shows the lifting scheme for Daubechies (9, 7) biorthogonal filter.

The lifting scheme algorithm to the (9, 7) filter is applied as:

i. Split step

$$X_e \leftarrow X(2i) \quad \text{Even Samples} \quad \dots\dots\dots(3)$$

$$X_o \leftarrow X(2i+1) \quad \text{Odd Samples} \quad \dots\dots\dots(4)$$

ii. Lifting Steps

For (9, 7) filter, N=2

$$\text{Predict P1: } D(i) = X_o(i) + a [X_e(i) + X_e(i+1)] \quad \dots\dots\dots(5)$$

$$\text{Update U1: } S(i) = X_e(i) + b [D(i-1) + D(i)] \quad \dots\dots\dots(6)$$

$$\text{Predict P2: } Y_H(i) = D(i) + c [S(i) + S(i+1)] \quad \dots\dots\dots(7)$$

$$\text{Update U2: } Y_L(i) = S(i) + d [Y_H(i-1) + Y_H(i)] \quad \dots\dots\dots(8)$$

iii. Scaling Step

$$Y_H(i) = K Y_H(i) \quad \dots\dots\dots(9)$$

$$Y_L(i) = 1/K Y_L(i) \quad \dots\dots\dots(10)$$

Where $a=-1.586134342$, $b=-0.0529801185$, $c=0.882911076$, $d=-0.443506852$, and $K=1.149604398$. These fractional values are multiplied by a factor of 128 to convert them to decimal values.

These mathematical equations can be illustrated by the Figure 7. Another feature of lifting scheme is that it allows for an inplace computation.

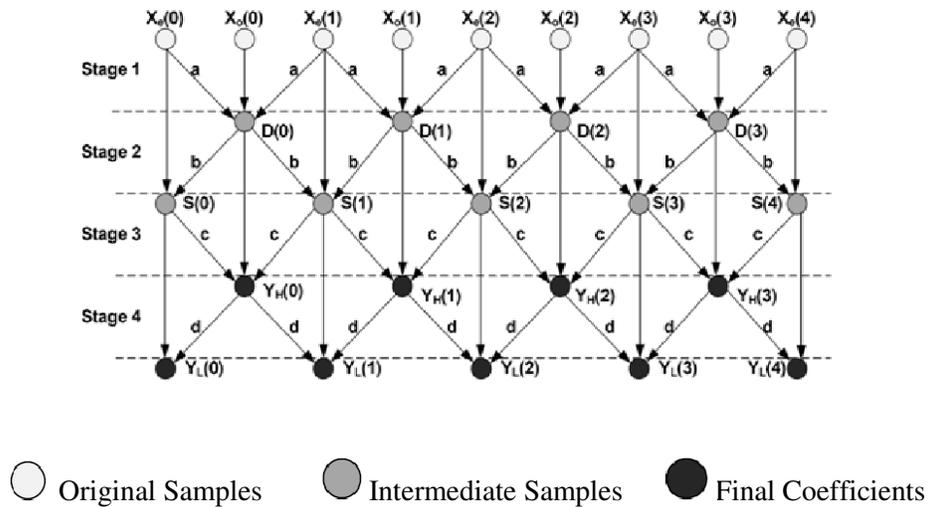


Figure 7: The diagram of 1-D DWT using Lifting Scheme (9,7) filter.[12]

Stage1: In this stage even and odd bits are considered accordingly and equation (5) is computed to get predict1 output $D[i]$.

Stage 2: The predict1 output ($D[i]$) along with even position of initial inputs is taken to compute equation (6) which results in update1 output $S[i]$.

Stage 3: Predict1 ($D[i]$) and Update1($S[i]$) outputs are taken to compute equation(7), which results in Predict2 output $Y_H[i]$.

Stage 4: Predict2 ($Y_H[i]$) and Update1 ($S[i]$) outputs are taken to compute equation (8), which results in Update2 output $Y_L[i]$.

Just reverse operation of this with corresponding sign change is carried out to compute IDWT.

6. RESULTS & DISCUSSION

6.1 RTL Schematic of the design

Figure 8 shows the RTL schematic of the proposed design with interconnects between the various blocks. It is a technology independent schematic.

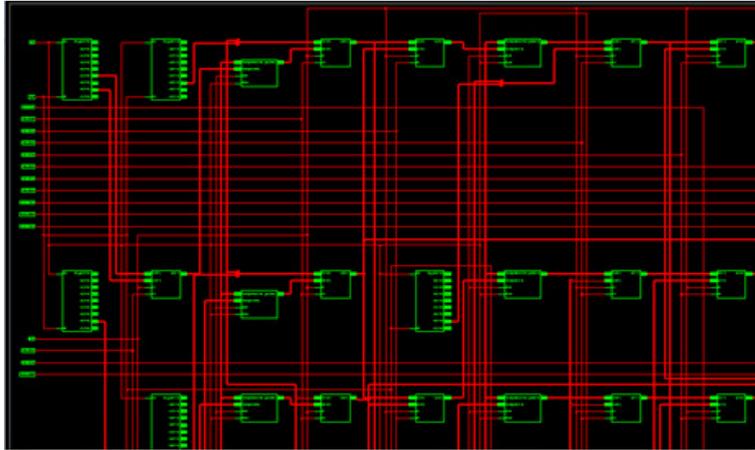


Figure 8: RTL Schematic of DWT-IDWT

The top level RTL schematic of the designed lifting scheme based DWT-IDWT architecture is obtained by the Schematic View tool in Xilinx ISE, which is shown in above figure 8. The netlist will be generated after synthesis process. This netlist will be saved in Verilog and DDC format (so that the constraints are embedded in the DDC file). The actual power and the timing were verified in Primetime. In this design clock period is set as 8ns (means frequency of operation is 125MHz) to meet slack constraint.

6.2 SIMULATION using MODELSIM

In this the lifting scheme based DWT architecture is proposed using $(9/7)$ Db filter and then the design is modeled using Verilog HDL in structural modeling. Simulation is done using modelsim and results are analyzed. Synthesis is the transformation of design from higher level of abstraction to lower level of abstraction. The DWT design using Lifting Scheme is carried out on Virtex5 FPGA development kit. It is seen that the pre-simulation and post place and route simulation results match, thereby proving that the design is perfectly mapped onto FPGA meeting the required design specifications.

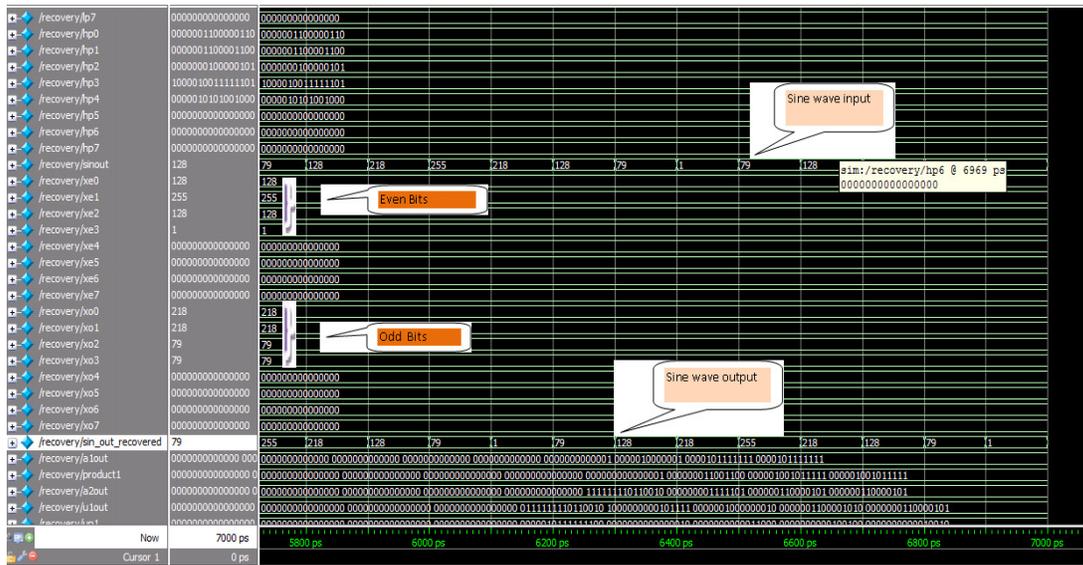


Figure 9: Simulation result using Modelsim

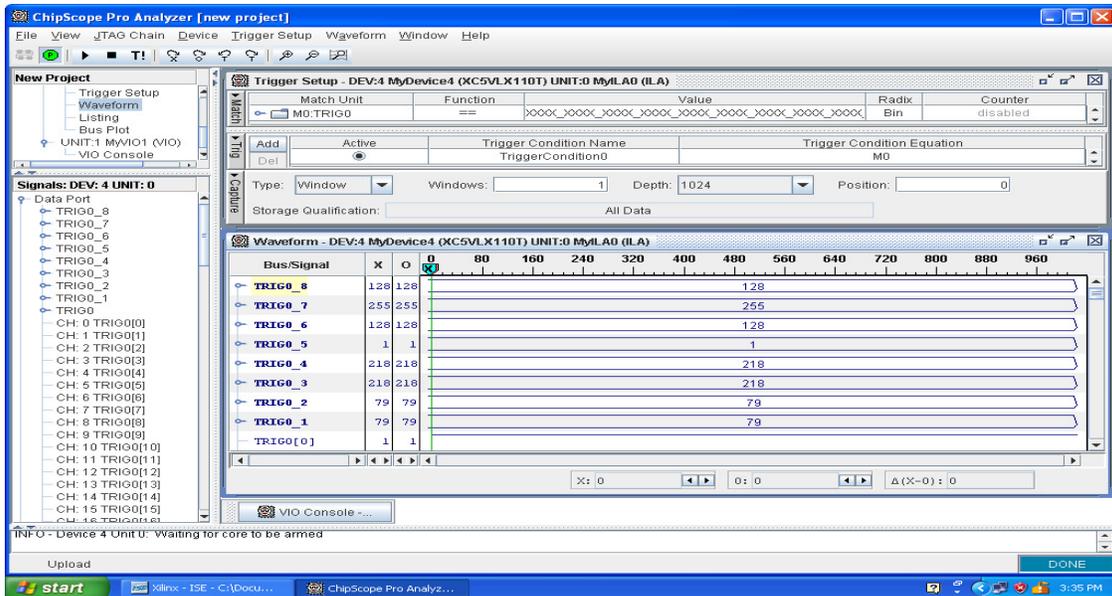


Figure 10: Outputs of Chip Scope Pro

From Figure 9 it is seen that the simulation results of the proposed architecture modeled in ModelSim matches with the results from Chip scope Pro as shown in Figure 10. Thus the design is efficiently mapped and optimized for area, power and speed. The synthesis results show that the design consumes total power of 1.2W, operates at a frequency of 131 MHz, consuming total of 35% of the resources.

7. CONCLUSION

In this paper, we presented the simulation result approaches for DWT-OFDM as an alternative form for FFT-OFDM system. It is seen that as Fourier based systems need addition of cyclic prefix whereas DWT based OFDM systems do not need cyclic prefix because of the overlapping nature of their properties, thus increasing the bandwidth efficiency by approximately 25%. Also it is seen that DWT (Haar) outperformed FFT-OFDM system by nearly 1.5db for 16-QAM modulation scheme for the same BER of 0.001. In this paper the lifting scheme based DWT architecture is proposed using (9/7) filter and then the design is modeled using Verilog HDL in structural modeling. Simulation is done using modelsim and results are analyzed. Then the design is implemented on FPGA and results are validated using ChipScope.

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