DESIGN AND IMPLEMENTATION OF FPGA BASED SIGNAL PROCESSING CARD

Priya Gupta[1] and Deepak Gupta[2]

[1]Banasthali University, Rajasthan India,
er.priya20@gmail.com
[2]Alpine System, New Delhi India
info@alpinesystems.net.in

ABSTRACT

This paper describes the design of FPGA based signal processing card. An on board real time digital signal processing system is designed using FPGA. The platform can decode process of various kinds of digital and analog signals simultaneously. The design trend in this card is towards small size, high integration and fast real time processing. For the optimum performance a 16 bit 1 MSPS ADC is used which is interfaced with FPGA to make all the data processing onboard in real time. This card can be used in many signal processing based applications like audio signal processing, audio compression, digital image processing, video compression, speech processing, speech recognition, digital communications by interfacing several separate board using inbuilt I/O's, each with a number of input channels that will communicate with each other in real time over a high speed communication link. The resulting images can be displayed directly on LCD or OLED panel displays using I/O's peripherals. The project introduces many challenging issues, which are being addressed in turn with different prototype designs. These issues are the ADC performance, interfacing the ADCs to the FPGA, implementing the flexible processing algorithms and high speed interconnection between the boards.

1. INTRODUCTION

Digital hardware is generally superior and more reliable than its analogue counterpart which can be prone to ageing and can give uncertain performance in production[21]. DSP on the other hand gives a guaranteed accuracy and essentially perfect reproducibility (Rabiner and Gold 1975). In addition, there is considerable interest in merging the multiple networks that transmit these signals,This provides a strong motivation to convert a wide range of information formats into their digital formats. Microprocessors, DSP micros and FPGAs perform a suitable platform for processing such digital signals, More recently,the field-programmable gate array (FPGA) has been proposed as a hardware technology for DSP systems in many new designs and applications for a variety of reasons but primarily because of their extreme-high performance and flexibility[23]. This is particularly true now that FPGAs have integrated gigabit serial communications, memory interfaces, immersed processors, and a wide range of available core firmware modules .This card is tested for laser beam communication which requires very fast data processing although it can also be used for a vast range of signal processing's simultaneously. For that purpose a high speed system is being developed that not only delivers high performance, but also a high degree of flexibility that is not commercially available. To limit

DOI : 10.5121/vlsic.2011.2311

energy in a reasonable size battery, minimum power dissipation in the mixed-signal integrated circuits is necessary [17].The analog-to-digital converter (ADC) is the key component because it bridges the gap between the analog physical world and digital logic world[1][2].

2. DEVELOPMENT STRATEGY

The main concept is that by using A/D converter we can maintain the good energy and time resolution. We are using AD7671 ADC with 16-bit resolution, 1 MSPS, charge redistribution SAR, analog-to-digital converter that operates from a single 5 V power supply[6]. It contains a high speed 16-bit sampling ADC, a resistor input scalar that allows various input ranges, an internal conversion clock, error correction circuits, and both serial and parallel system interface ports[2].For superior performance and highest flexibility, a PROM flash memory LHF00L28(16Mbit- 1MX16 with a read operation of 70ns) externally connected to the FPGA[22]. is used for storing the data, allowing the implementation of high performance signal processing tasks. Resulting images can be displayed directly on LCD or OLED panel displays using I/O's peripherals[3]. In this FPGA, volatile memory devices can also be programmed via the JTAG port normally during development work. In addition, newer parts, for instance Xilinx Virtex-4, have internal monitoring capability (temperature, voltage and current) accessible via the JTAG port.

2.1 Connecting the peripherals to a logic analyzer

The first step to evaluate an RS232, OLED, GPIOs, ADC and memories that could be suitable for our design, was to connect the evaluation board to a logic analyzer through custom designed adapter boards. Data from the logic analyzer was transferred to a computer using hypertext terminal for offline processing. After checking the functionality of all these peripherals which are required for developing the signal processing system, are being used.

2.2 Development and interfacing of FPGA with ADC, flash memory.

The second step was to develop a prototype board with a Virtex-4SX FPGA to interface with ADC[4]- [19], Memory[6], RS232, Power Supply, OLED and GPIOs. For interfacing these peripherals their Drivers has to be made, hence VHDL coding is used for making drivers. The bit file generated after coding is burned in PROM memory of FPGA. After the proper interfacing all the peripherals are tested and their responses are adjusted accordingly. Therefore the outcome is a adaptive hardware that continuously change in response to the input data, the design trends in this card are towards small size, high integration and fast real time processing.

3. SIGNAL PROCESSING SYSTEM

This FPGA based signal processing card is compatible for both types of signals, digital as well as analog. This card uses FFT, it gives capability to accelerate and verify their real time signal processing design. The new system signal processing kit radically reduces simulation time and simplifies the overall design process. The tool allows designer to easily incorporate their FPGA hardware directly into the impact tool using a JTAG interface. By using push button a designer can automatically generate a FPGA bit stream from the tool and incorporate the FPGA back into the system level simulation .this card also gives a tremendous choice of FPGA based boards to target a unique capability. The AD7671 has a maximum integral nonlinearity of 2.5 LSB with no

missing 16-bit code.ADC output samples stored in 16 bit flash memory i.e. LHF00L28 IC .Flash memory used to store multiple samples which are coming from LASER beam through ADC. After the comparison of different samples the effective data pass through the DDS interface.

4. PROTOTYPE BOARD

This card is on board user programmble xilinx virtex-4SX FPGA for signal processing funtion such as channelization ,modulation , and error correction, with the data rates of 600 Mb/s HSTL & SSTL (on all single-ended I/O) and 1 Gb/s LVDS (on all differential I/O pairs).The card has a large number of high speed input output GPIOs ,DDS interface and OLED interface that are connected to FPGA through buffer.Data from ADC is received by dedicated DDS register, which enables high performance data receptions . FPGAs have integrated gigabit serial communications, memory interfaces, immersed processors, and a wide range of available core firmware modules. Three software's are used to design this card i.e. ORCAD for designing the schematic part, MENTOR GRAPHICS for the layout and Xilinx is used for VHDL coding.

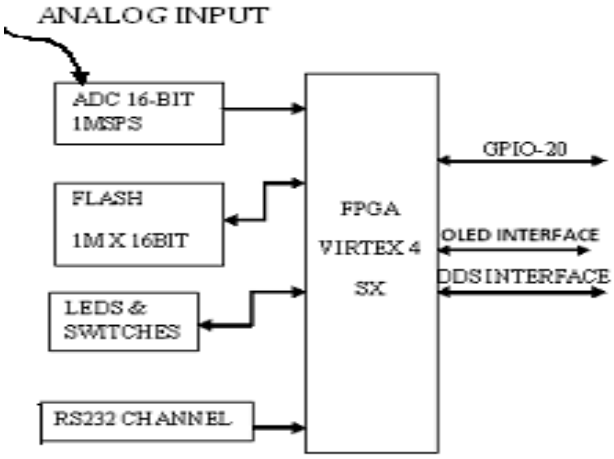

Figure1: Block diagram of signal processing card

Block diagram of signal processing card which is shown in Figure.1, the FPGA interfaced with I/O and other peripheral device.

As far as our card specification is concerned :

Area of the PCB - 70mX130m

Execution time- 200ms

Power consumption- 40mw

Input signal- various analog signals ranging from 10mv to 30mv as well as digital signals. Tested for LASER beams incident on a photo diode.

5. RESULT AND DISCUSSION

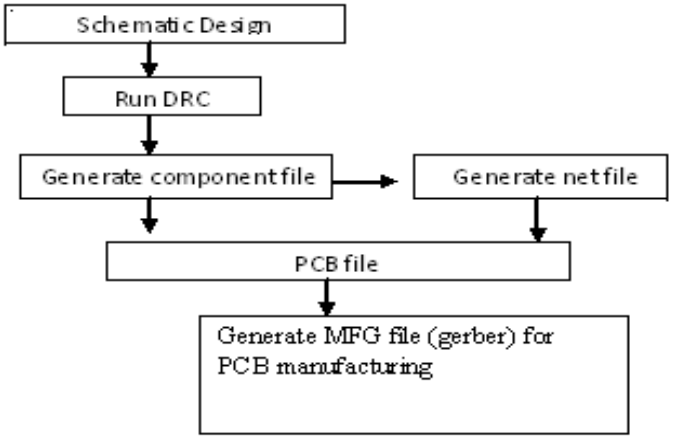

Figure 2: PCB Design steps

5.1 FPGA based signal processing board outline drawing

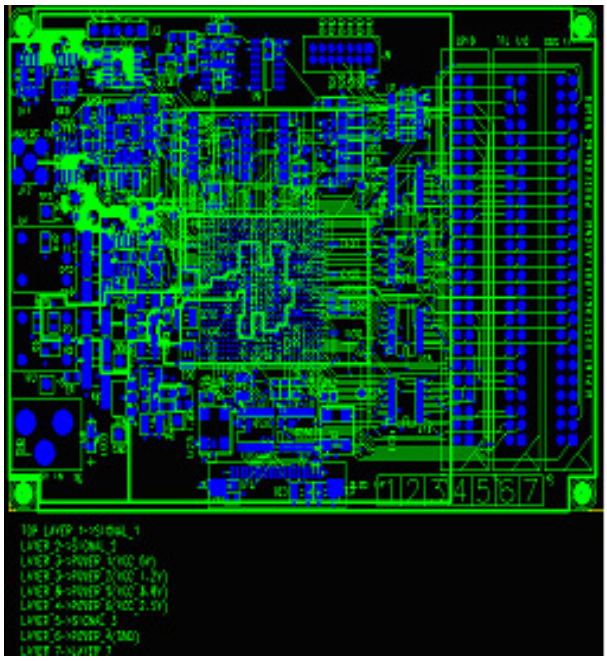

Figure 3: PCB Outline

There are total eight layers in the PCB whose layer wise description is given below:Layer1 (copper top) : signal 1, Layer2 (copper inside) : signal 2, Layer3 (copper inside) :Power1 (Vcc +5V), Layer4(copper inside): Power2 (Vcc +1.2V), Layer5 (copper inside): Power3 (Vcc +3.5V), Layer6 (copper inside) :Power4 (Vcc +2.5V), Layer7 (copper inside) : signal3, Layer8 (copper bottom) : Power (Gnd). There are some of the design protocols which are to be followed while placement and routing[12]. PROM Memory and Flash memory should be placed first and near to

the FPGA and routed straight through the shortest path available. This reduces delay as well as noise in the channel. The crystal oscillator must be routed straight and close to the FPGA with a ground pad. Analog and Digital signal tracks should be away from Each other with a Ground track between them. This practice prevents the digital signal to be effected by the noise of analog signal. There must be separate Gnd signals for analog and digital signals and both the Gnd signals should be connected to each other with an inductor at the end.

6. WORKING

The following flow chart shows the working of signal processing card (Figure.4), first the FPGA is initialized for all I/O peripherals. Then analog data is applied to the ADC in the form of LASER beam, where it gets converted to digital form and stored in FLASH memory. This digital signal is then retrieved and processed by FPGA and synthesized by DDS interface, the o/p of this stage is noise free analog signal. This analog signal is then compared with the previous analog signal and is checked for noise removal. If the noise has been removed the signal is transferred to the display. If there is no change in the compared signal then it is again send for processing and synthesizing.

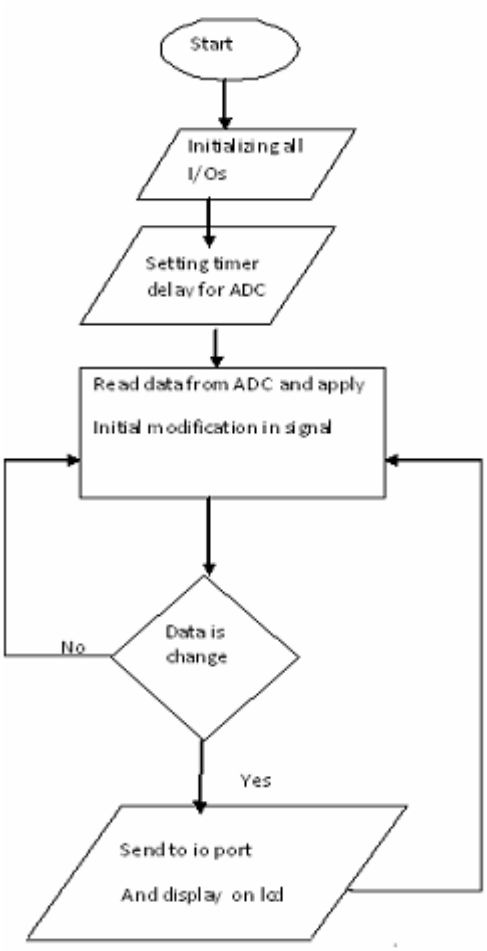

Figure 4 : Working of signal processing card

7.CONCLUSION

Microprocessors, DSP micros and FPGAs perform a suitable platform for processing of digital signals, and this paper represents a number of basic issues with implementing DSP algorithms on, in this case, FPGA platforms. These issues range from understanding both the sampling rates and computational rates of different applications with the aim of understanding how these requirements affect the final FPGA implementation. This paper leads to conclude the advantages of FPGA over general purpose microcontrollers like very high data rate, flexibility, data security, parallel processing which are necessary for real time application such as in this paper FPGA and some of high speed peripherals are used in LASER detection system for missile application and LASER based audio application, light sensors are used to detect the laser beam and the data is then processed and converted into suitable format to be used in various applications. Like light signals other signals can also be used simultaneously depending upon the need, this shows the processing of signal at a high speed . FPGA based platform is addressing the problems by allowing add-on cards to meet application-specific feature and performance requirements

8. REFERENCES

[1] Attila Hidvegi et.al."A High Speed Data Acquisition System for Segmented GE-Detectors", IEEE, 2006

[2] A.Hidvegi et al., A High-Speed Data Acquisition System for Segmented Ge-Detectors, IEEE Nuclear Science Symposium Conference Proceedings, (2006) ISSN: 1082-3654

[3] Hitachi HD44780U (LCD-II) Dot Matrix Liquid Crystal Display Controller/Driver Datasheet, Revision 0.0. Hitachi Ltd.

[4] http://www.latticesemi.com/documents/doc26686x11.pdf

[5] http://www.eetimes.com/design/programmable-logic/ 4014823/

[6] http://www.xilinx.com/publications/archives/solution guides/ memory interfaces. pdf

[7] http://e2e.ti.com/support/data converters/ high speed data converters /f /68/ t /102548.aspx

[8] http://wenku.baidu.com/view/2b6ffffc910ef12d2af9e7f5. html

[9] http://www.mentor.com/products/pcb-system-design/blog/ post/pcb-design-perfection-starts-in-the-cad-library-part-19-e2558ae4-04e4-42c6-94f5-31207e92ffd1

[10] http://www.mentor.com/products/pcb-system-design/blog/tag/hyperlynx-c3befda1-74cf-49b4-8d49-22bb460766e4

[11] http://www.docstoc.com/docs/26451369/Mentor-Graphics-PCB-Layout-Tips

[12] Kung SY VLSI Array Processors. Prentice Hall

[13] DeHon A Dynamically programmable gate arrays: A step toward increased computational density.

[14] www.focus.ti.com

[15] www.researchandmarkets.com

[16] www.alldatasheets.com

[17] F. Hatori, T. Sakurai, K. Nogami, K. Sawada, M. Takahashi, M. Ichida, M. Uchida, I. Yochii, Y.Kawahara, T. Hibi, Y. Saeki, H. Muroga, A. Tanaka, and K. Kanzanki. Introducing redundancy in field programmablegate arrays. In Custom integrated Circuis Conference, 1993

[18] C. Chun Tsai, Kai-Wei Hong, Yuh-Shyan Hwang, Wen-Ta Lee and Trong-Yen Lee, "New Power saving design method for CMOS flash ADC," The 2004 47th Midwest Symposium on Circuits and Systems, vol. 3. pp. 371-374, July 2004.

[19] A. Stojcevski, H. P. Le, J. Singh and A. Zayegh, " Flash ADC architecture", IEE Electronics Letters, vol.39, no.6, pp. 501-502, March 2003.

[20] Li Z and Hauck S (2001) Configuration compression for virtex fpgas Proc. IEEE Conf. on FPGA-based Custom Computing Machines.Roger woods, John McAllister, Gaye Lightbody, Ying yi."FPGA- based implementation of signal processing systems".

[21] Roger woods, John McAllister, Gaye Lightbody, Ying yi."FPGA- based implementation of signal processing systems".

[22] Davis J, Venkatesan R, Kaloyeros A, Beylansky M, Souri S, Banerjee K, Saraswat K, Rahman A, Reif R and Meindl J (2001) Interconnect limits on gigascale integration (gsi) in the 21st century. Proc. IEEE 89.

[23] DeHon A (1996) Dynamically programmable gate arrays: A step toward increased computational density Proc. 4th Canadian Workshop on Field-Programmable Devices.

Authors:

PRIYA GUPTA received Bachelor of Engineering from Bundelkhand University (U.P) in 2009 and Master of Engineering degree from Banasthali University (Rajasthan) in2011.Presently working as a asst. prof in Manav Rachna Inaternational University (Faridabad).