LINEARITY AND ANALOG PERFORMANCE ANALYSIS OF DOUBLE GATE TUNNEL FET: EFFECT OF TEMPERATURE AND GATE STACK

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ABSTRACT

The linearity and analog performance of a Silicon Double Gate Tunnel Field Effect Transistor (DG-TFET) is investigated and the impact of elevated temperature on the device performance degradation has been studied. The impact on the device performance due to the rise in temperature and a gate stack (GS) architecture has also been investigated for the case of Silicon DG-MOSFET and a comparison with DG-TFET is made. The parameters governing the analog performance and linearity have been studied, and high frequency simulations are carried out to determine the cut-off frequency of the device and its temperature dependence.

KEYWORDS

Analog, DG-TFET, Gate Stack, Linearity

1. INTRODUCTION

With the advancements in the wireless and mobile communication demand of high levels of integration and cost effective technologies are needed. The continuous scaling of CMOS technology has resulted in high speed MOS devices suitable for analog RF applications [1]. The modern day communication requires low distortion and linear systems as a building block for their design. But today the challenges CMOS technology is facing in terms of severe Short channel effects (SCEs), punch through arising from the extremely scaled dimensions has resulted in the need to explore new device architectures and design [2]. There are several experimental and simulation based studies showing TFETs as a potential candidate for the deep sub micron regime. The immunity against the SCEs, low leakage current and CMOS compatible technology makes it an attractive alternative for conventional MOSFETs. The earlier studies on TFETs are focused on achieving high I_{on}/I_{off} [3], sub 60mV/dec subthreshold slope [4], low power supply

operation [5], device performance mainly targeted for the digital applications. The analog and linearity performance is still an unexplored area and needs to be investigated too. So the focus of this study is on studying the linearity and analog performance of TFETs to determine their suitability for analog/ RF applications. Tunnel FETs has been demonstrated experimentally as a device with immunity against temperature variations over a wide range [6-9]. The earlier studies have reported weak temperature dependent TFET characteristics and the temperature independent behavior of Subthreshold swing. To address the issue of low ON currents in TFETs several device designs and optimizations are reported, use of a high-k dielectric being one of the possible solutions [10-11]. In the present work, the effect of two parameters namely the impact of temperature variations and the impact of a Gate Stack architecture has been studied on the linearity, distortion and analog performance metrics like VIP2, VIP3, IMD3, device efficiency g_m/I_{ds}, drain output resistance R_{out}, early voltage (V_{ea}) intrinsic device gain g_m/g_d. The effect of temperature has also been studied for DG-MOSFET through the above mentioned parameters in order to make a comparison with DG-TFET in terms of its capability to sustain the temperature variations.

The paper has been divided into two sections. In first part, the impact of temperature has been analyzed and in the second part the effect of Gate Stack architecture is considered and finally the results are concluded

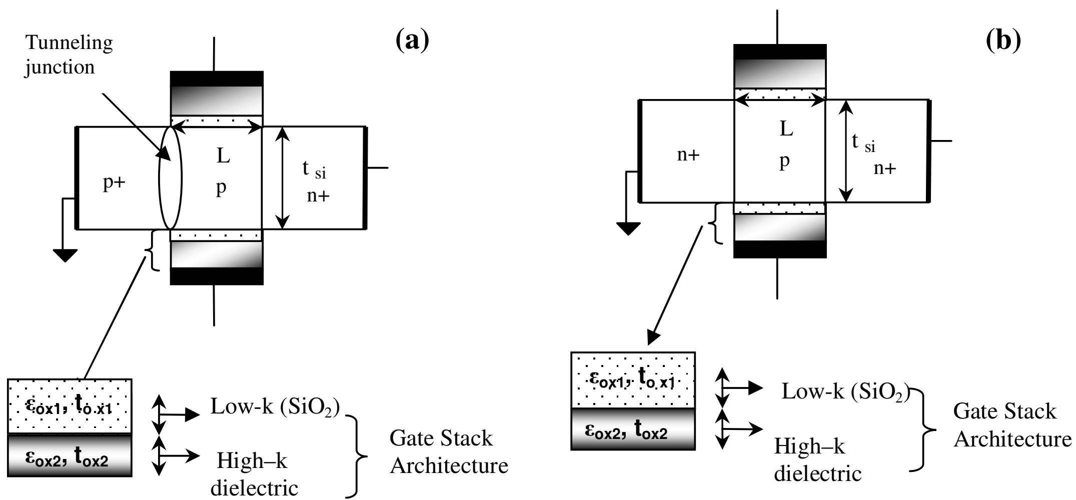

Figure 1. Schematic of the simulated devices (a) DG-TFET and (b) DG-MOSFET

2. DEVICE DESIGN AND SIMULATION TOOLS

The schematic for the simulated devices DG-TFET and DG-MOSFET are shown in fig. 1. All the simulations have been carried out using the numerical device simulation software ATLAS 3D [12]. Kane's Band to Band tunneling model is employed for DG-TFET. Physical models activated for simulation comprises of concentration and field dependent and surface mobility models, Shockley Read Hall recombination models, and Fermi Dirac statistics. Source and drain junctions are considered to be abrupt. Quantum corrections are neglected. A uniform and asymmetric source and drain doping are chosen for DG-TFET (p+ source $N_A=10^{20}cm^{-3}$, n+ drain $N_D=5x10^{18}cm^{-3}$ and a lightly doped p type channel $N_i=10^{15}cm^{-3}$) in order to suppress the ambipolar behavior. Silicon channel thickness (t_{si}) is considered as 10nm with a gate oxide thickness t_{ox} of 3nm SiO_2 and channel length L=70nm. The gate stack architecture consists of a

2nm high-k (t_{ox2}) and 1nm of SiO_2 (t_{ox1}). For DG-MOSFET a symmetric doping profile is chosen with source and drain doping (n+) of $N_D=10^{20}cm^{-3}$ and channel doping similar to DG-TFET. Both the devices (DG-MOSFET and DG-TFET) are optimized for same threshold voltage i.e V_{th}=0.33V @ V_{ds}=1V (evaluated using the constant current method V_{th} @ V_{ds}=1V @ $I_{ds}=10^{-7}$A/um). For Gate Stack architecture, 1nm of SiO_2 ($\boldsymbol{\varepsilon_{ox1}}$ =3.9) and a 2nm of high-k gate with dielectric constant $\boldsymbol{\varepsilon_{ox2}}$ =10 is considered. The simulations has been carried out with default simulator parameters, the magnitude of the results obtained may have 5-10% variations with respect to experimental results, but the basic trends and findings would remain same.

3. LINEARITY AND ANALOG PERFORMANCE METRICS

The important device parameters for linearity and analog applications are transconductance (g_m) and drain output conductance (g_d). Transconductance (g_m) determine the various Figure of Merits (FoM) namely VIP_2, VIP_3, IMD_3 used to assess linearity and distortion as well as gain and cut-off frequencies. For analog design the crucial parameters are device efficiency g_m/I_{ds}, intrinsic dc gain g_m/g_d and drain output resistance R_{out} [13-15].

$$VIP_2 = 4 * g_{m1} / g_{m2} \Big|_{constant \; V_{ds}} \quad (1)$$

$$VIP_3 = \sqrt{24 * g_{m1} / g_{m3}} \Big|_{constant \; V_{ds}} \quad (2)$$

$$IMD_3 = R_L * \left(4.5 * (VIP_3)^3 * g_{m3}\right)^2 \quad (3)$$

$$g_{m1} = \partial I_{ds} / \partial V_{gs}, \; g_{m2} = \partial^2 I_{ds} / \partial V_{gs}^2, \; g_{m3} = \partial^3 I_{ds} / \partial V_{gs}^3 \quad (4)$$

4. IMPACT OF TEMPERATURE

The transfer characteristics of DG-MOSFET and DG-TFET and the impact of temperature on drain current is shown in fig. 2. It is observed that the effect of temperature in case of DG-TFET is weak and it results in the increase of drain current both in ON and OFF state, although very small. This increase in value of drain current can be understood by the Kane's band to band tunnelling equation given by

$$I_{ds} \propto G_{btbt} = A \frac{|E|^2}{E_g^{1/2}} \exp\left(\frac{-B E_g^{3/2}}{|E|}\right) \quad (5)$$

where E is the electric field which is V_{gs} dependent, E_g is the band gap, A and B are the material dependent parameters having default values defined in the simulator.

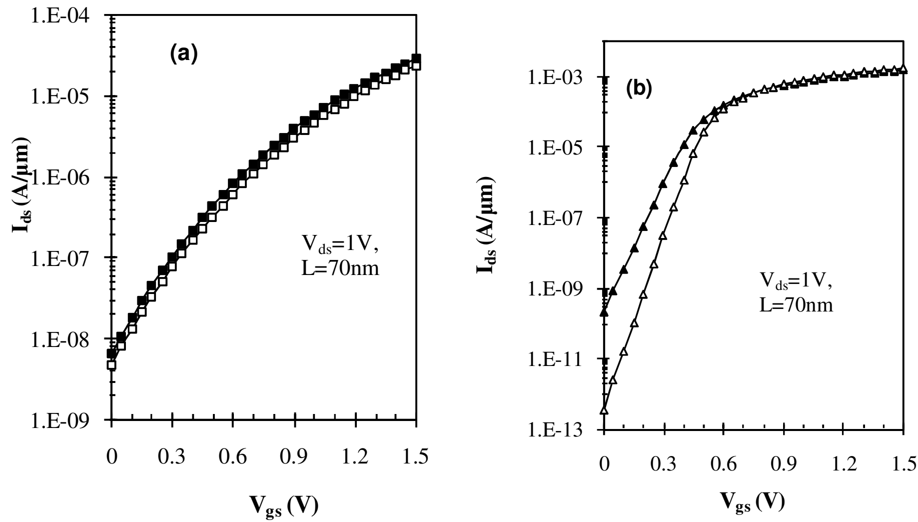

Figure 2 Transfer characteristics (I_{ds}-V_{gs}) of (a) DG-TFET and (b) DG-MOSFET at two different temperatures. Symbols: (□□□) for DGTFET, (ΔΔΔ) for DG-MOSFET where Open symbols for 300K, Solid symbols for 400K.

Since the current depends on the band gap which is a function of temperature [16] as modeled in ATLAS and given by eq. 6, where the default values of alpha and beta are material dependent. With rise in temperature the band gap value reduces which leads to the increase in the band to band tunneling current of the DG-TFET.

The reduction in the threshold voltage (V_{th}) is also minimum in case of DG-TFETs. The threshold voltage reduces to 0.296 @V_{ds}=1V and T= 400K from its value 0.33V @ V_{ds}=1V and T=300K. While in case of DG-MOSFET, due to increase in temperature the carriers generated in the channel increases thus leading to significant reduction of threshold voltage (V_{th} @ V_{ds}=1V and T= 400K is 0.22V and V_{th} @ V_{ds}=1V and T=300K is 0.33V) but the current degrades due to channel mobility degradation at high temperature arising due to the increased phonon scattering.
Fig 3 (a) & (b) shows the impact of temperature on the transconductance characteristics of DG-TFET and DG-MOSFET. As clearly observed there is a very insignificant change in the magnitude for the case of DG-TFET in contrast with that of DG-MOSFET in which the transconductance has significantly enhanced only in the subthreshold region due to degraded subthreshold characteristics of DG-MOSFET at elevated temperatures.

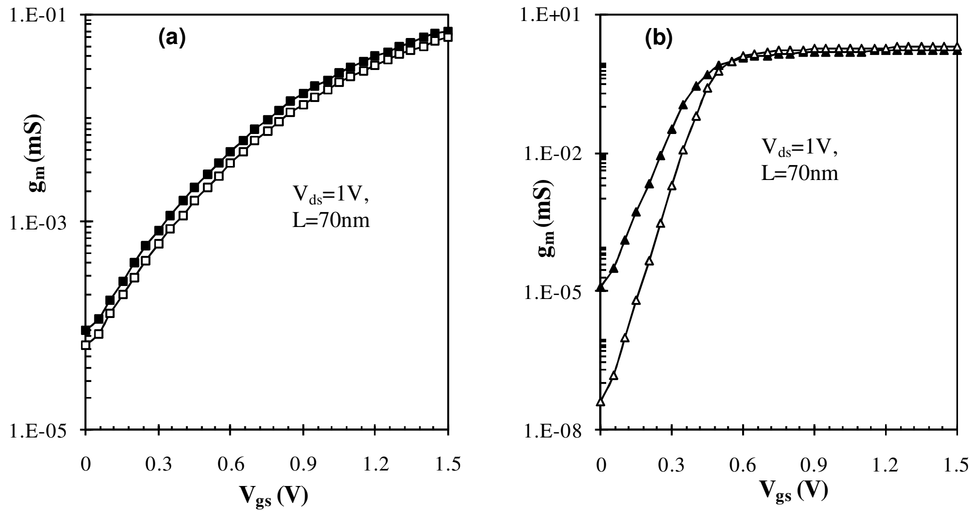

Figure 3. Variation of Transconductance (g_m) with V_{gs} at two different temperatures 300 and 400K a) DG-TFET b) DG-MOSFET. Symbols: (□□□) for DGTFET, (ΔΔΔ) for DG-MOSFET where Open symbols for 300K, Solid symbols for 400K.

$$E_g(T) = E_g(0) - \frac{alpha\ T^2}{T + beta} \quad (6)$$

For better linearity performance and effective suppression of nonlinear behavior introduced by g_{m3}, the optimum bias point is determined by the zero crossover point of g_{m3} (third order derivative of Transconductance g_{m1}) where its value is minimum and thereby suppressing the distortion created by g_{m3}. The maxima in the VIP_3 curve (corresponding to g_{m3} = 0) determines the selection of optimum bias point for device operation for MOSFETs. But for DG-TFET the peak in the VIP_3 curve is obtained at higher gate bias values as shown in fig. 4 (a). The peak has shifted to a lower gate bias with elevated temperature in case of DG-TFET. In case of DG-MOSFET there are two peaks appearing one at a higher gate bias and a local maxima at lower V_{gs} value. However for circuit applications the device operation in the moderate inversion regime is preferred so the maxima appearing at V_{gs}=0.5V can be considered as an optimum bias point for DG-MOSFETs. But as the temperature rises to 400 K the peak of the VIP_3 curve shifts further to lower V_{gs} (0.45V) as shown in fig. 4(b). This indicates the shifting of optimum bias point with temperature variation. Since in case of DG-TFET there is no peak appearing for the VIP_3 curve at the lower gate bias values we need to choose the optimum bias point on the basis of some other parameter, which is in this study is considered to be the intrinsic dc gain as will be discussed in the later part.

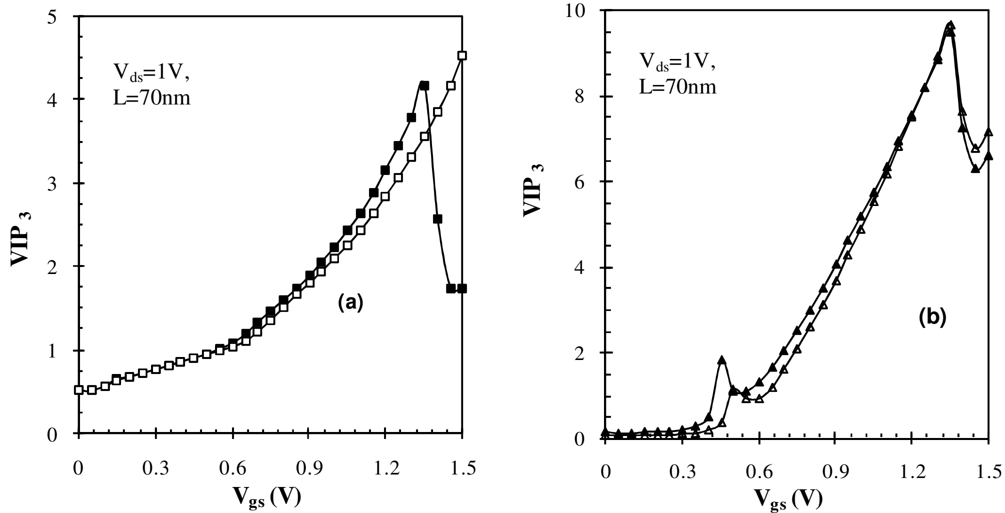

Figure 4. VIP_3 variation with V_{gs} for a) DG-TFET and b) DG-MOSFET. Symbols: (□□□) for DGTFET, (ΔΔΔ) for DG-MOSFET where Open symbols for 300K, Solid symbols for 400K.

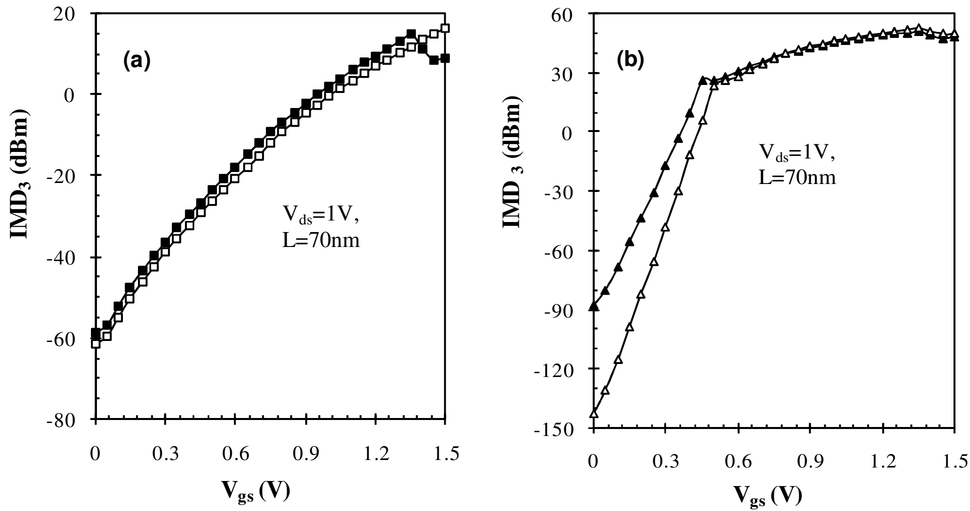

Figure. 5. IMD_3 variation with V_{gs} for a) DG-TFET and b) DG-MOSFET. Symbols: (□□□) for DGTFET, (ΔΔΔ) for DG-MOSFET where Open symbols for 300K, Solid symbols for 400K.

Fig. 5 shows the variation of IMD_3 with V_{gs} which determines the distortion performance of a device. For minimization of distortion this parameter should be low. As depicted, there is a very insignificant change in IMD_3 with rise in temperature in case of DG-TFET while it has degraded in the subthreshold to moderate inversion regime in case of DG-MOSFET. Moreover the value of IMD_3 is lower in comparison to DG-MOSFET near the bias point determined by VIP_3 in case of DG-MOSFET thus indicating better distortion suppression. Since in case DG-TFET, current increases with rise in temperature, thus a rise in the device efficiency (g_m/I_{ds}) can also be seen as shown in fig 6(a). In case of DG-MOSFET the device efficiency has degraded severely at elevated temperature as can be observed by fig. 6 (b), this is due to the degradation of I_{ds}-V_{gs} characteristics for high temperatures.

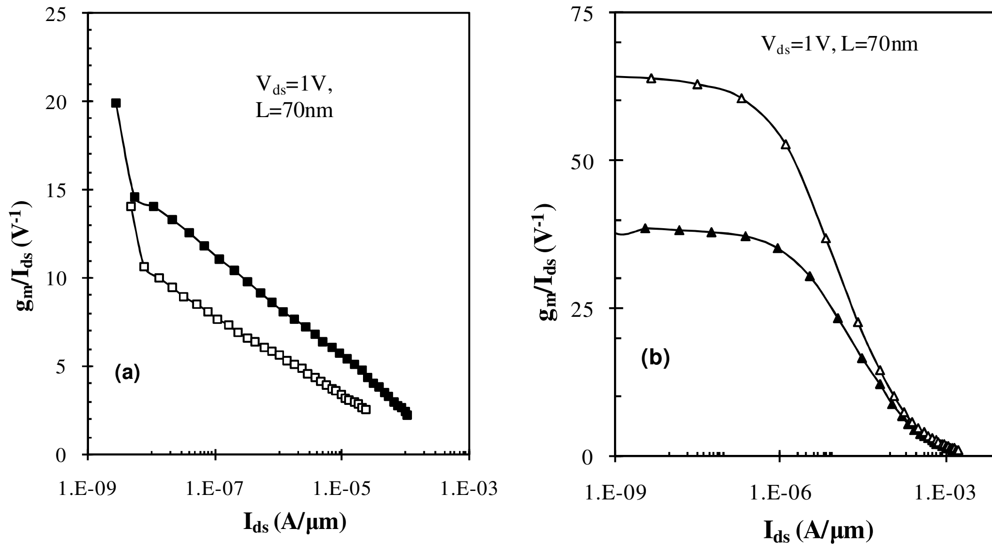

Figure 6. Device efficiency (g_m/I_{ds}) Vs I_{ds} for a) DG-TFET and b) DG-MOSFET. Symbols: (□□□) for DGTFET, (ΔΔΔ) for DG-MOSFET where Open symbols for 300K, Solid symbols for 400K.

Since the drain current has finite conductance (drain conductance g_d), and it is the result of CLM (channel length modulation) and Drain induced barrier lowering (DIBL) due to increase in drain voltage (V_{ds}) in case of a MOSFET, so the drain current is not constant in the saturation region.
The drain conductance is also an important analog performance parameter. A low value of drain conductance results in a high intrinsic gain (g_m/g_d) parameter. As depicted from fig. 7 (a) drain conductance for a DGTFET is very low as compared to a DGMOSFET (fig. 7 (b)) because the drain current saturation is better in case of a DGTFET, while for a DGMOSFET the CLM effect is visible in fig. 7(b). Figure 7 (a) also shows the effect of increasing gate bias on the drain conductance and it is seen that the drain saturation voltage shifts to higher values for high gate voltage. The low value of drain conductance results in high value of early voltage (V_{ea}) and R_{out} which are also important parameter for analog performance as shown in fig. 8 and 10. With increase in temperature drain conductance increases, the effect is more prominent at lower gate voltage for a DGMOSFET.

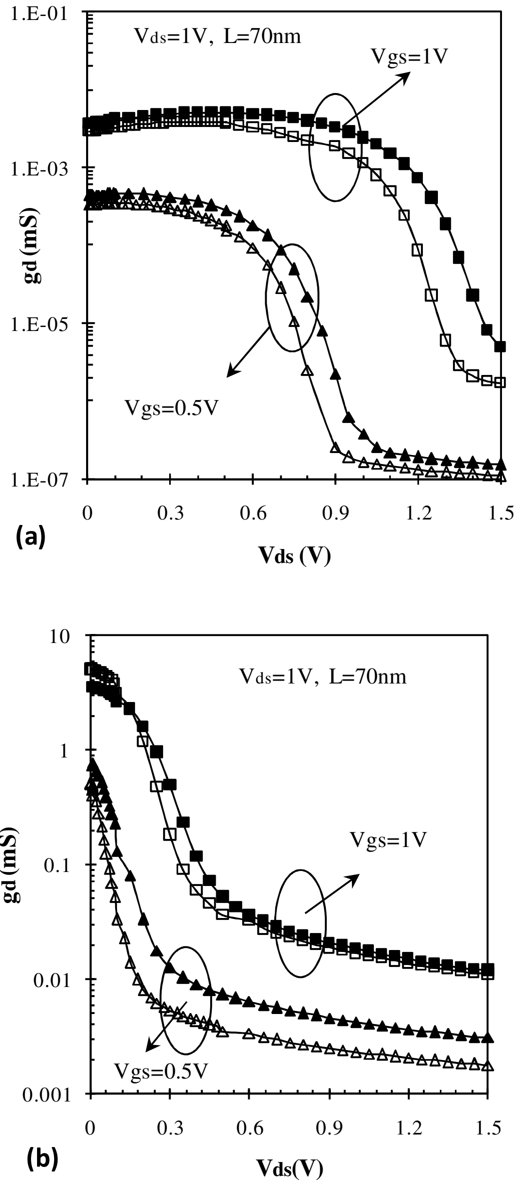

Figure 7 Drain conductance (g_d) at different gate bias for (a) DG-TFET (b) DGMOSFET. Symbols: Open symbols for 300K, Solid symbols for 400K.

Another important device parameter for analog circuit design is intrinsic dc gain g_m/g_d. The effect of temperature on g_m/g_d is shown in fig. 9. It is observed that the device gain does not degrade much in case of DG-TFET but the range of V_{gs} values over which the gain remains fairly constant and appreciable is reduced for higher temperature. But we can still choose the V_{gs} value where gain is appreciably higher and hence we can consider the g_m/g_d to be the parameter to determine the bias point at which a fairly high gain value is achieved with a decent linearity and distortion performance. In case of DG-MOSFET the gain reduces at elevated temperature.

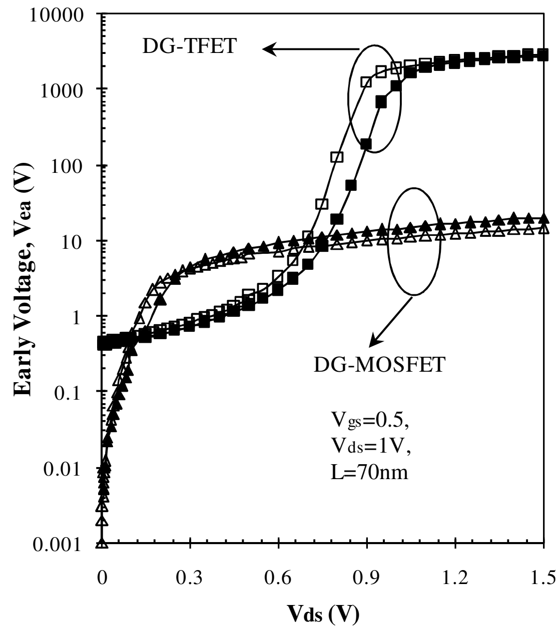

Figure 8. Early voltage (V_{ea}) variation with drain bias (V_{ds}) for DGTFET and DGMOSFET. Symbols: Open symbols for 300K, Solid symbols for 400K.

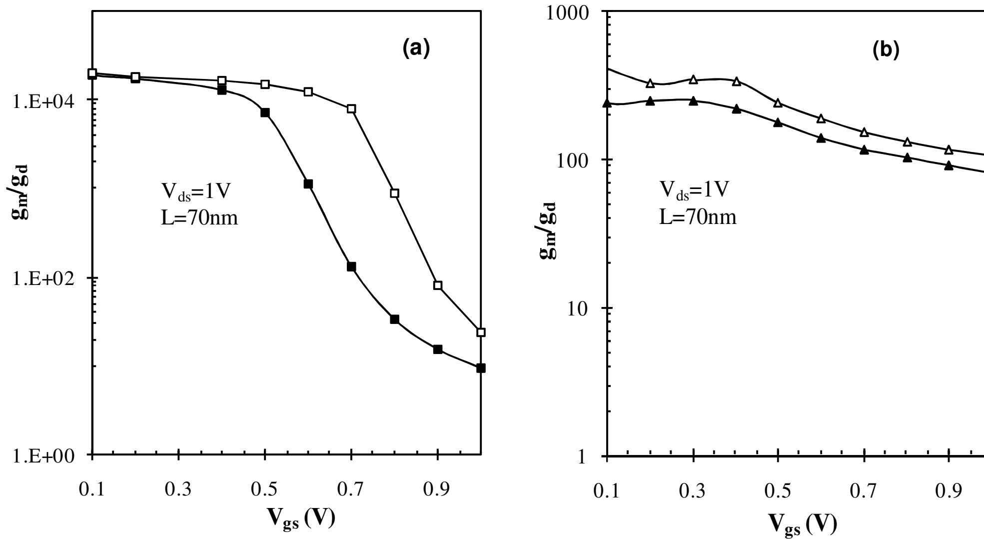

Figure 9. Intrinsic dc gain (g_m/g_d) Vs V_{gs} a) DG-TFET b) DG-MOSFET. Symbols: (□□□) for DGTFET, (ΔΔΔ) for DG-MOSFET where Open symbols for 300K, Solid symbols for 400K.

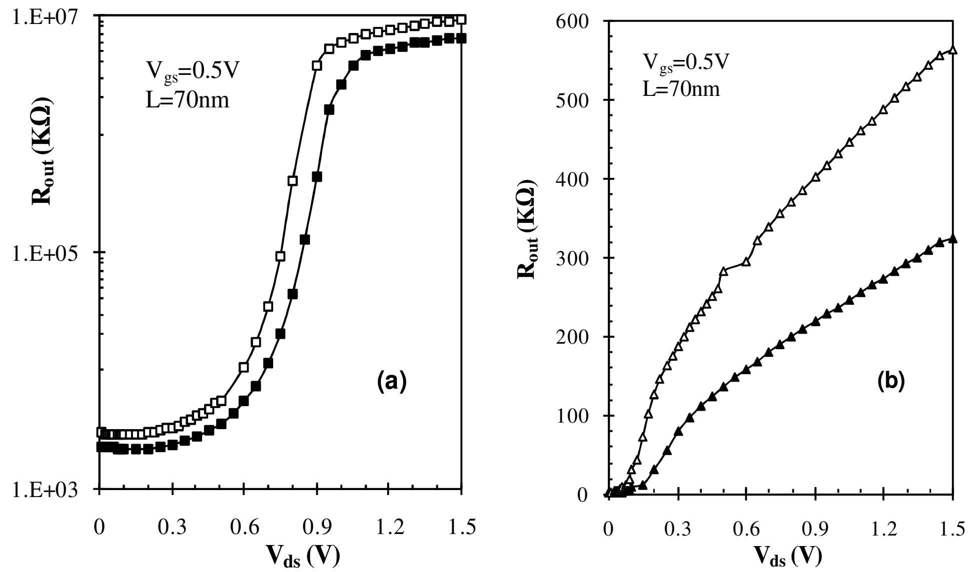

Figure 10. Output resistance (R_{out}) vs V_{ds} for a) DGTFET b) DGMOSFET. Symbols: (□□□) for DGTFET, (ΔΔΔ) for DG-MOSFET where Open symbols for 300K, Solid symbols for 400K

The drain output resistance degrades rapidly for a DG-MOSFET at higher temperature while the reduction is nominal in case of DG-TFET as shown in fig. 8. Thus DGTFET offers better analog performance as also predicted in an experimental demonstration of multiple gate TFET [17].
To study the dynamic performance, high frequency ac simulations are carried out in the range of 100MHz to 100 GHz. The parameter Current gain (H_{21}) is extracted and its variation with frequency is shown in fig. 11. Current gain ($H_{21} = \frac{g_m}{2\pi f\,(C_{gs} + C_{gd})}$) depends on trans conductance (g_m) and source, drain parasitic capacitances C_{gs} and C_{gd}. With increasing temperature, drain current increases in case of a TFET and so does transconductance, thus current gain also increases (fig. 11) and similarly the maximum available power gain also increases (fig.12). Cut off frequency which is evaluated as that frequency at which the current gain becomes unity. It also increases, because it directly depends on transconductance. The cut-off frequencies obtained at gate bias (V_{gs}=0.5V, V_{ds}=1V) are 1.84GHz, 2GHz and 2.54 GHz at temperatures 250K, 300K and 400K respectively. At high gate bias (saturation condition, V_{gs}=0.7V, V_{ds}=1V), cut off frequencies evaluated for a DGTFET are 4.9GHz, 5.4 and 6.4GHz at temperatures 250K, 300K and 400K respectively.

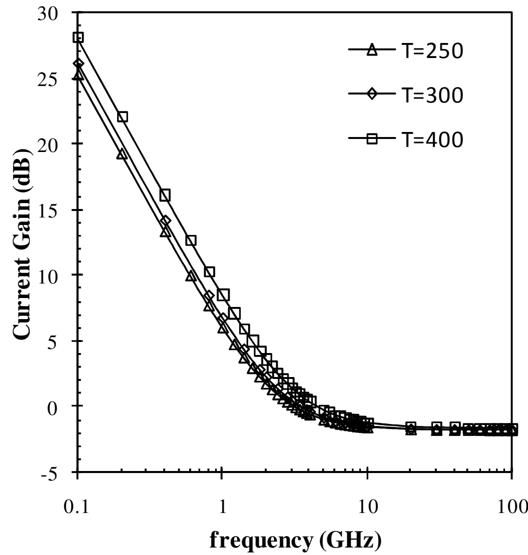

Figure 11. Current gain variation over frequency range at different temperatures for a DGTFET L=45nm, V_{gs}=0.5V, V_{ds}=1V

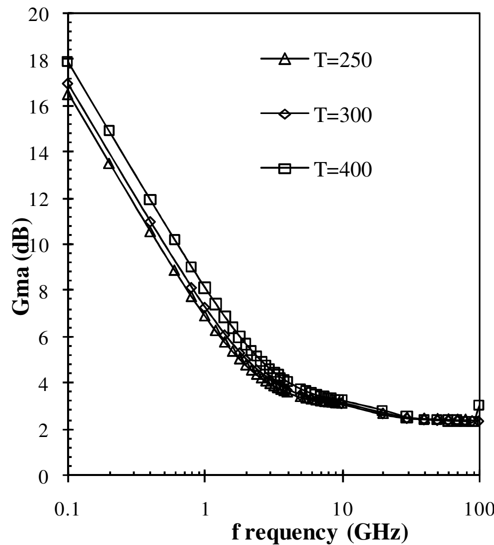

Figure 12. Variation of maximum available power gain with frequency for a DGTFET at different temperatures. L=45nm, V_{gs}=0.5V, V_{ds}=1V

5. IMPACT OF GATE STACK

In this section, the impact of Gate Stack architecture on various linearity and analog performance parameters are studied. Since use of high-k is considered to be an alternative to overcome the impediments of low ON currents in case of TFETs. So in view of that the performance of DG-TFET has been studied with Gate Stack architecture and the possible enhancements brought about are investigated.

As can be seen from fig. 13 (a) the trans conductance has improved with the usage of a high-k dielectric Gate Stack architecture due to the enhanced gate control and current driving capability. The linearity FoM, VIP_2 has also enhanced for a Gate Stack DG-TFET. Similarly the impact can also be depicted by the shifting of the peak of VIP_3 to lower gate bias and improvement in the magnitude at the lower V_{gs} values (fig. 14(a)). The IMD_3 parameter degrades for Gate Stack DG-TFET as shown by fig. 14(b).

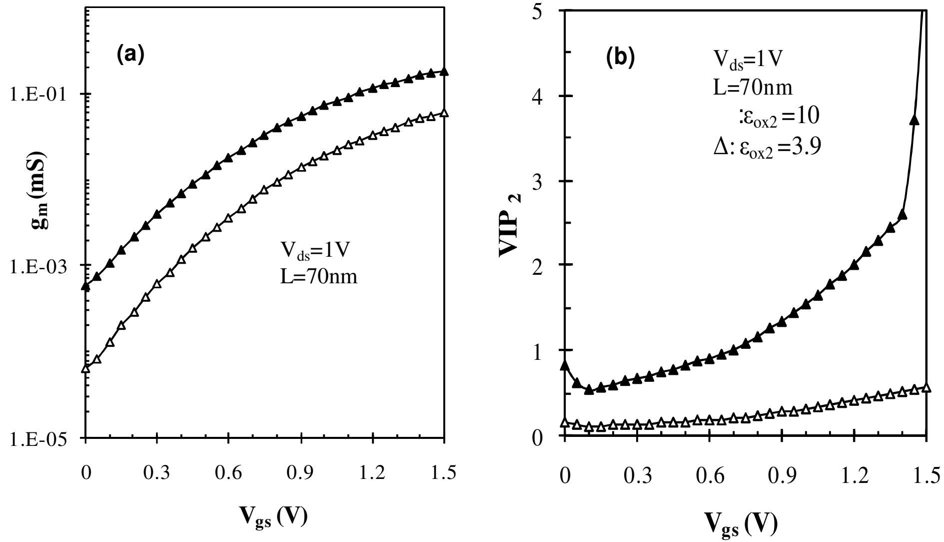

Figure 13. a) Transconductance (g_m) variation with V_{gs} (b) VIP_2 variation with V_{gs} for DG-TFET with SiO_2 and Gate Stack architecture. Open symbols (ΔΔΔ) for DG-TFET with ε_{ox2} =3.9 Solid symbols (▲▲▲) for GS-DG-TFET with ε_{ox2} =10.

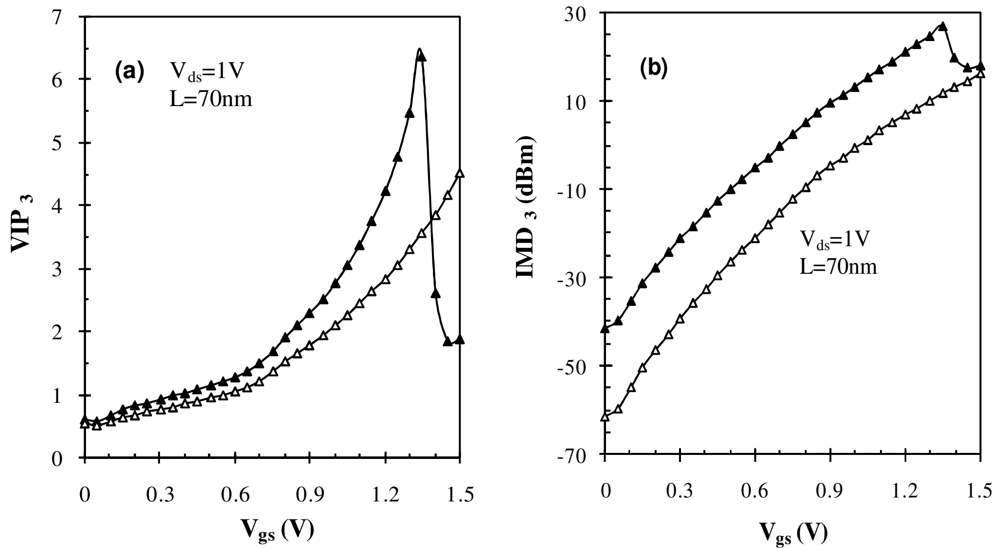

Figure 14. VIP_3 variation with V_{gs} (b) IMD_3 variation with V_{gs} for DGTFET with SiO_2 and Gate Stack architecture. Open symbols (ΔΔΔ) for DG-TFET with ε_{ox2} =3.9 Solid symbols (▲▲▲) for GS-DG-TFET with ε_{ox2} =10.

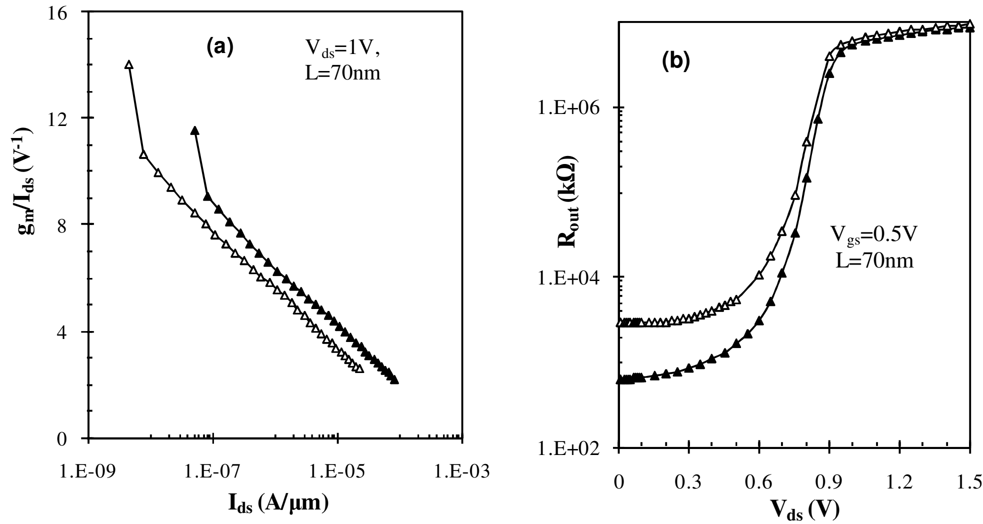

Figure. 15. (a) Device efficiency (g_m/I_{ds}) variation with I_{ds} (b) Output resistance R_{out} variation with V_{ds} for DGTFET with SiO_2 and Gate Stack architecture. Open symbols (ΔΔΔ) for DG-TFET with ε_{ox2} =3.9 Solid symbols (▲▲▲) for GS-DG-TFET with ε_{ox2} =10.

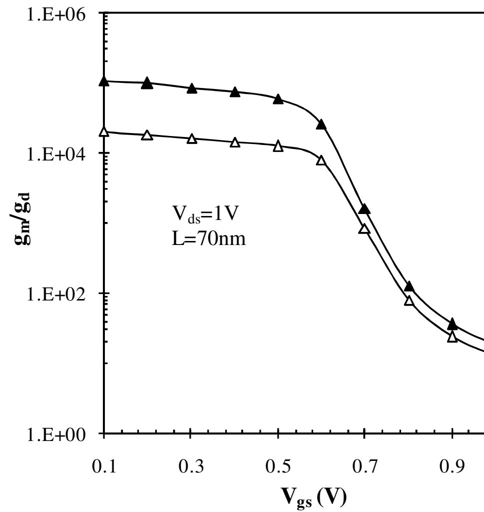

Figure 16. Intrinsic dc gain (g_m/g_d) comparison for a DG-TFET and Gate Stack-DG-TFET. Open symbols (ΔΔΔ) for DG-TFET with ε_{ox2} =3.9 Solid symbols (▲▲▲) for GS-DG-TFET with ε_{ox2} =10.

The drain output resistance (fig. 15(b)) degrades at lower V_{ds} values for a GS- DGTFET as compared to without gate stack DG-TFET implying an increased effect of drain voltage at the source side due to the improved gate control over the channel.

As fig. 15 (a) shows that the device efficiency has improved for higher drain current value (inversion regime) for Gate Stack architecture as compared to a low k dielectric (SiO_2) based DG-TFET. This improvement is also reflected in the intrinsic dc gain value (fig. 16) which has

significantly improved for GS-DGTFET. This improvement is due to the enhanced current and Transconductance (g_m) due to the improvement of gate control introduced by gate stack.

6. CONCLUSIONS

The impact of temperature variation and introduction of Gate Stack architecture on the linearity and analog performance of a DG-TFET has been studied. It has been shown that TFETs are more immune to temperature variations in terms of its stable bias point selection based on achieving high dc gain value, which is an advantage as compared to DG-MOSFET in which the bias point chosen varies with temperature variations. The suppression of distortion is better in case of DG-TFET as compared to DG-MOSFET and they also offer a high drain output resistance (due to a lower DIBL effect), early voltage and intrinsic dc gain which does not significantly degrade even at high temperature range. Further improvement in terms of linearity and higher gain can also be obtained by using Gate Stack architecture.

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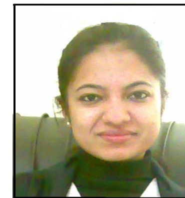

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