Impact of Interface Fixed Charges on the Performance of the Channel Material Engineered Cylindrical Nanowire MOSFET

Rajni Gautam[1], Manoj Saxena[2], R.S.Gupta[3] and Mridula Gupta[1]

[1] Semiconductor Device Research Laboratory, Department Of Electronic Science.
University Of Delhi, South Campus, Benito Juarez Road, New Delhi, India
Email: rajni7986@gmail.com, mridula@south.du.ac.in
[2] Department Of Electronics, Deen Dayal Upadhyaya college,
University Of Delhi, Karampura, New Delhi, India
saxena_manoj77@yahoo.co.in
[3] Department Of Electronics and communication Engineering ,
Maharaja Agrasen Institute Of Technology, Sector 22, Rohini, Delhi, India
rsgu@bol.net.in

ABSTRACT

The paper presents a simulation study of effect of interface fixed charges on the performance of the cylindrical nanowire MOSFET for different channel materials (Si, GaAs and Ge). The objective of the present work is to study the effect of hot carrier damage/stress induced damage/process damage/radiation damage induced fixed charges at the semiconductor-oxide interface of the cylindrical nanowire MOSFET. Also the circuit reliability issues of the device are discussed in terms of the performance degradation due to interface fixed charges. The performance has been compared for the three materials in terms of drain current driving capability, I_{on}/I_{off} ratio, early voltage, transconductance, parasitic gate capacitance, intrinsic delay, current gain and power gain of the device.

KEYWORDS

ATLAS-3D, channel length modulation, fixed Charges, hot carrier effect, interface traps, nanowire MOSFET.

1. INTRODUCTION

This Silicon technology is all pervasive and underpins the IT revolution that is now reshaping society. The technology keeps improving year on year as chip sizes are being continually reduced and transistor speeds increase. However as we reduce the dimensions SCEs cause several problems such as threshold voltage lowering, increased substrate bias effect while the narrow width transistors cause a decrease of current derivability and reliability degradation due to large fields. To continue the scaling of Si CMOS in the sub-65nm regime, innovative device structures and new materials have to be created in order to continue the historic progress in information processing and transmission. Examples of novel device structures being investigated are double gate or surround gate MOS and examples of novel materials are high mobility channel materials like strained Si, Ge and GaAs, high-k gate dielectrics and metal gate electrodes. As the semiconductor industry approaches the limits of traditional silicon CMOS scaling, introduction of performance boosters like novel materials and innovative device structures has become necessary

DOI : 10.5121/vlsic.2011.2319

for the future of CMOS. High mobility materials are being considered to replace Si in the channel to achieve higher drive currents and switching speeds. Ge [1]-[2] has particularly become of great interest as a channel material, owing to its high bulk hole and electron mobilities. MOSFETs based on III-V semiconductors promise to combine III-V high frequency performance with scalability and integration known from silicon. GaAs MOSFET technology is used where high RF power is required at low voltage and high efficiency, i.e. wireless and mobile products. The technology also have a unique advantage in regard to integration of RF power, switching, and power control functions. This is of interest where integration lowers cost and enables new functionality. GaAs MOSFET [3]-[4] has many advantages over Silicon MOSFET such as higher electron mobility, shorter transit time, higher resistivity. But as GaAs has no native oxide thereby it limits the voltage that can be applied to the gate. Also, GaAs has lower thermal conductance. Besides the channel material engineering in order to overcome scaling limitations several novel geometrical device structures were proposed. One such structure is the cylindrical nanowire MOSFET where gate has greater influence over the channel potential and reduces the short channel effects and improves subthreshold slope [5]. In addition it enables use of an undoped channel, which has the potential to minimize threshold voltage variation due to reduced random dopant fluctuations. Nanowire MOSFET is considered as one of the promising candidates for further extending the device downsizing, owing to its gate-all-around(GAA) structure which enables better gate control capability than planar transistors [5]. Si nanowire FET has been fabricated by several techniques including, Si Fins are patterned by lithography and etching followed by the oxidation i.e. Top-down approach [6] or Methods using CVD, MBE and other processes to grow Si nanowire with better controllability of the size of the wire i.e. Bottom-up approach [7]. Several papers have been reported on analytical modeling of SRG MOSFET [8]-[10]. Device aging is becoming a big problem for the optimum performance of the recent age devices. There are many factors responsible for device aging problems: (1)process induced damage [11], (2)stress induced damage [12], (3) radiation induced damage [13] and (4) hot carrier induced damage [14]. The degradation of short-channel MOSFET characteristics due to the injection of hot carriers into the gate oxide stands as one of the most important challenges to further progress of device down-scaling [15]-[17]. The device aging induced by hot- electron injection is summarized in the formation of a narrow defective interface region. The interface trap or oxide-trapped charges which exist at the semiconductor-oxide interface can be transformed into equivalent interface fixed charges. Recently hot carrier effect has been studied in SOI MOSFET [18] and pi-gate p-MOSFET [19]. F.Djeffal *et al.* studied the effects of hot carrier induced interface fixed interface charges for DG and Gate All Around (GAA) MOSFET [20]. Chiang *et al.* [21] proposed an analytical threshold voltage model of Surrounding-Gate MOSFETs with localized interface trapped charges. With the scaling down of Si technologies, the Radio Frequency (RF) Figure of Merits (FOMs) such as intrinsic delay (or cut-off frequency) and minimum noise figure (NF) of MOSFET are greatly improved to allow high performance RF applications. As a result, RF performance of CMOS devices has attracted significant amount of interest [22],[23]. In this paper three different channel materials i.e. Si, Ge and GaAs have been used to compare the performance of the nanoscale cylindrical SRG MOSFET in two cases: damaged and undamaged device. The effect of interface fixed charges on the device characteristics (potential, drain current, transconductance, early voltage, parasitic capacitance, intrinsic delay, current and power gain) has been analyzed by extensive simulation using ATLAS 3-D device simulator [24].

2. SIMULATION DETAILS

Nanoscale surrounding cylindrical gate MOSFET with interface interface fixed charges has been simulated using ATLAS-3D device simulator [24] using drift diffusion approach and the models activated in simulation comprise field dependent mobility, concentration dependent mobility model along with the Shockley– Read–Hall (SRH) models for minority carrier recombination. Density of fixed charges, substrate and source/drain doping densities and all other parameters are

taken from the work of [21]. All the simulations have been performed at room temperature. Model parameters used for simulation are given in Table1.

The schematic cross section of the structure with interface fixed charges is shown in Fig.1. Channel has divided into two regions, i.e.L_2 (length of damaged region) and L_1 (damage free part i.e. L-L_2). In simulation INTERFACE statement along with its density and position parameters are used to define the damaged region at the interface. Models for quantum mechanical effects (QME) have not been invoked as QME come into picture when radius of the silicon pillar is less than 5 nm [25]. Uniform distribution of interface fixed charges has been used in the analysis.

Table1. Model Parameters used in simulation.

Model	Parameters (Electron)	Parameter (Hole)
Concentration dependent mobility	Using look up table μ_o=1300 cm^2/Vs	Using look up table μ_o=491.1 cm^2/Vs
Field dependent mobility $\mu(E)=\mu_O\left\lvert\frac{1}{1+\left(\frac{\mu_O E}{v_{sat}}\right)^{\beta}}\right\rvert^{\frac{1}{\beta}}$	v_{sat} = $1.03\text{x}10^7$ cm/s β =2	v_{sat} = $1.03\text{x}10^7$ cm/s β =2
Recombination $R_{SRH}=\frac{pn-n_i^2}{\tau_p\left\lvert n+n_i\exp\left(\frac{E_{trap}}{kT}\right)\right\rvert+\tau_n\left\lvert p+n_i\exp\left(\frac{-E_{trap}}{kT}\right)\right\rvert}$	E_{trap} =0V τ_n =$1\text{x}10^7$ s	E_{trap} =0V τ_p =$1\text{x}10^7$s

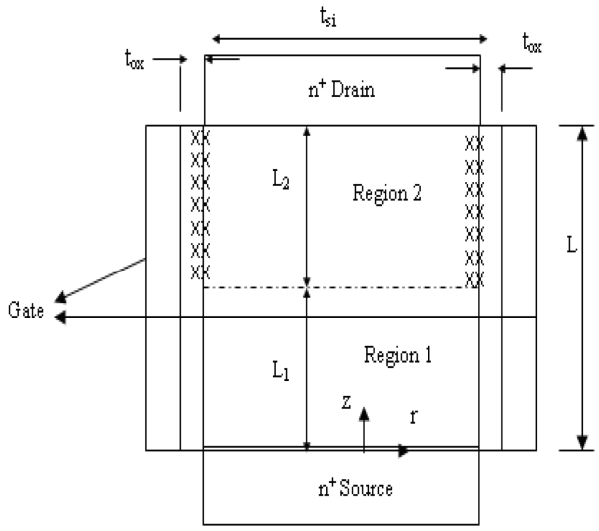

Fig. 1 Schematic cross section of the simulated Nanowire MOSFET structure. Other parameters Channel Length (L)=70 nm, Length of damaged region (L_2)=35nm, Oxide thickness (t_{ox})=1.5 nm, Radius of Silicon pillar ($R=t_{si}/2$)=15nm, Source/Drain doping (N_d)=$1x10^{26}m^{-3}$, Substrate Doping (N_a)=$1x10^{21}m^{-3}$.

3. RESULT AND DISCUSSION

The interface near the drain side is susceptible to strongest electric field and the high field-induced hot carriers will create permanent damage. Similarly, radiation damage/stress induced damage/process damage cause interface traps at the semiconductor-oxide interface. As the interface traps appears at the semiconductor-oxide interface, it is known that it will accept an electron if the trap level is located beneath the fermi level for an acceptor-type interface trap. In this situation, it acts as a fixed negative charge. Similarly for a donor type interface trap it acts as fixed positive interface charge. Therefore, interface traps can be transformed into equivalent interface fixed charges. There is a band banding due to the work function difference between the metal and the semiconductor in MOS device. Fixed charges at the interface causes additional band bending under the gate which in turn causes change in flat band voltage in the damaged region. Thus surface potential is lowered (raised) in case of negative (positive) interface fixed charges in the damaged region w.r.t the undamaged device as shown in fig.2. It can be shown that minimum surface potential and its position remains nearly unchanged for positive fixed charges but it gets shifted towards drain side for negative fixed charges. Fig.3 shows the surface potential when the fixed charges are located near the source side for all the three materials. In case of fixed charges present near the source side minimum potential and its position is changed (unchanged) for positive (negative) interface fixed charges. Also positive (negative) fixed charges provides screening to the undamaged region from the higher drain to source bias (V_{ds}) effects in case of fixed charges are present near the drain (source) side just as in case of DMG structure. Thus minimum surface potential and its position changes and induces a shift in the threshold voltage. Although magnitude of surface potential is different because of the different values of semiconductor work function for the three materials but the change in surface potential due to fixed charges is same as it depends only on the oxide properties (relative permittivity and thickness) and the density of fixed charges.

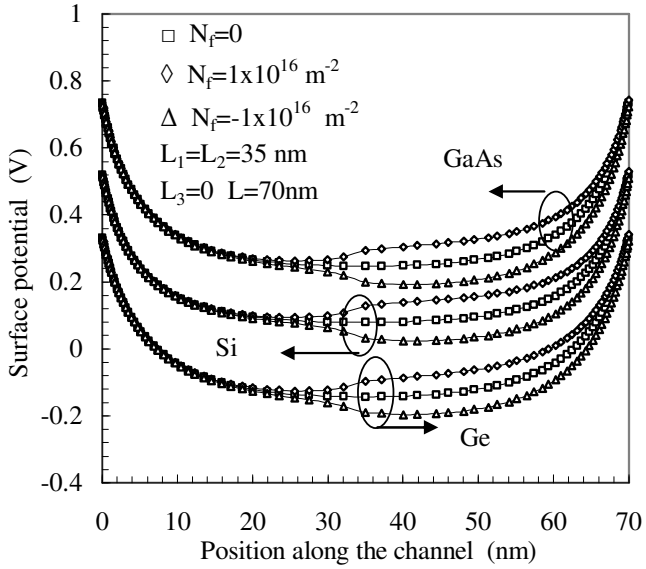

Fig. 2 Surface Potential as a function of distance along the channel when fixed charges are located at the drain side. Other parameters are: t_{ox} =1.5 nm, R=15nm, N_d =1x10^{26} m^{-3}, N_a=1x10^{21} m^{-3}, V_{gs}=0V, V_{ds}=0V, L_1=L_2=L/2.

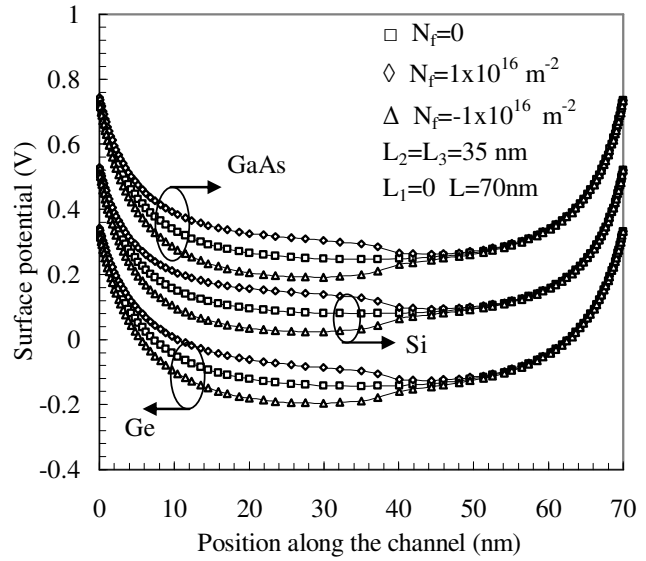

Fig. 3 Surface Potential as a function of distance along the channel when fixed charges are located at source side. Other parameters are: t_{ox} =1.5 nm, R=15nm, N_d =1x10^{26} m^{-3}, N_a=1x10^{21} m^{-3}, V_{gs}=0V, V_{ds}=0V, L_1=L_2=L/2.

All the three devices i.e. Si, Ge and GaAs SRG MOSFETs have been optimized to have same threshold voltage (i.e. V_{th}= 0.3V) by adjusting the metal work function so as to compare their performance in terms of degradation caused due to interface fixed charges. Fig.4 and 5 shows the effect of fixed charges on the transfer characteristics. Performance is compared taking Si as the reference. It clearly shows that the among the three channel materials GaAs shows highest current

driving capability then Ge followed by Si. This is because of higher mobility. Also the drain current degradation is there for damaged device. Although drain current is increased (decreased) for positive (negative) interface fixed charges in all regions i.e. subthreshold, linear and saturation but the order of change in off current is greater than the on current. Thus overall effect is enhanced I_{on}/I_{off} ratio in case of negative fixed charges and reduced I_{on}/I_{off} ratio in case of positive fixed charges. Fig. 6 shows the I_{on}/I_{off} ration for all cases i.e. all three materials both undamaged and damaged device. Also the I_{on}/I_{off} ratio is highest for GaAs.

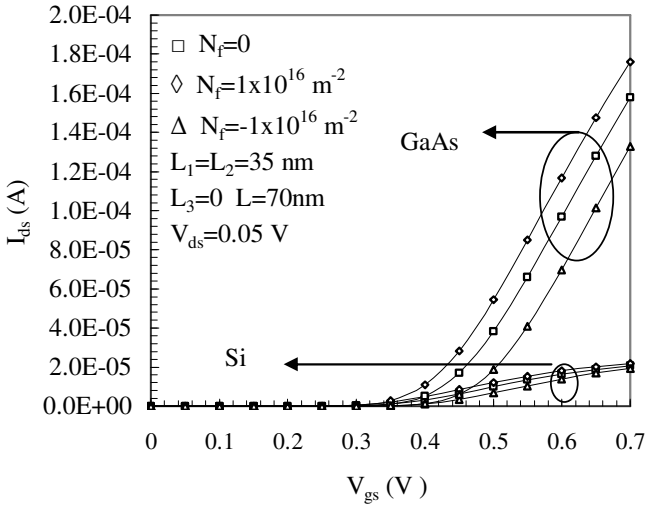

Fig. 4 Drain current as a function of gate to source voltage for Si and GaAs. Other parameters are: t_{ox} =1.5 nm, R =15nm, N_d =1x10^{26} m^{-3}, N_a=1x10^{21} m^{-3}, L_1=L_2=L/2, V_{ds}=0.05V.

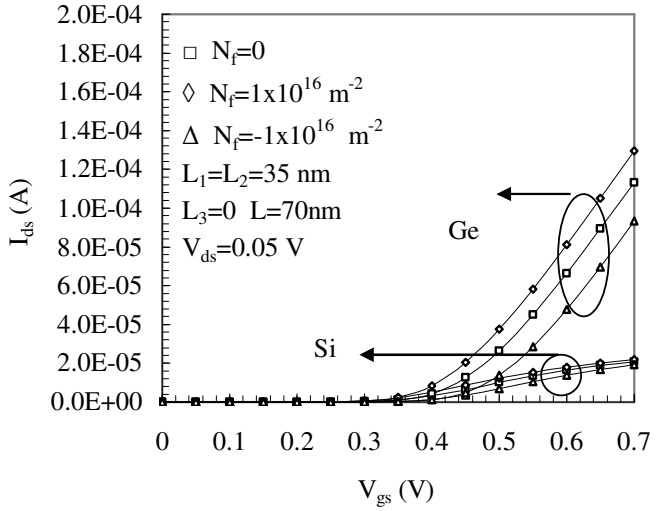

Fig. 5 Drain current as a function of gate to source voltage for Si and Ge. Other parameters are: t_{ox} =1.5 nm, R =15nm, N_d =1x10^{26} m^{-3}, N_a=1x10^{21} m^{-3}, L_1=L_2=L/2, V_{ds}=0.05V.

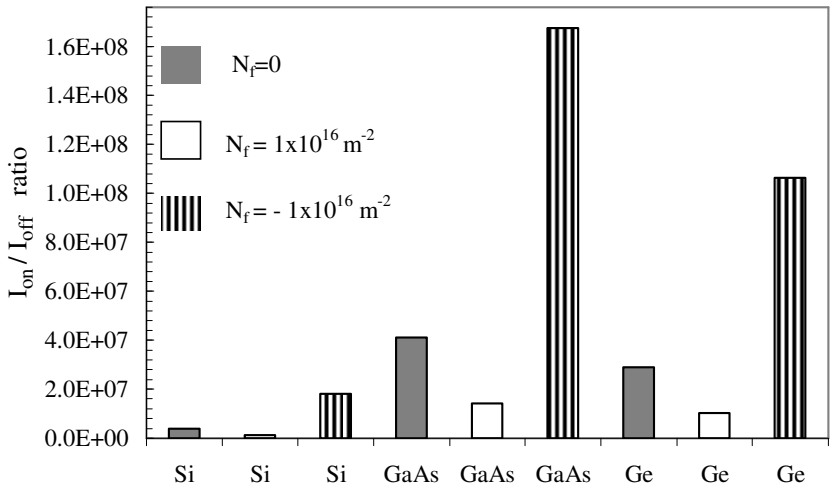

Fig. 6 I_{on}/I_{off} ratio for all materials. Other parameters are: t_{ox} =1.5 nm, R=15nm, N_d =1x10^{26}m^{-3}, N_a=1x10^{21} m^{-3}, L=70nm, N_f=± 1x10^{16} m^{-2}, L_1=L_2=L/2, V_{ds}=0.05V.

Fig. 7 and 8 illustrate the I_{ds}-V_{ds} characteristics of the device in inversion region i.e. at V_{gs}=0.6V. Taking Si as the reference it can be shown that GaAs shows better output characteristics. Important observation here is the increase in drain current with drain bias and a reduction of output resistance in saturation region. This is due to the channel length modulation (CLM) effect i.e. shortening the length of the channel region at higher drain bias. This variation in drain current can be better understood by studying the early voltage. Fig. 9, 10 and 11 illustrate the impact of fixed charges on the early voltage for Si, GaAs and Ge respectively. As can be seen from the figures Si has the highest early voltage and Ge has the lowest. Thus Si has better immunity against CLM effect which is a common short channel effect in nanoscale devices. Also positive (negative) fixed charges lead to enhanced (reduced) early voltage because of the screening effect provided by the damaged region to the undamaged region. For 1x10^{16} m^{-2} density of localised charges there is a increase (decrease) by 46.44% (30.1%) in the early voltage for Si.

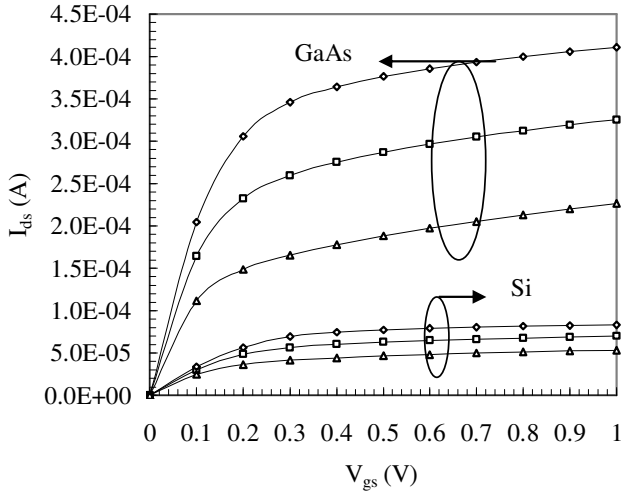

Fig.7 Drain current as a function of drain to source voltage for Si and GaAs. Other parameters are: t_{ox} =1.5 nm, R =15nm, N_d =1x10^{26} m^{-3}, N_a=1x10^{21} m^{-3}, L_1=L_2=L/2, V_{gs}=0.6V.

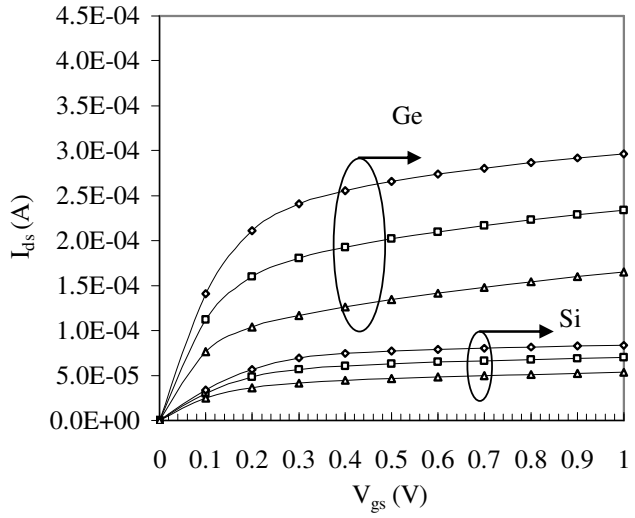

Fig.8 Drain current as a function of drain to source voltage for Si and Ge. Other parameters are: t_{ox} =1.5 nm, R =15nm, N_d =1x10^{26} m^{-3}, N_a=1x10^{21} m^{-3}, L_1=L_2=L/2, V_{gs}=0.6V.

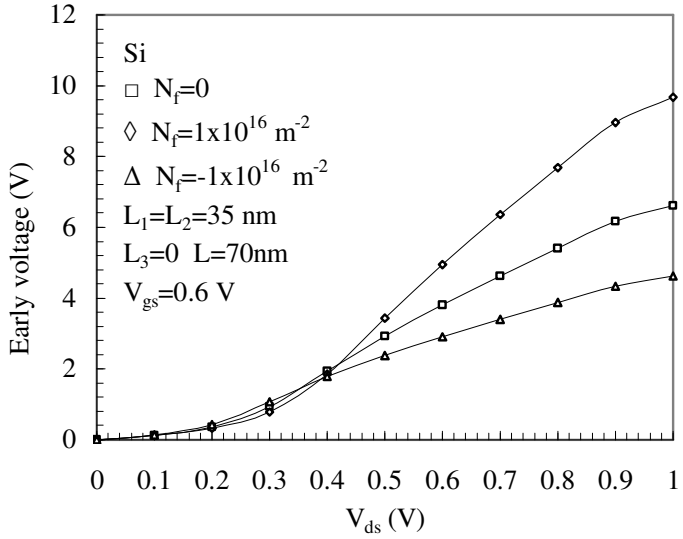

Fig.9 Early voltage as a function of drain to source voltage for Si. Other parameters are:

t_{ox} =1.5 nm, R=15nm, N_d =1x10^{26} m^{-3}, N_a=1x10^{21} m^{-3}, L_1=L_2=L/2, V_{gs}=0.6V.

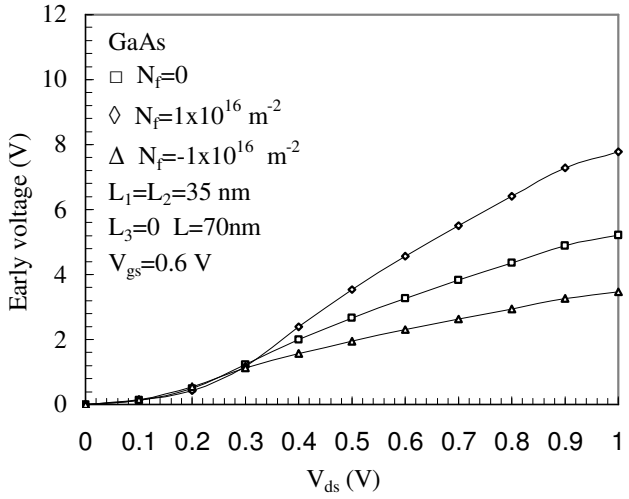

Fig.10 Early voltage as a function of drain to source voltage for GaAs. Other parameters are: t_{ox} =1.5 nm, R =15nm, N_d =1x10^{26} m^{-3}, N_a=1x10^{21} m^{-3}, L_1=L_2=L/2, V_{gs}=0.6V.

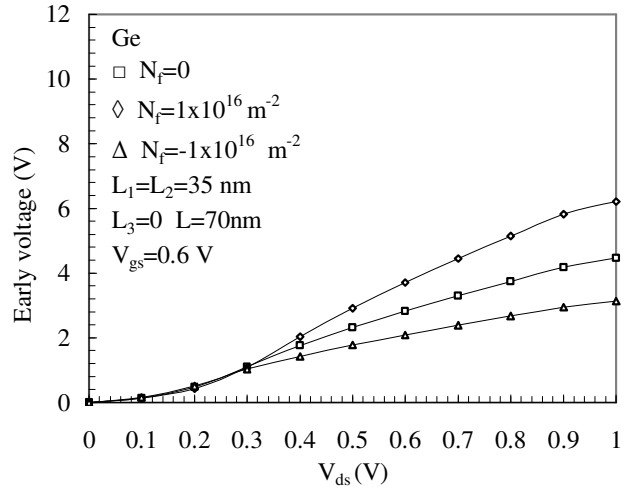

Fig.11 Early voltage as a function of drain to source voltage for Ge. Other parameters are: t_{ox} =1.5 nm, R =15nm, N_d =1x10^{26} m^{-3}, N_a=1x10^{21} m^{-3}, L_1=L_2=L/2, V_{gs}=0.6V.

Gain of any device is given by its transconductance and peak of transconductance curve gives the optimum bias point if device is to be used as an amplifier. Fig.12 and 13 shows the impact of interface fixed charges on the transconductance of the device. As can be seen positive (negative) fixed charges result in reduced (enhanced) transconductance in inversion region. At V_{gs}=0.6V for 1x10^{16} m^{-2} density of positive (negative) localized charges, decrease (increase) in transconductance of the device is 10.59% (18.22%), 0.81% (2.44%) and 5.4% (7.19%) for Si, GaAs and Ge respectively. Thus Si nanowire MOSFET is most affected by the localized charges. Also the peak of the transconductance curve shifts towards lower (higher) V_{gs} values. This has a serious impact on the circuit reliability of the device since it changes the bias point of the device. Also GaAs (Si) has the highest (lowest) transconductance and hence highest (lowest) gain among the three channel materials used.

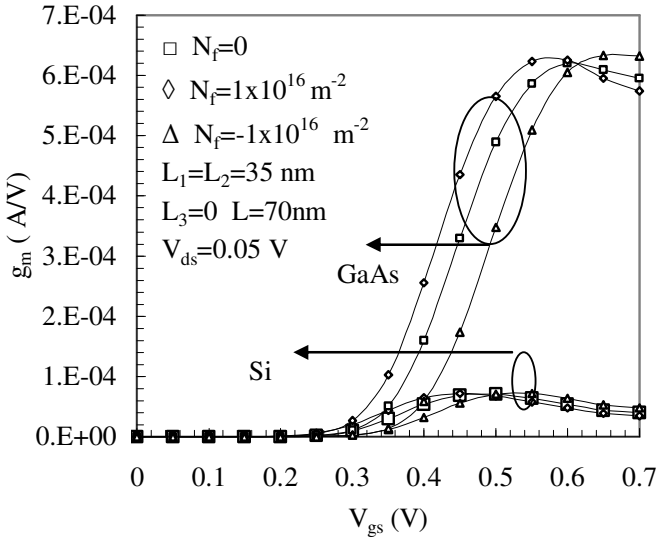

Fig.12 Transconductance as a function of gate to source voltage for Si and GaAs. Other parameters are: t_{ox} =1.5 nm, R =15nm, N_d =1x10^{26} m^{-3}, N_a=1x10^{21}m^{-3}, L_1=L_2=L/2, V_{ds}=0.05V.

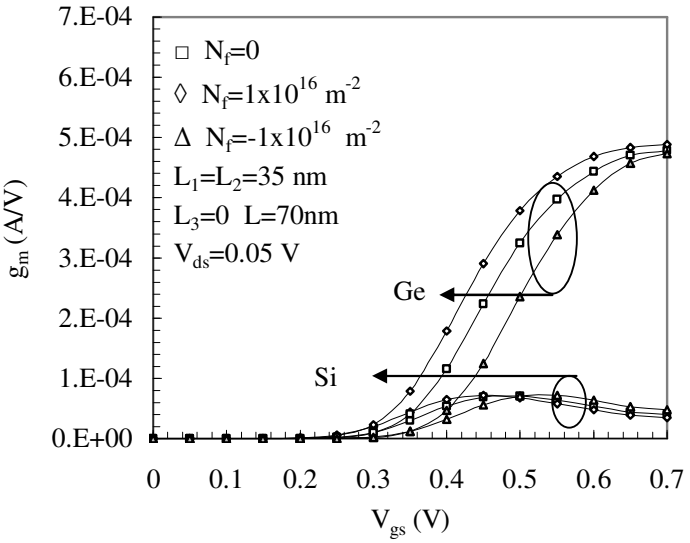

Fig.13 Transconductance as a function of gate to source voltage for Si and Ge. Other parameters are: t_{ox} =1.5 nm, R =15nm, N_d =1x10^{26} m^{-3}, N_a=1x10^{21}m^{-3}, L_1=L_2=L/2, V_{ds}=0.05V.

Another important metric used to benchmark the performance of a transistor in a circuit configuration is the intrinsic delay which is defined as [26]

$$\frac{1}{4} * C_{gg} * I_{on} * V_{ds} \quad (1)$$

where C_{gg} is the total gate capacitance and I_{on} is the on-current. For RF applications, device degradation is mainly attributed to the existence of the parasitic capacitances: gate-to-source (C_{gs}) and gate-to-drain (C_{gd}). C_{gg} is the total gate capacitance which includes C_{gs} and C_{gd}. Low parasitic capacitances can significantly improve the device speed performance and hence can

reduce the power dissipation. Thus C_{gg} has to be as low as possible for a higher cut-off frequency to meet the desired RF requirements. Fig.14 illustrates the behavior of C_{gg} in presence of localised charges for Si, Ge and GaAs. As can be seen from the fig.14, C_{gg} is lowest for GaAs leading to high speed and low power dissipation. Since the localized charges present at semiconductor-oxide interface changes the charges distribution in the damaged region in the channel thus degrading the C_{gg}. Positive localised charges increases the value of C_{gg} whereas negative localised charges decreases the C_{gg} value. The Intrinsic delay is a function of C_{gg} and represents the fundamental RC delay of the device (where R is the device resistance and C is the capacitance) and provides a frequency limit for transistor operation that is relatively insensitive to gate dielectrics and device width, and thus, represents a good parameter for comparing different types of devices. Fig.15 compares the damaged and undamaged Si, Ge and GaAs devices using the intrinsic delay metric. As is clear from the fig.15, intrinsic delay of the damaged device with negative localised charges is significantly higher than the undamaged device i.e. induced negative localised charges leads to a significant enhancement of intrinsic delay whereas positive localized charges leads to reduction in intrinsic delay. As can be seen from the graph, the change in intrinsic delay due to positive (negative) localized charges is 4.52% (8.9%), 18.34% (38.6%), 10.65% (23.7%) in case of Si, Ge and GaAs respectively. Thus Ge has the highest impact of localized charges on its intrinsic delay. Again GaAs has the lowest delay thus a better candidate among the three materials for high speed, high frequency applications.

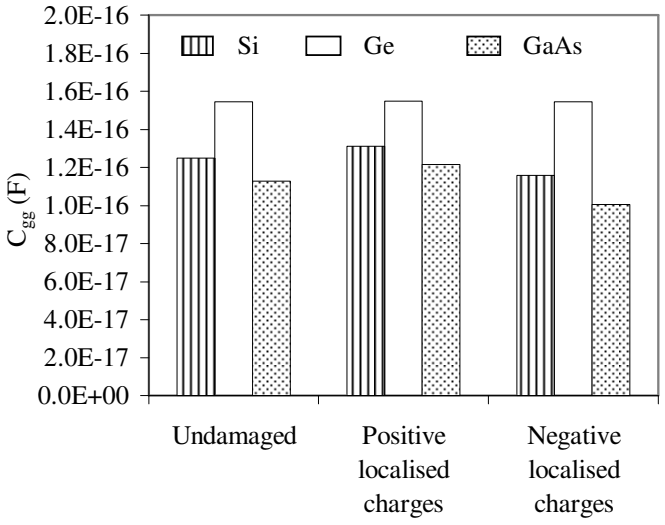

Fig.14 Impact of localized charges on gate capacitance. Other parameters are: L=70nm, t_{ox} =1.5 nm, R =15nm, $N_d = 1x10^{26}$ m^{-3}, $N_a = 1x10^{21} m^{-3}$, $L_1 = L_2 = L/2$, V_{gs}=0.6V, V_{ds}=0.05V.

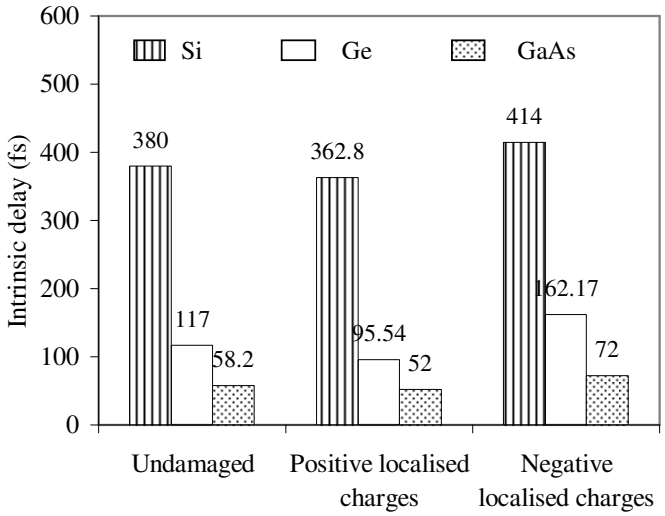

Fig.15 Impact of localized charges on intrinsic delay of the device. Other parameters are: L=70nm, t_{ox} =1.5 nm, R =15nm, N_d =1x10^{26} m^{-3}, N_a=1x$10^{21}$$m^{-3}$, L_1=L_2=L/2, V_{gs}=0.6V, V_{ds}=0.05V.

If the device is to be used as an amplifier, then its quality can be characterized by a number of specifications and the most important is the gain. The evaluation of current gain, h21, is an important parameter to investigate the RF performance of the device. As can be seen from the fig.16 GaAs has 37.7% higher gain than Si and 13.24% than Ge for undamaged case. Also positive (negative) localized charges lead to reduction (enhancement) in current gain by 3.82% (39.78%) , 0.4% (6.45%), 1.02% (1.53%) for Si, Ge and GaAs nanowire MOSFET respectively due to lower transconductance in inversion region. Thus impact of localized charges on the current gain is highest in case of Si nanowire MOSFET as compared to other materials. On the other hand impact of localized charges on intrinsic delay is minimum for Si nanowire MOSFET. Thus there is a trade off to decide whether low sensitivity of the device gain to localized charges is required or low sensitivity of device speed. In radio frequency circuits, the power gain of an amplifier is often more important than the voltage gain/current gain. The power gain of an electrical network is the ratio of an output power to an input power. Maximum available power gain (Gma) is a figure of merit (FOM) for the LNA design, which indicates the maximum theoretical power gain that can be expected from the device. Fig.17 reflect the performance degradation due to induced localised charges in terms of maximum available power gain (Gma). Improvement in Gma in case of negative localised charges is due to lower parasitic and higher transconductance in inversion region.

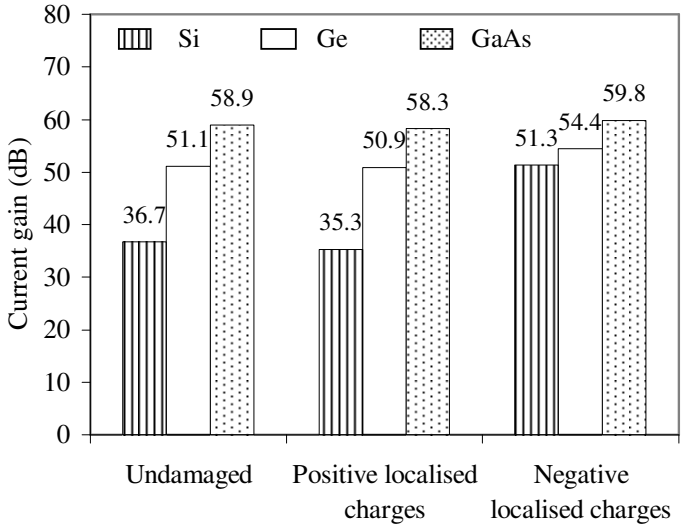

Fig.16 Impact of localized charges on current gain of the device. Other parameters are: L=70nm, t_{ox}=1.5 nm, R =15nm, N_d =1x10^{26} m^{-3}, N_a=1x$10^{21}$$m^{-3}$, L_1=L_2=L/2, V_{gs}=0.6V, V_{ds}=0.05V.

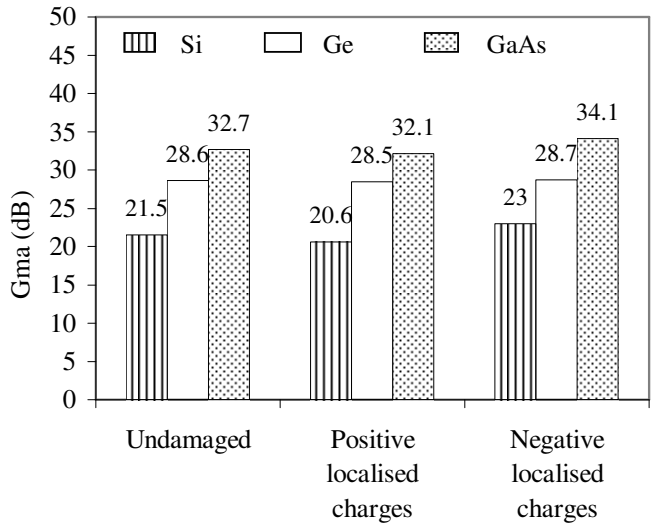

Fig.17 Impact of localized charges on Gma of the device. Other parameters are: L=70nm, t_{ox} =1.5 nm, R =15nm, N_d =1x10^{26} m^{-3}, N_a=1x$10^{21}$$m^{-3}$, L_1=L_2=L/2, V_{gs}=0.6V, V_{ds}=0.05V.

4. CONCLUSION

Impact of hot carrier induced/stress induced/process damage induced interface fixed charges has been studied for three channel materials Si, Ge and GaAs optimized to have same threshold voltage. Presence of fixed charges at semiconductor-oxide interface causes a step in the potential profile which results in the shift of threshold voltage, degradation of drain current, transconduction, intrinsic delay, current and power gain of the device. Sensitivity of the device due to variations caused by hot carrier damage/process damage/radation damage has been compared for the three materials. If low sensitivity of device gain on localized charges is required

Ge is better over Si and GaAS. On the other hand if low sensitivity of device speed on localized charges is required then Si is the choice material. However if we compare fresh device in terms of higher current driving capability, device gain, and device speed, GaAs is found to be a better material than Ge and Si and is the suitable material for high speed and high frequency applications.

ACKNOWLEDGEMENT

The Author (Rajni Gautam) is thankful to University Grants Commission (UGC), Government of India for necessary financial assistance to carry out this research work.

REFERENCES

[1] K. C Saraswat, C.O.Chui, T. Krishnamohan, A. Nayfeh, P. McIntyre, (2005) "Ge based high performance nanoscale MOSFETs", *Microelectronic Engineering*, vol. 80, pp. 15-21.

[2] D. Wang, Q. Wang, A. Javey, R. Tu, H. Dai, H. Kim, P.C. McIntyre, T. Krishnamohan, K.C. Saraswat, (2003) "Germanium nanowire field-effect transistors with SiO2 and high-k HfO2 gate dielectrics", *Applied Physics Letters*, vol. 83, pp.2432-2434.

[3] J. Y. Wu, H. H. Wang, Y. H. Wang, M.P. Houng, (2001) "GaAs MOSFET's Fabrication with a Selective Liquid Phase Oxidized Gate", *IEEE transactions on electron devices*, vol. 48, no. 4, pp.634-637.

[4] M. Passlack, R. Droopad, K. Rajagopalan, J. Abrokwah, P. Zurcher, P. Fezes, (2007) "High Mobility III-V Mosfet Technology", Cs Mantech Conference, May 14-17, Austin, Texas, USA, pp.39-42.

[5] J.P. Colinge, (2004) "Multiple-gate SOI MOSFETs", *Solid State Electronics*, vol. 48, no. 6, pp. 897-905.

[6] J. Appenzeller, J. Knoch, E. Tutuc, M. Reuter, and S. Guha, (2006) "Dual gate silicon nanowire transistors with nickel silicide contacts", *Technical Digest of IEDM*, pp. 1-4, San Francisco, CA .

[7] J. T. Sheu, S. P. Yeh, C. H. Lien, and S. T. Tsai, (2006) "Fabrication of nanoscaled-schottky diodes based on metal silicide/silicon nanowire with scanning probe lithography and Wet etching and its electrical characterization" *Japanese Journal of Applied Physics*, Vol.45 , No.4B, pp. 3686-3689 (2006).

[8] J. He, X. Zhang, G. Zhang, M. Chan, Y. Wang, (2006) "A carrier-based analytic DCIV model for long channel undoped cylindrical surrounding-gate MOSFETs", *Solid State Electronics*, vol.50, no.3, pp.416-421.

[9] B. Yu, Y. Yuan, J. Song, Y. Taur, (2009) "A Two-Dimensional Analytical Solution for Short-Channel Effects in Nanowire MOSFETs", *IEEE Transactions on Electron Devices*, vol.56, no.10, pp.2357-2362.

[10] T.K. Chiang, (2009) "A new compact subthreshold behavior model for dual-material surrounding gate (DMSG) MOSFETs.", *Solid State Electronics*, vol.53, no.5,pp.490-496.

[11] E. H. Poindexter,(1989) "MOS Interface States: Overview and physicochemical Perpective", *Semicond. Sci. Techno., vol.* 4 , pp. 961-969.

[12] L. Trabzon And O. O. Awadelkarim, (1998) "Damage to n-MOSFETs from electrical stress Relationship to processing damage and impact on device reliability", *Microelectron. Reliab.* , vol.38 , pp. 651-657.

[13] Y. H. Lho and K.Y. Kim, (2005) "Radiation Effects on the Power MOSFET for space applications", ETRI Journal, vol. 27, pp. 449-452.

[14] S. Naseh, M. J. Deen, C.-H. Chen, (2006) "Hot-carrier reliability of submicron NMOSFETs and integrated NMOS low noise amplifiers", *Microelectronics Reliability* , vol. 46, pp. 201-212.

[15] K.K. Ng , G.W. Taylor, (1983) "Effects of hot-carrier trapping in n- and p-channel MOSFET's", *IEEE Transactions on Electron Devices*, vol. ED-30, pp. 871-876.

[16] J. Bracchitta, T.L. Honan, R.L. Anderson, (1985) "Hot-electron-induced degradation in MOSFET's at 77 K", *IEEE Transactions on Electron Devices*, vol. ED-32, no. 9, pp. 1850-1857.

[17] K.R. Hofmann, C. Werner, W. Weber, G. Dorda, G. (1985) "Hot-electron and hole emission effects in short-channel MOSFET's.", IEEE Transactions on Electron Devices, vol. ED-32, no. 3, pp. 691-699.

[18] S.J. Jang, D.H. Ka, C.G. Yu, W.J. Cho, J.T. Park, (2008) "Hot-carrier effects as a function of silicon film thickness in nanometer-scale SOI pMOSFETs", *Solid State Electronics*, vol.52, no.5, pp.824-829.

[19] C.W. Lee, I. Ferain, A. Afzalian, R. Yan, N. Dehdashti, P. Razavi, J.P. Colinge, J.T. Park, (2009) "NBTI and hot-carrier effects in accumulation-mode Pi-gate pMOSFETs", in Proceedings of 20th European Symposium on the Reliability of Electron Devices, Failure Physics and Analysis, *Microelectronics Reliability*, vol.49, no. 9-11, pp.1044--1047.

[20] F. Djeffal, Z. Ghoggali, Z. Dibi, N. Lakhdar, (2009) "Analytical analysis of nanoscale multiple gate MOSFETs including effects of hot-carrier induced interface charges", *Microelectronics Reliability*, vol. 49, no. 4, pp. 377-381.

[21] T. K. Chiang (2011) "A Compact Model for Threshold Voltage of Surrounding-Gate MOSFETs With Localized Interface Trapped Charges", *IEEE Transactions On Electron Devices*, vol. 58, pp. 567-571.

[22] S. Kang, B. Choi, and B. Kim, (2003) "Linearity Analysis of CMOS for RF Application," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no.3, pp. 972–977.

[23] H. S. Bennett , R. Brederlow , J. C. Costa , P. E. Cottrell , W. M. Huang , A. A. Immorlica Jr., J. E. Mueller , M. Racanelli , H. Shichijo , C. E. Weitzel, and B. Zhao (2005) "Device and technology evolution for Si-based RF integrated circuits," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1235-1258.

[24] ATLAS User's Manual: 3-D Device Simulator, SILVACO International, Version5.14.0.R, 2010.

[25] A Tsormpatzoglou1, D H Tassis1, C A Dimitriadis1, G Ghibaudo, G Pananakakis and R Clerc, (2009) "A compact drain current model of short-channel cylindrical gate-all-around MOSFETs**",** *Semicond. Sci. Technol.* , vol.24 , pp. 1-8.

[26] J. Guo, A. Javey, H. Dai, and M. Lundstrom, (2004) "Performance analysis and design optimization of near ballistic carbonnanotube field-effect transistors", In Proceedings of IEDM, San Francisco, CA, pp.703–706.

Authors

Rajni Gautam received B.Sc. and M. Sc. Degrees in Electronics from University of Delhi, India, in 2007 and 2009, respectively. She is currently working toward the Ph.D. degree with the Department of Electronic Science, University of Delhi. Her research interests include device modeling and simulation for advanced metal oxide–semiconductor field-effect transistors (MOSFET) structures such as surrounding gate MOSFET with study of interface localized charges and analytical modeling, design, and simulation of Optically controlled MESFET/ MOSFET nanodevices.

Manoj Saxena is Assistant Professor in Department of Electronics, Deen dayal Upadhyaya College, University of Delhi, New Delhi, India. He received B.Sc. (with honors), M. Sc., and Ph.D. degrees from the University of Delhi, New Delhi, in 1998, 2000, and 2006, respectively, all in electronics. He joined Department of Electronics, Deen Dayal Upadhyaya College, University of Delhi in 2000. He is the Co-principal Investigator in research project sponsored by DRDO, Govt. of India and University Grants Commission (UGC), Govt. of India. He has authored or coauthored **119** technical papers in international

journals and various international and national conferences. He has contributed one chapter entitled MOSFET Modeling in the Encyclopedia on RF and Microwave Engineering (New York: Wiley, 2005). His current research interests are in the areas of analytical modeling, design, and simulation of Optically controlled MESFET/MOSFET, silicon-on-nothing, insulated-shallow-extension, grooved/concave-gate MOSFETs, cylindrical gate MOSFET and Tunnel FET. Dr. Saxena has reviewed extensively for IEEE TRANSACTIONS ON ELECTRON DEVICES, Semiconductor Science Technology, Solid State Electronics, Journal of Physics: D Applied Physics, Superlattices and Microstructures, Elsevier Science, UK, International Journal of Numerical Modeling: Electronic Networks, Devices and Fields, Wiley, Journal of Electrical and Electronics Engineering Research (JEEER), MAPAN-Journal of Metrology Society of India and International Journal of Science and Technology Education Research. His name appeared in the Golden List of IEEE TRANSACTIONS ON ELECTRON DEVICES Reviewers since 2005. He is also listed in the 25th Anniversary edition of Who's Who in the World. He is Member of Institute of Physics (IOP), UK and Senior Member-IEEE (USA). He is Member of National Academy of Sciences India (NASI), Allahabad, India, Institution of Engineering and Technology (IET), UK, and International Association of Engineers, Hong Kong, Life Member of Semiconductor Society of India, New Delhi, India, Life Member of Indian Science Congress Association (ISCA), Young Associate of Indian Academy of Sciences (IAS), Bangalore, India and Joint Secretary of Society for VLSI and Microelectronics, New Delhi, India and Secretary of IEEE EDS Delhi Chapter, New Delhi

R. S. Gupta (SM'81) received the B.Sc. and M.Sc. degrees from Agra University, Agra, India, in 1963 and 1966, respectively, and the Ph.D. degree in electronic engineering from the Institute of Technology, Banaras Hindu University, Varanasi, India, in 1970.

In 1971, he was with Ramjas College, University of Delhi, Delhi, India. In 1987, he was with the Department of Electronic Science, University of Delhi South Campus, New Delhi, India, as a Reader and later as a Professor from 1997 to 2008. He was CSIR Emeritus Scientist with the Semiconductor Devices Research Laboratory, Department of Electronic Science, University of Delhi till March 2009. Currently he is Professor and Head, Department of Electronics & Communication Engineering, Maharaja Agresen Institute of Technology (GGIP University, Delhi). He heads several major research projects sponsored by the Ministry of Defence, the Department of Science and Technology, the Council of Science, and the Industrial Research and University Grants Commission. In 1988, he was a Visitor with the University of Sheffield, Sheffield, U.K., under the ALIS Link exchange program and also visited several U.S. and Spanish universities in 1995 and 1999, respectively. He also visited the Czech Republic in August 2003; Korea in November 2003; Rensselaer Polytechnic Institute, Troy, NY, in August 2004; and China in December 2005. In Dec 19, 2007 he visited Rome, Italy and in 2009 he visited North Texas University and Southeast Missouri State University USA. He has authored or coauthored over 520 papers in various international and national journals and conference proceedings. He contributed the chapter entitled "MOSFET Modeling" in the *Encyclopedia on RF and Microwave Engineering* (Wiley, 2005). He has supervised 38 Ph.D. students. In addition to that he has also supervised/supervising 12 PhD students. His current interests and activities include modeling of SOI sub-micrometer MOSFETs and LDD MOSFETs, modeling and design of HEMTs, hot-carrier effects in MOSFETs, and modeling of GaAs MESFETs for high-performance microwave and millimeter-wave circuits and quantum-effect devices.

Prof. Gupta was an Executive Member of the IEEE Electron Devices Society/Microwave Theory and Techniques Society Chapter of the IEEE India Council. Prof Gupta is Life Senior Member IEEE and was Chairman of IEEE EDS Delhi Chapter. His name also appeared in the Golden List of the IEEE TRANSACTIONS ON ELECTRON DEVICES in December 1998, 2002, and 2004. He is a Fellow of the Institution of Electronics and Telecommunication Engineers (India), a Life Member of the Indian Chapter of the International Centre for Theoretical Physics, and a Life Member of the Semiconductor Society of India and chairman of society for microelectronics and VLSI. He was the Secretary of ISRAMT'93 and the 1996 Asia–Pacific Microwave Conference (APMC'96), and the Chairman of the Technical Programme Committee of APMC'96. He edited the proceedings of both of these international conferences. He was the Chairman of APMC'2004 held in New Delhi in December 2004. He has been listed in *Who's Who in the World*. Prof Gupta was chairman of 12TH ISMOT 2009 held in Dec 2009 in India.

Mridula Gupta (SM'09) received the B.Sc. degree in physics, the M.Sc. degree in electronics, the M.Tech. degree in microwave electronics, and the Ph.D. degree in optoelectronics from the University of Delhi, Delhi, India, in 1984, 1986, 1988, and 1998, respectively.

Since 1989, she has been with the Department of Electronic Science, University of Delhi South Campus, New Delhi, India, where she was previously a Lecturer and is currently an Associate Professor and with the Semiconductor Devices Research Laboratory. She has authored or coauthored approximately 235 publications in international and national journals and conference proceedings. She has supervised 14 Ph.D. students. She contributed the chapter entitled "MOSFET Modeling" in the *Encyclopedia on RF and Microwave Engineering* (Wiley, 2005). Her current research interests include modeling and simulation of MOSFETs, MESFETs, and HEMTs for microwave-frequency applications.

Dr. Gupta is a Fellow of the Institution of Electronics and Telecommunication Engineers (India) and a Life Member of the Semiconductor Society of India. She is the Chairperson of IEEE EDS Delhi Chapter. She was the Secretary of the 2004 Asia–Pacific Microwave Conference, New Delhi, held in December 2004. Dr. Gupta was General Secretary of 12th ISMOT 2009 held in Dec 2009 in India.