An Analytical Model for Fringing Capacitance in Double gate Hetero Tunnel FET and Analysis of effect of Traps and Oxide charges on Fringing Capacitance

Brinda Bhowmick[1] and Srimanta Baishya[2]

[1]Department of Electronics and Communication Engineering, National Institute of Technology Silchar, Silchar, India
brinda_bh@yahoo.co.in
[2]Department of Electronics and Communication Engineering, National Institute of Technology Silchar, Silchar, India
baishya_s@rediffmail.com

ABSTRACT

In this paper fringe capacitance of double hetero gate Tunnel FET has been studied. The physical model for fringe capacitance is derived considering source gate overlap and gate drain non overlap. Inerface trap charge and oxide charges are also introduced under positive bias stress and hot carrier stress and their effect on fringe capacitance is also studied. The fringe capacitance is significant speed limiter in Double gate technology. The model is tested by comparing with simulation results obtained from Sentauras TCAD simulations.

KEYWORDS

Band-to-band tunnelling, hetero-gate, parasitic fringe capacitance.

1. INTRODUCTION

As MOSFETs are scaled to nanometer dimensions, various short channel effects such as DIBL, V_T roll-off, sub 60mV/decade subthreshold swing etc are coming into picture. Subthreshold swing can not be scaled and hence off state characteristics will be degraded [1]. To overcome short channel effects, one needs to design a device which uses other mode of carrier transport so that a lower subthreshold swing can be achieved. The other modes are based on impact ionization [2] and interband tunneling [3]. Sub 60mV/decade value of subthreshold swing is possible for these two modes of carrier transport [4]. The impact ionization MOSFET appeared to be very promising due to its near ideal switching characteristics [5]. But problems like threshold voltage shift caused by hot carrier injection, non-rail to rail voltage swings, and high operating voltage requirements will arise in Impact ionization MOSFETS [2]. However, devices based on these mechanisms fail to meet the ITRS requirements [6].

Here a hetero gate tunnel FET based on band-to-band tunneling is considered for which a good trade off between SCEs , parasitic fringe capacitance, and parasitic series resistance is achieved [7]-[8] . The fringe capacitance (C_f) for this device includes the inner and outer components. Unlike MOSFET, tunnel FET has asymmetrical source and drain [8]. The gate is extended over the source but gate on the drain side is shorten. This is due to increase the gate coupling i.e to increase the control of gate over the source channel junction. Models for C_{if} and C_{of} for the double MOSFETS are already defined [9]. In nano scale DG MOSFETS the models are defined

DOI : 10.5121/vlsic.2012.3101

considering weak inversion and strong inversion of channel [10]. Since tunnel FET operation is completely different from MOSFET, the derivations for inner and outer fringe capacitance is also different. For the first time, the inner and outer components of parasitic fringe capacitance is modelled for tunnel FET. The model is verified by comparing with simulated data for varying silicon layer thickness, oxide thickness, drain voltage, and gate voltage.

In this paper, we report first time the effect of positive bias stress and hot carrier stress on the fringe capacitor of double hetero gate tunnel FET. To simulate this, interface traps (Q_{IT}) and oxide charges (Q_{OT}) are introduced with various distributions. The oxide charge is dominant in case of hot carrier stress and the interface traps are dominant in case of positive bias stress [11].

2. Device structure and parasitic capacitances

The device is a heterogate dielectric double gate device as shown in Figure. 1. It can operate both in n and p channel modes . In p mode, $V_{gs} < V_A$ and in n mode, $V_{gs} > V_A$, where V_A is a reference voltage required to align the P^+ valence band and channel conduction band. In n-channel mode, tunneling occurs in the source side while in p-channel mode, tunneling occurs in the drain side. An electron inversion layer is created in the channel at the interface with the gate dielectric when a gate voltage greater V_F is applied. Tunneling takes place from the source valence band to the conduction band in the inversion layer of the channel [3]. As mentioned, we have used heterogate dielectric. A low-K gate oxide (SiO_2 with dielectric constant 3.9) at the drain side and high-K oxide (HfO_2 with dielectric constant 25) at the tunneling junction are used. To reduce the ambipolar current at the drain side, low-K gate oxide is used. The EOT of high-K gate oxide is less so it increases the control over the tunneling junction and here tunneling takes place between source and channel [12]. The on current of the device is of the order of mA range and off current is in pico amp range. This agrees with ITRS requirement. The fringe capacitance effect is studied to investigate its effect on drain current. Also, the effect of trap and oxide charges are observed on the fringe capacitance model.

The fringe capacitance (C_f) of double heterogate tunnel FET includes inner (C_{if}) and outer components (C_{of}) as shown in Figure. 1. There is a choice to be made between attaining the best characteristics possible by finding the precise alignment of the gate that produces the thin tunnel barrier at on-state, and stabilizing characteristics by overlapping the gate to the source region. There is no gate drain overlapping .Hence, the fringe capacitance at the source side is assumed to be dominant compare to the drain side. In the Fig. 2, the fringe capacitance of only one gate is shown. The other gate is also symmetric about X direction and having the similar fringing effect.

This paper is organized as follows – first the inner and outer fringe capacitances are modelled. Next the influence of variation of t_{si} ,t_{ox} on fringe capacitance model is compared with simulated data. The effect of fringe capacitance on the total gate capacitance is also observed. The trap and oxide charges are introduced and their effect on fringe capacitance is analyzed.

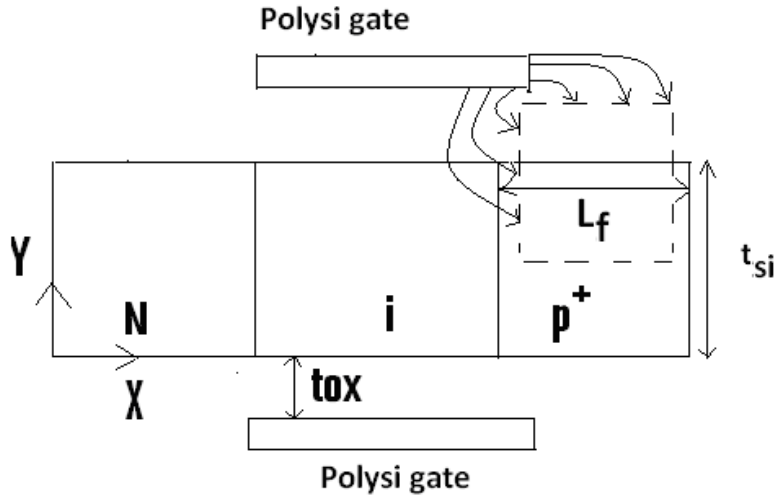

Figure 1. Hetero double gate dielectric tunnel FET with fringe capacitance components.

3. PHYSICAL MODEL

3.1. Model of C_{of}

Assume outer fringing field is Y directional. Dotted line is showing Gaussian surface. t_{ox} is the oxide thickness, t_{si} is body layer thickness.

$$Q_{of} = 2\varepsilon_{si} E_y(x,y) L_f \quad (1)$$

$$E_y = a_1(x) + 2a_2(x)y \quad (2)$$

$$\psi(x,0) = \psi_s(x)$$

$$\frac{d\psi(x,t_{si})}{dy} = -\frac{\varepsilon_{ox}\{\psi_s(x) - v\}}{\varepsilon_{si} t_{ox}} \quad (3)$$

$$\frac{d\psi(x,0)}{dy} = \frac{\varepsilon_{ox}\{\psi_s(x) - v\}}{\varepsilon_{si} t_{ox}}$$

the coefficients $a_1(x)$, and $a_2(x)$ are determined from this solution under the boundary conditions for potentials are given in (3).

$\psi_s(x)$ is the surface potential, v is the difference of V_{GS} *and* V_{FB}.

$$C_{of} = 2\varepsilon_{si} L_f \frac{dE_y(x,y)}{dV_{GS}} \quad (4)$$

Using (2) and (3) we get,

$$C_{of} = -2L_f \frac{\varepsilon_{ox}}{t_{ox}}\left(1 - \frac{2y}{t_{si}}\right) \quad (5)$$

3.2. Model of C_{if}

Inner fringing field is assumed to be X directional as shown in Figure.1. Applying Gauss's law we get,

$$Q_{if} = -2\frac{\varepsilon_{si} E_x(0,y) \mathrm{t_{si}}}{2} - 2\varepsilon_{si} E_y(x,0) L_f \quad (6)$$

The second term is very small compare to the first term.

$$E_x = \frac{d\psi_s(x)}{dx} + \frac{\varepsilon_{ox}\left\{\frac{d\psi_s(x)}{dx} - \upsilon\right\}}{\varepsilon_{si}\ t_{ox}} y - \frac{1}{2}\frac{\varepsilon_{ox}\left\{\frac{d\psi_s(x)}{dx} - \upsilon\right\}}{\varepsilon_{si}\ t_{ox}\ t_{si}} y^2 \quad (7)$$

$$C_{if} = \varepsilon_{si} t_{si} \frac{dE_x(0,y)}{dV_{GS}} \quad (8)$$

$$\frac{dE_x(0,y)}{dV_{GS}} = -\frac{\varepsilon_{ox}}{\varepsilon_{si} t_{ox}} \mathrm{y} + \frac{1}{2}\ \frac{\varepsilon_{ox}}{\varepsilon_{si} t_{ox} t_{si}} \mathrm{y}^2 \quad (9)$$

3.3 Model of fringe capacitance considering interface traps and oxide charges

To study the reliability performance of double gate tunnel FET, we simulate the fringe capacitance considering various traps and oxide charges. Any traps and/or charge near the tunnelling junction will modify the tunnelling field [13].

Considering above equations we can modify the fringe capacitance by modifying the $\frac{dE}{dV_{gs}}$.

$$\frac{dE_x(0,y)}{dV_{GS}} = -\frac{\varepsilon_{ox}}{\varepsilon_{si} t_{ox}} \mathrm{y} + \frac{1}{2}\ \frac{\varepsilon_{ox}}{\varepsilon_{si} t_{ox} t_{si}} \mathrm{y}^2 - \frac{dV_{FB}}{dV_{GS}}\left(-\frac{\varepsilon_{ox}}{\varepsilon_{si} t_{ox}} \mathrm{y} + \frac{1}{2}\ \frac{\varepsilon_{ox}}{\varepsilon_{si} t_{ox} t_{si}} \mathrm{y}^2\right) \quad (10)$$

$$\frac{dE_y(x,y)}{dV_{GS}} = -\frac{\varepsilon_{ox}}{\varepsilon_{si} t_{ox}}\left(1 - \frac{2y}{t_{si}}\right) + \frac{dV_{FB}}{dV_{GS}} \frac{\varepsilon_{ox}}{\varepsilon_{si} t_{ox}}\left(1 - \frac{2y}{t_{si}}\right)$$

$$\frac{dV_{FB}}{dV_{GS}} = -\frac{1}{C_o}\left(\frac{\frac{dE}{dV_{GS}}}{\frac{dE}{dQ_{OT}}} + \frac{\frac{dE}{dV_{GS}}}{\frac{dE}{dQ_{IT}}}\right) \quad (11)$$

where C_o is the oxide capacitance.

It is already established that both the factor in (11) are nearly independent on V_G, leading to parallel shift .A small modification in E may cause a large change in the tunneling current Id. In order to keep a constant I_D, the gate voltage V_G should be modified [11]. The change in gate voltage induced by interface generation and by oxide charge to keep the drain current constant is given by

$$\Delta V_{GS \text{ at } \Delta ID=0} = -\left[\frac{\frac{dE}{dQ_{IT}}}{\frac{dE}{dV_G}}\right] \frac{dQ_{IT}}{dN_{IT}} \Delta N_{IT} \quad (12)$$

$$\Delta V_{GS \text{ at } \Delta ID=0} = -\left[\frac{\frac{dE}{dQ_{oT}}}{\frac{dE}{dV_G}}\right] \Delta Q_{oT} \quad (13)$$

$\frac{dQ_{IT}}{dN_{IT}}$ is the charge filling factor of traps.

Both the factors in [ ] are nearly independent on V_{GS} . The variation in flat band voltage with respect to gate voltage can be obtained by using (12) and (13).

3. Result and Discussions

In this paper simulation is done using Synopsys TCAD tools. Band gap narrowing is activated. The device is a hetero gate dielectric double gate Tunnel FET for which fringing capacitance is considered only at the source side since there is no gate drain overlap. In Figure. 2, the variation of body layer thickness on external fringe capacitance is observed. With the increasing t_{si}, C_{of} increases. C_{if} is also increases with t_{si}. The model and the simulated data shows good agreement. But for increasing t_{si} , model becomes less accurate. This is because of neglecting the second term in (6). The fringe capacitance components are decreasing with the increase of oxide thickness. Hence there is a trade off between oxide thickness and the silicon body layer thickness. Therefore optimized value of silicon layer thickness 15 nm to 20 nm and for tox, the optimized value should lie in-between 2.5 nm to 3 nm to get minimum fringe capacitance C_f. The effect of fringe capacitance on the total gate capacitance is shown in Figure. 6. The effect of oxide and trap charge on capacitance voltage characteristic including fringe capacitance is also analyzed and it is observed that C_f is a significant speed limiter in double gate technology [14]-[15]. Therefore, C_f should be minimized. Using the results of the derived model and simulation shows that the t_{ox}, t_{si} should be optimized.

Here the effect of trap charges and oxide charges are also studied. To realize the effects , we simlulate the electric field under the positive bias stress (V_G = 3.5V, V_S = V_D = 0) and hot carrier stress (V_G=V_D=3.5V, Vs=0). In Figure. 7, I_D-V_{GS} characteristics considering Positve bias stress and hot carrier stress (HC) is compared.

The variation of Ey and Ex along the channel are shown in Figure.8 and Figure. 9 under positive bias stress and HC stress.The peak in the y component of electric field in the source channel junction leading to the fact that P+ doping of source which gives rise to more negative V_{FB} in the source gate overlapping region compared to channel gate region [16]-[18]. Ex peak is also in the source channel junction. Hence Ey peak will induce large interface traps and tunneling charge in the tunneling path and oxide charge is more likely generated under HC stress [11]. Considering the effects of interface traps and oxide charges, the model of fringe capacitance in (5) and (8) are modified. This modified model includes the

$\frac{dV_{FB}}{dV_{GS}}$ term. The flat band voltage is a function of interface and oxide charges. In Figure. 10, the variation of inner and outer fringe capacitance considering interface trap and oxide charges with the silicon layer thickness is shown. The effect of trap and oxide charge on inner fringe capacitance is almost same. But in case of outer fringe capacitor, the effect of interface trap charge is more compare to oxide charge because Ex exhibits higher value under HC stress.

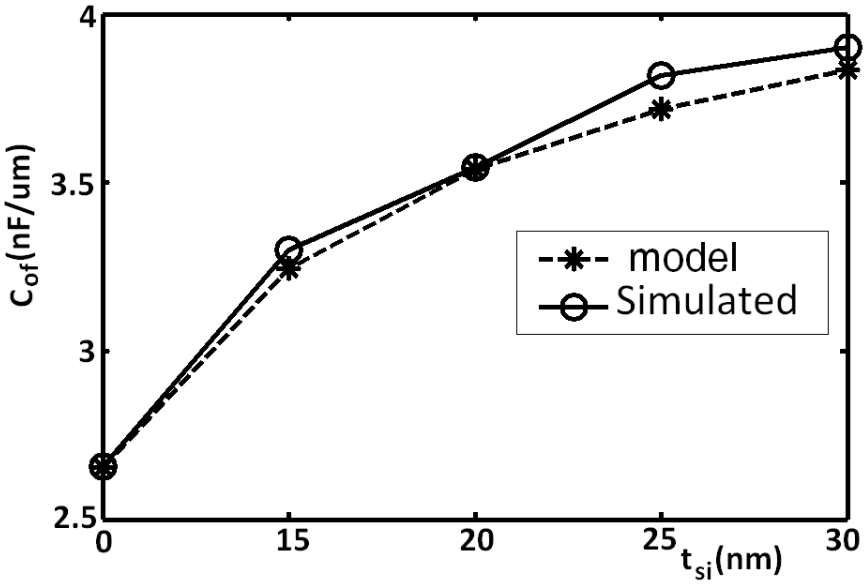

Figure. 2 Outer fringing capacitance increases with body layer thickness.

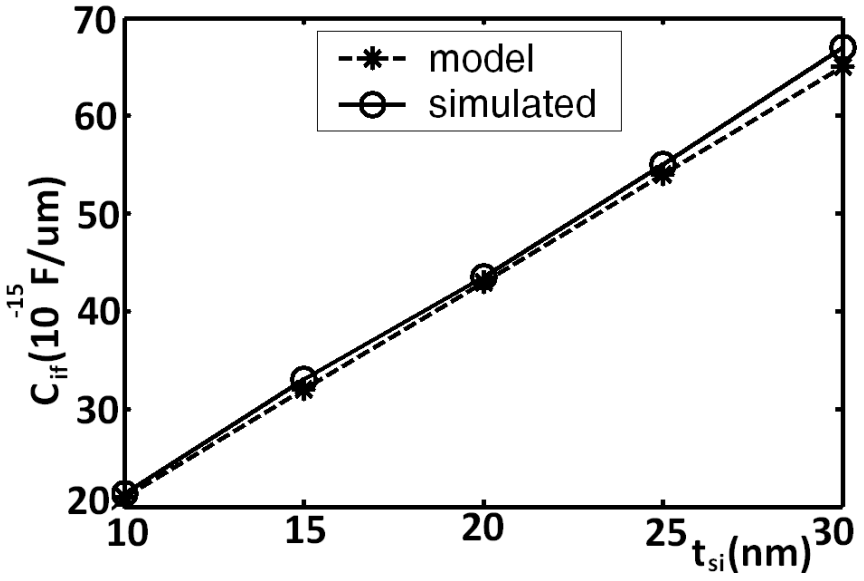

Figure. 3 Inner fringing capacitance for model and simulated data are plotted for various t_{si}

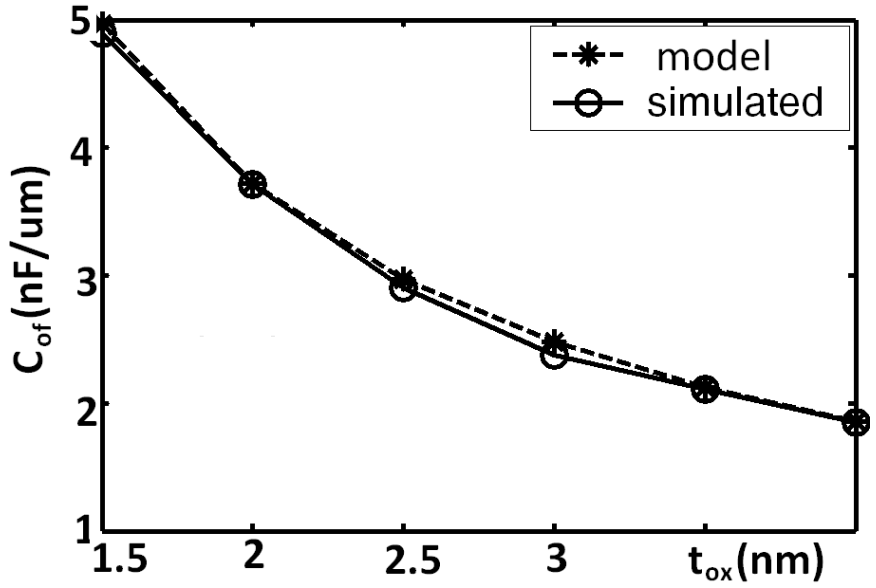

Figure. 4 Outer fringe capacitance decreases with increase in oxide thickness.

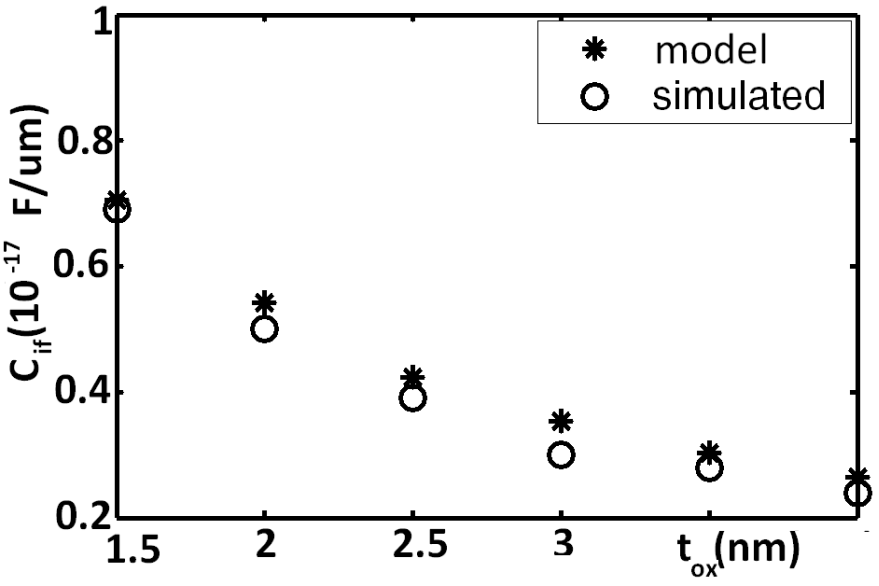

Figure . 5 There is close match between the model and simulated values.

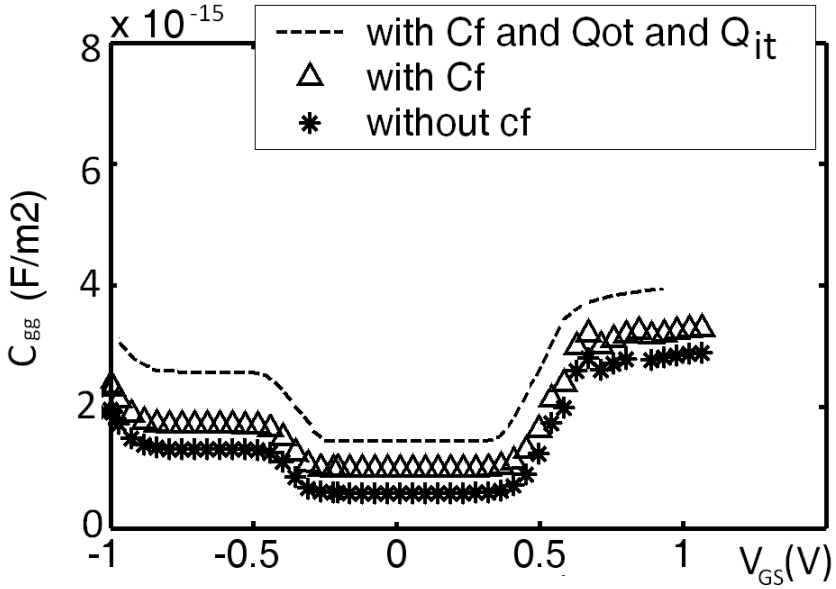

Figure. 6 Capacitance voltage characteristic

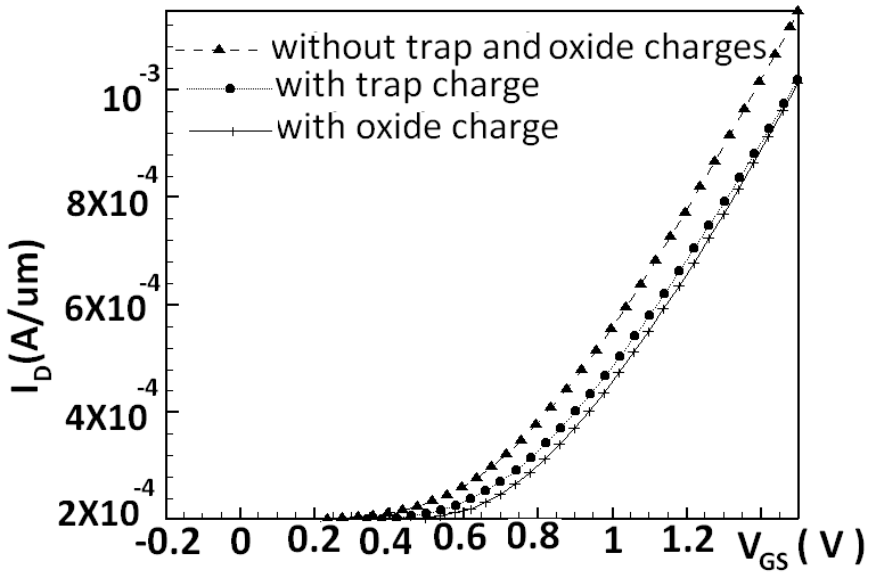

Figure. 7 Effect of interface trap and oxide charge on the degradation of drain current at VDS=1V.. The I_D degradation is mainly induced by interface traps and oxide charges within 10 nm range above the tunneling region along the X-direction .

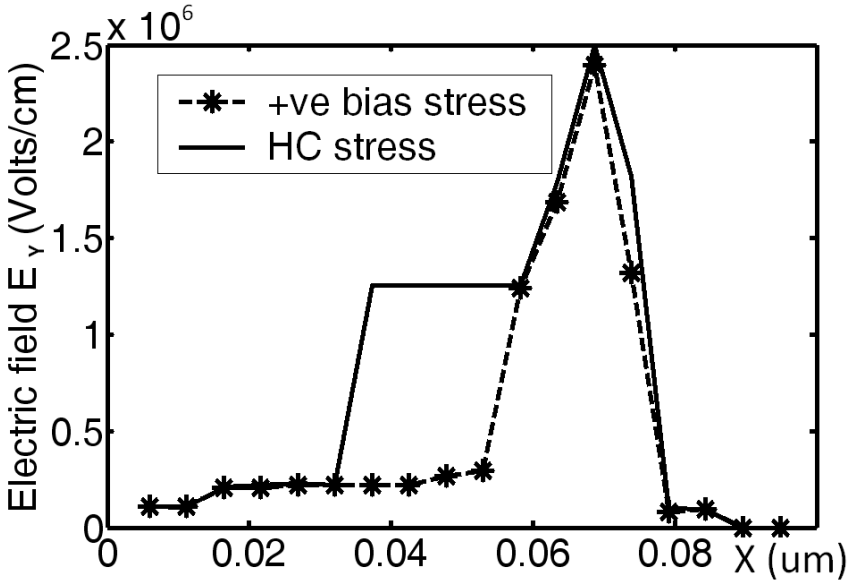

Figure. 8 The tunnel junction is x =70nm.

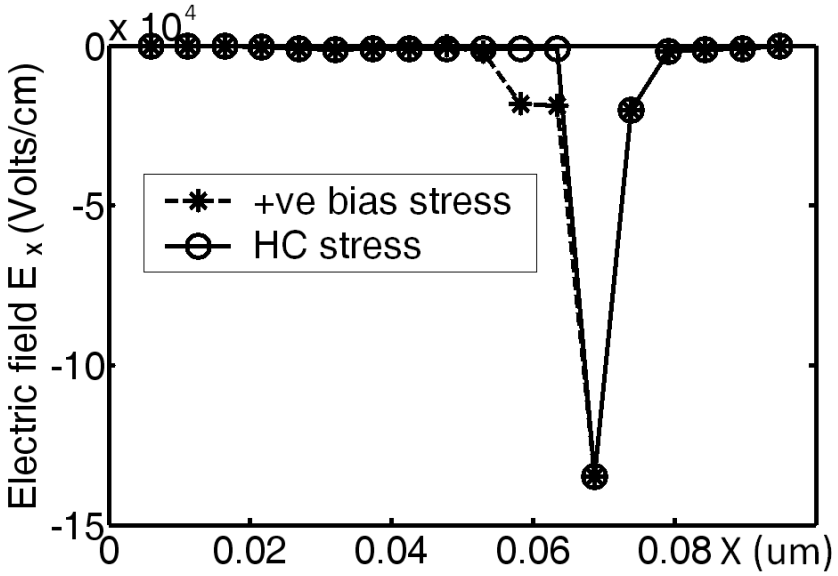

Figure. 9 E_X peak is located near the source channel junction which may induce impact ionization.

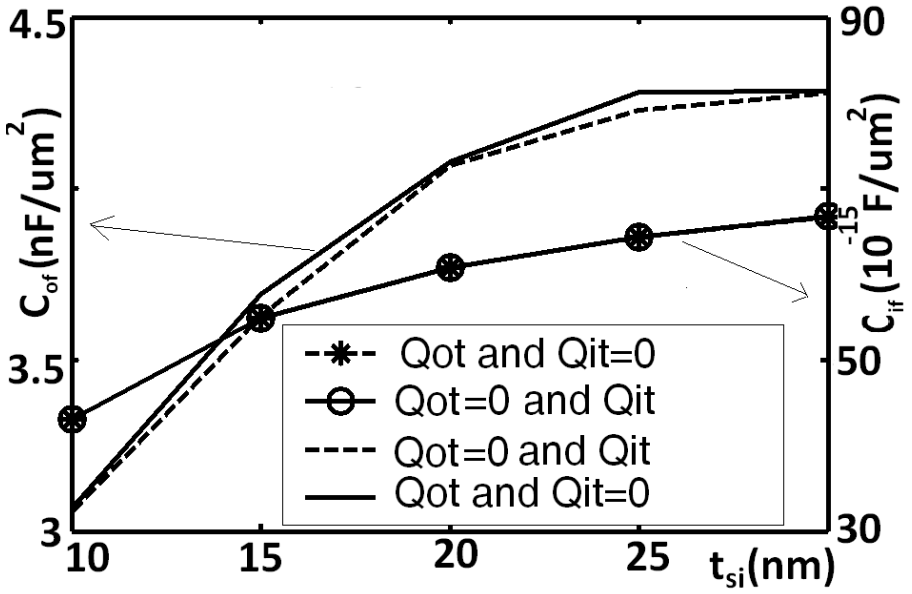

Figure. 10

4. CONCLUSIONS

In this paper, the degradation in the drain current due to interface trap and/or oxide charges is investigated. For the first time the inner and outer fringe capacitance of a hetero double gate dielectric is modelled and optimized considering the variation of silicon layer thickness and oxide thickness. It is found that optimised value of silicon body thickness is 15 to 20 nm and the same for gate oxide is 2.5 to 3 nm. Also, the effect of trap and oxide charge is analyzed on inner and outer fringe capacitance model and shows degradation in drain current as well as capacitance voltage characteristics. The results obtained could be useful while considering for the reliability issues.

ACKNOWLEDGEMENTS

This work was supported by ALL INDIA COUNCIL FOR TECHNICAL EDUCATION (AICTE), under Grant 8023/BOR/RID/RPS-253/2008-09.

REFERENCES

[1] E. P. Vanndamme, P. Janson, and L. Deferen, "Modelling the subthresholdswing in MOSFETS", IEEE Electron Device Letters. vol. 18, no.8, pp .369-371, Aug. 1997.

[2] K. Gopalakrishnan, K. Woo, R.Jungemann, C.Graffin, P.B.Plummer, "Impact ionization MOS-IMOS-part-III,experimental results", IEEE Electron Device letters, vol.52, pp.77-84, Jan.2005.

[3] J. Appenzeller, Y.-M. Lin, J. Knoch, P. Avouris, " Band-to-band tunneling in carbon Nanotube fiel-effect transistors", Phys. Rev.Lett.93 (19), 196805-1—196805-4, 2005.

[4] K. Bhuwalka, S. Sedlmaier, A. Ludsteck, C.Tolksdorf, J. Schulze, I.Eisele, "Vertical tunnel field effect transistor", IEEE Trans. Electron Devices, vol. 51, pp. 279-282, 2004.

[5] K. Gopalakrishnan, P. Griffin, J. Plummer, I-MOS: a novel semiconductor device with subthreshold slope lower than kT/q in IEDM Technical Digest , pp.289-292, 2002.

[6] Semiconductor Industry Association (SIA), International Technology Roadmap for Semiconductors (ITRS),2009 available www.itrs..net online.

[7] S. Agarwal , J G. Fossum, " A physical Model for Fringe Capacitance in Double –Gate MOSFET With Non-Abrupt Source/Drain Junctions and Gate Underlap", IEEE Trans. Electron Devices, vol.57, no.5, pp.1069-1075, may 2010.

[8] C. Aydin, A. Zaslavsky, S. Luryi, S. Cristoloveanu, D Mariolle, D. Fraboulet ,and S. Deleoniibus, "Lateral interband tunneling Transistor in silicon-on-insulator", Appl. Phys. Lett.,vol. 84 (10) , pp. 1780-82,2004.

[9] A.S. Roy, C.CEnz, and J.M. Sallese, "Compact modelling of gate sidewall capacitance of DGMOSFET," IEEE Trans. Electron Devices, vol. 53, no.10, pp. 2655-2657, Oct.2006.

[10] W. Reddick, G. Amartunga, "Silicon surface tunnel transistor", Appl. Phys. Lett. 67 , no. 4, pp.494-496, Jul. 1995.

[11] X.Y. huang, G.F. Jiao, W.Cao, D.Huang, H.Y. Yu, Z.X. Chen, N.Singh, G.Q.Lo, D.L. Kwong And Ming-Fu Li, " Effect of Interface Traps and oxide Charge on Drain Current Degradation In Tunneling Field-Effect Transistors", IEEE Trans. Electron Device.

[12] Woo Young Choi, Woojun Lee, " Heterogate Dielectric tunneling Field effect Transistors', IEEE Transaction on Electron Devices, vol. 57(9), pp. 2317-2319, Sept.2010.

[13] G. F. Jiao, Z. X. Chen, H. Y. Yu, X. Y. Huang, D. M. Huang, N. Singh, G. Q. Lo, D.-L. Kwong,and Ming-Fu Li , "Experimental Studies of Reliability Issues in Tunneling Field-Effect Transistors", IEEE Electron Device Letters, vol. 31, no. 5, May2010.

[14] S.-H.Kim, J.G. fossum, and J. Yang, " Modeling and significance of fringe capacitance in nonclassical CMOS devices with gate-source/drain underlap. "

[15] Collinge JP. 2008. Silicon on insulator Technology: Materials to VLSI, 3rd ed, SPRINGER.

[16] A. E. Islam, H. Kufluoglu, D. Varghese, S. Mahapatra, and M. A. Alam,"Recent issues in negative-bias temperature instability: Initial degradation field dependence of interface trap generation, hole trapping effects, and relaxation," IEEE Trans. Electron Devices, vol. 54, no. 9, pp. 2143–2154, Sep. 2007.

[17] Z. X. Chen, H. Y. Yu, N. Singh, N. S. Shen, R. D. Sayanthan, G. Q. Lo,and D.-L. Kwong,"Demonstration of tunneling FETs based on highly scalable vertical silicon nanowires," IEEE Electron Device Lett., vol. 30 ,no. 7, pp. 754–756, Jul. 2009.

[18] T. Krishnamohan, D. Kim, S. Raghunathan, and K. Saraswat, "Double gate strained-Ge Hetero structure tunneling FET (TFET) with record high drive currents and < 60 mV/decsubthreshold slope," in IEDM Tech. Dig.,2008, pp. 947–949.

Authors

Brinda Bhowmick is an Assistant Prof. in Electronics and Communication Engineering Deptt. NIT Silchar, Deemed university, ASSAM, India. She is doing research in semiconductor device modelling.

Dr. Srimanta Baishya is a Professor of ECE Deptt. NIT Silchar, Deemed university, ASSAM, India. He is a member of IEEE. His research interest includes semiconductor device modelling, process integration and technology development. He has more than thirty International conference and Journal papers.