LEAKAGE POWER REDUCTION AND ANALYSIS OF CMOS SEQUENTIAL CIRCUITS

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ABSTRACT

A significant portion of the total power consumption in high performance digital circuits in deep sub-micron regime is mainly due to leakage power. Leakage is the only source of power consumption in an idle circuit. Therefore it is important to reduce leakage power in portable systems. In this paper two techniques such as transistor stacking and self-adjustable voltage level circuit for reducing leakage power in sequential circuits are proposed. This work analyses the power and delay of three different types of D flip-flops using pass transistors, transmission gates and gate diffusion input gates. . All the circuits are simulated with and without the application of leakage reduction techniques. Simulation results show that the proposed pass transistor based D flip-flop using self-adjustable voltage level circuit has the least leakage power dissipation of 9.13nW with a delay of 77 nS. The circuits are simulated with MOSFET models of level 54 using HSPICE in 90 nm process technology.

KEYWORDS

Leakage Power, Pass Transistors, Process Technology, Stacking Effect, Transmission Gates

1. INTRODUCTION

The rapid growth in semiconductor device industry has led to the development of high performance potable systems with enhanced reliability. In such portable applications, it is extremely important to minimize current consumption due to the limited availability of battery power [1]. Consequently, power dissipation is becoming recognized as a top priority issue for VLSI circuit design. Leakage power makes up to 50% of the total power consumption in today's high performance microprocessors [2]. Therefore leakage power reduction becomes the key to a low power design. Leakage power dissipation is the power dissipated by the circuit when it is in sleep mode or standby mode. Leakage power is given by equation 1 [3] and the propagation delay (T_{pd}) of a circuit is given by equation 2.

$$P_{leak} = I_{leak} * V_{dd} \quad (1)$$

$$T_{pd} \ \alpha V_{dd} / (V_{dd}-V_{th})^2 \quad (2)$$

Where I_{leak} is the leakage current that flows in a transistor when it is in off state, V_{dd} is the supply voltage, V_{th} is the threshold voltage of the transistor. This power dominates dynamic power especially in deep submicron circuits and also in circuits that remains in idle mode for a long time such as cell phones. Therefore in this paper the focus is on the reduction of leakage power dissipation .The leakage current consists of various components, such as sub-threshold leakage, gate leakage, reverse-biased junction leakage, gate-induced drain leakage [4]. Among these, sub-

DOI : 10.5121/vlsic.2012.3102

threshold leakage and gate-leakage are dominant. The sub-threshold leakage current of a MOS device can be modeled as follows [3]:

$$I_{subth} = I_0 \exp [(V_{gs}-V_t) / (n V_T)] [1- \exp (-V_{ds}/V_T)] \quad (3)$$

$$\text{And} \quad I_0 = \mu_{eff} C_{ox} (W/L)V_T^2 \quad (4)$$

Where μ_{eff} is the electron/hole mobility, C_{ox} is the gate capacitance per unit area, W and L are width and length of the channel respectively, V_t is the threshold voltage, n is the sub-threshold swing co-efficient, V_T is the thermal voltage, V_{gs} is the transistor gate to source voltage and V_{ds} is the drain to source voltage. This paper is organized as follows: Section 2 gives the related work in the area of flip-flop design. In section 3 we present three different designs of D flip-flops using pass transistors, transmission gates and Gate-Diffusion Input (GDI) gates. Section 4 describes two leakage reduction techniques such as transistor stacking and self-adjustable voltage level circuit that are applied to the above designs. Section 5 presents the simulation results of the flip-flops with and without the leakage reduction techniques and section 6 gives the conclusion.

2. RELATED WORK

Flip flops are critical timing elements in digital circuits and have a large effect on speed and power consumption of the digital circuits. Intensive research is going on in the field of low power, high speed flip flops. In [5] Jaehyun et.al proposes a mixed- Vt flip-flop with reduced leakage which has a small increase in either setup time or clock-to-Q delay. In [6] Weiqiang presents a reduction technique of leakage consumption for adiabatic sequential circuits based on two-phase complementary pass-transistor adiabatic logic using power gating scheme. A combined dual voltage assignment technique with intended clock skew scheduling is presented by Meng Tie et.al in [7]. In this work first a leakage weight based clock skew scheduling algorithm is proposed to enlarge the leakage power optimization potential. Then a dual-threshold voltage assignment algorithm is implemented to minimize leakage power. In [8] Jin Tao Jiang et.al investigates gate leakage reduction of the pass-transistor adiabatic logic with pull-up configuration circuits. In [9] Hamid et.al proposes a conventional data-retention scheme which uses a balloon latch applied to a transmission gate flip-flop. In this the balloon latch and some switches which are not in the critical paths use high threshold voltage transistors to reduce their leakage power. This scheme requires extra data-preserving balloon latches and complicated timing for transferring data back and forth between balloon latches and flip-flops on any transition from power down to active mode and vice versa. In [10] David Levacq designed an ultra low power flip-flop using two ultra-low leakage diodes and analysis of master slave latches and flip-flops is discussed in [11]. In [12] Linfeng et.al proposes a new transmission gate flip-flop based on dual threshold CMOS technique to reduce it's leakage power. In this low threshold transistors are assigned to critical paths of the circuits to enhance the performance, while high threshold transistors are assigned to non-critical paths to reduce the leakage current.. In [13] Morgenstein et.al describes the implementation of D flip –flop using GDI technique. The analysis of single edge triggered flip flops is presented by D. Markovic et.al in [14] and Nedovic et.al in [15] describes the design of dual edge triggered flip-flops. Sagi Fisher et.al in [16] proposes two architectures for implementing flip-flop cells by integrating a GDI multiplexer in their design. A dynamic forward bias technique is proposed in [17] by Hailong Jiao et.al, which alleviate the ground bouncing noise in sequential MTCMOS circuits without sacrificing the data retention capability. In [18] Jianping Hu et.al presents new low leakage power flip-flops with power-gating scheme for ultra-low power systems. The proposed flip-flops are realized based on CMOS ratioed latches with the master-slave structure. Dual-threshold CMOS (DTCMOS) and channel length biasing techniques are used for the flip-flops with power-gating scheme to reduce leakage power dissipations. Jatin N. Mistry et.al presents a new technique called sub-clock power gating, for reducing leakage power in digital

circuits in [19]. The proposed technique works concurrently with voltage and frequency scaling and power reduction is achieved by power gating within the clock cycle during active mode unlike traditional power gating which is applied during idle mode. In [20] Weiqiang Zhang et.al proposes improved effective charge recovery logic flip-flops with reduced leakage power.

3. CMOS IMPLEMENTATION OF D FLIP FLOPS

The wide use of sequential logic and memory storage systems in modern electronics results in the implementation of low power and high speed design of basic memory elements. One of the most important basic memory element is the D flip-flop (DFF). Three different designs of D flip-flops in CMOS logic are presented in this section. The D flip-flop combines a pair of master and slave D latch. Design –I uses pass transistors (PT) and inverters for the master-slave latches [21] as shown in Fig. 1. The two chained inverters are in memory state when the PMOS loop transistor is on, that is when clk = 0.Other two chain inverters on the right hand side acts in the opposite way. The flip-flop changes its state during the falling edge of the clock. Fig 2 shows the design – II that uses transmission gates (TG) and inverters [21]. At the negative edge of the clock, transmission gates T1 and T4 are ON and transmission gates T2 and T3 are OFF. During this time the slave maintains a loop through two inverters P3, P4 and T4. Now the previous triggered value from Din is stored in the slave. At the same time master latches next state but as T3 is OFF it is not passed to slave. At the positive clock edge T2 and T3 are turned ON and the new latched value passes to slave through the loop of two inverters P1, P2 and T2.

Fig. 3 shows design –III with master-slave connection of two GDI D-latches [13]. In this the body gates are responsible for the state of the circuit. These gates are controlled by the clock (clk) signal and create two alternative paths. One for transparent state of the latch ,when the clk is low and the signals are propagating through PMOS transistors .The other one is for the holding state of the latch ,when the clk signal is high and internal values are maintained due to conduction of the NMOS transistors. The inverters are responsible for maintaining the complementary values of the internal signals and the circuit outputs.

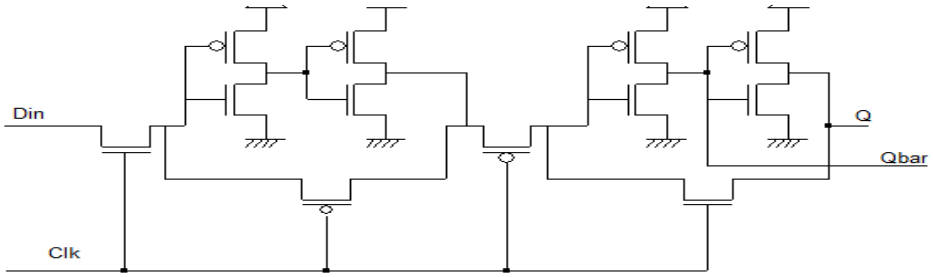


Figure 1. D flip-flop using pass transistors

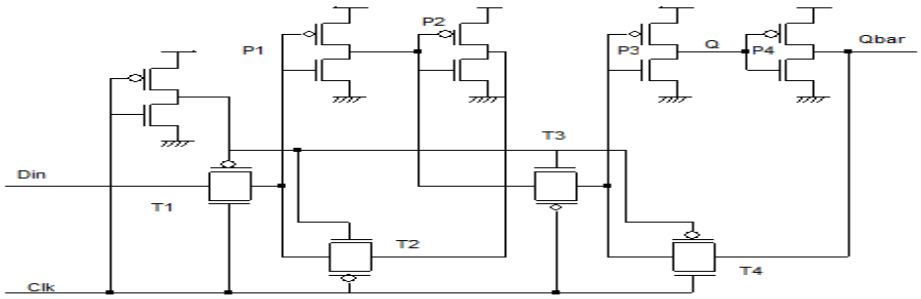


Figure 2. D flip-flop using transmission gates

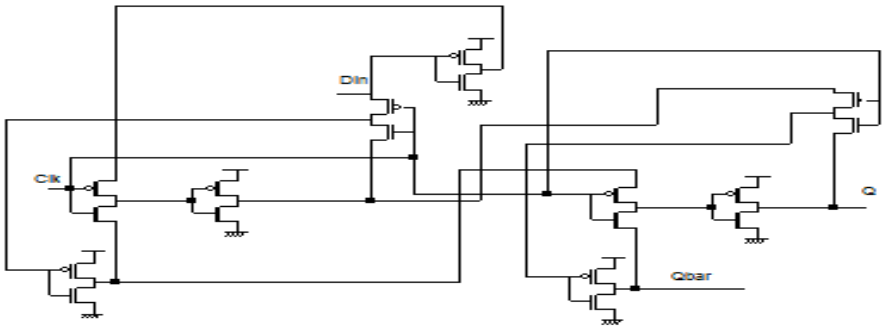


Figure 3. D flip-flop using GDI gates

4. PROPOSED LEAKAGE REDUCTION TECHNIQUES

In this section two leakage reduction techniques namely transistor stacking and self-adjustable voltage level circuit that are applied to the above circuits are described.

4.1. Leakage current control using transistor stack

The leakage current flowing through a stack of series connected transistors reduces when more than one transistor of the stack is turned OFF. This effect is known as the "Stacking Effect" [22]. When two or more transistors that are switched OFF are stacked on top of each other [Refer Fig. 4a], then they dissipate less leakage power than a single transistor that is turned OFF [Refer Fig. 4b]. This is because each transistor in the stack induces a slight reverse bias between the gate and source of the transistor right below it, and this increases the threshold voltage of the bottom transistor making it more resistant to leakage. Therefore in Fig. 4a transistor T2 leaks less current than transistor T1 and T3 leaks less than T2. Hence the total leakage current through the transistors T1, T2 and T3 is decreased as it flows from V_{dd} to Gnd. So Ileak1 is less than Ileak2. If natural stacking of transistors do not exist in a circuit, then to utilize the stacking effect a single transistor of width W is replaced by two transistors each of width W/2. The proposed D flip-flop circuit using stacking effect is shown in Fig. 5.The leakage reduction achievable in a two-stack comprising of devices with widths W_u and W_l compared to a single device of width w is given by equation 5 [23].

$$X=\frac{I_{device}}{I_{stack}}=\frac{w}{W_u^{\alpha}W_l^{1-\alpha}}10^{\frac{\lambda_d V_{dd}}{s}}(1-\alpha) \quad (5)$$

$$\text{where} \quad \alpha=\frac{\lambda d}{1+2\lambda d} \quad (6)$$

λ_d is the drain-induced barrier lowering (DIBL) factor and s is the sub-threshold swing co-efficient.

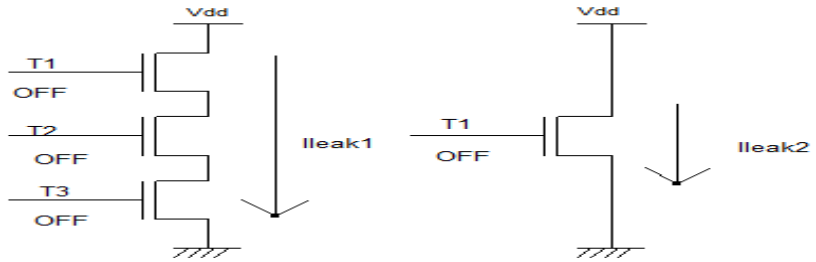
When $w_u = w_l = w/2$ then the leakage reduction factor or stack effect factor *X* is rewritten as

$$X=\frac{w}{\frac{w}{2}^{\alpha}\frac{w}{2}^{(1-\alpha)}}10^{\frac{\lambda_d V_{dd}}{s}}(1-\alpha) \quad (7)$$

$$X=2\times 10^{\frac{\lambda_d V_{dd}}{s}\left(\frac{1+\lambda_d}{1+2\lambda_d}\right)} \quad (8)$$

$$X=2\times 10^{u} \quad (9)$$

Where u is the universal two-stack exponent which depends only on the process parameter, λ_d and s, and the design parameter V_{dd}.Thus the leakage current through a single OFF device is greater than leakage through a stack of two OFF devices.



(a) (b)

Figure 4. Transistor stacking effect

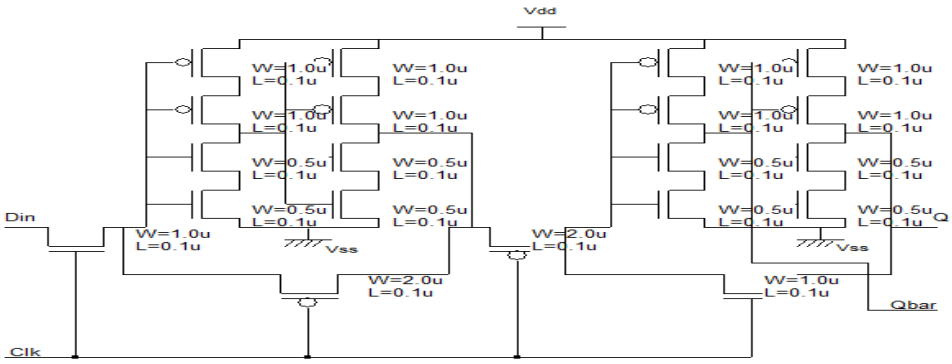


Figure 5. D flip-flop with transistor stacking

4.2. Self-adjustable voltage level circuit (SAL)

Fig. 6. Shows the general self-adjustable voltage level circuit [24], where V_{dd} is the supply voltage and V_L is the output voltage of this circuit, which is applied to any load circuit. (In this paper D flip-flop is the load circuit). During the active mode (when SL=0), this circuit supplies maximum supply voltage to the load circuit through the ON PMOS transistor (P1) so that the load circuit can operate quickly. During the standby mode (SL=1), it provides slightly lower supply voltage to the load circuit through the weakly ON NMOS transistors (N1, N2, N3 - -Nm). So the voltage applied to the load circuit is given by

$$V_L = V_{dd} - V_n \quad (10)$$

Where V_n is the voltage drop of m weakly ON NMOS transistors. The drain to source voltage V_{dsn} of the OFF NMOS in the standby mode is expressed as

$$V_{dsn} = V_L - V_{ss} = V_L \quad (11)$$

V_{dsn} can be decreased by increasing V_n that is increasing m, the number of NMOS transistors. When V_{dsn} is decreased, the drain- induced – barrier-lowering (DIBL) effect is decreased and this in turn increases the threshold voltage V_{tn} of NMOS transistors. Consequently the sub threshold leakage current of the OFF MOSFETs decreases, so leakage power is minimized, while data are retained. Fig. 7 shows the proposed leakage power reduced D flip-flop design using self-adjustable voltage level circuit.

5. SIMULATION RESULTS

In this work different designs of D flip-flops have been implemented in 90 nm CMOS process technology. The leakage power dissipation of the above circuits are compared with and without the power reduction techniques. The net lists of the circuits are extracted and simulated with BSIM4 models of MOSFET [25]. The simulations are done in HSPICE with a supply voltage of 1 volt, at a temperature of 27º C with a load capacitance of 50fF. The Fig. 8 and Fig. 9 show the input-output waveforms of D flip-flop with and without SAL circuit respectively. The power dissipation and delay of D flip-flops at 1 GHz clock frequency are given in Table I. The simulation results of D flip-flop with and without transistor stacking technique is presented in Table II. In this the leakage power reduction is more (12.27%) in D flip-flop designed using transmission gates. Table III shows the leakage power reduction using SAL technique and the reduction is maximum (36.93%) in transmission gate based D flip-flop. The leakage power and delay comparison of D flip-flops with the two proposed reduction techniques are given in Table IV. Fig. 10 shows the leakage power of the D flip-flops with and without the reduction techniques.

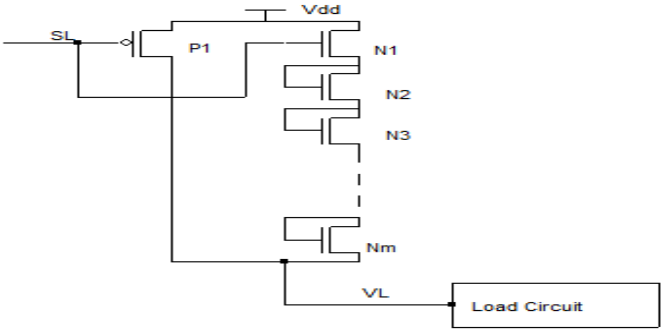


Figure 6. Self-adjustable voltage level circuit

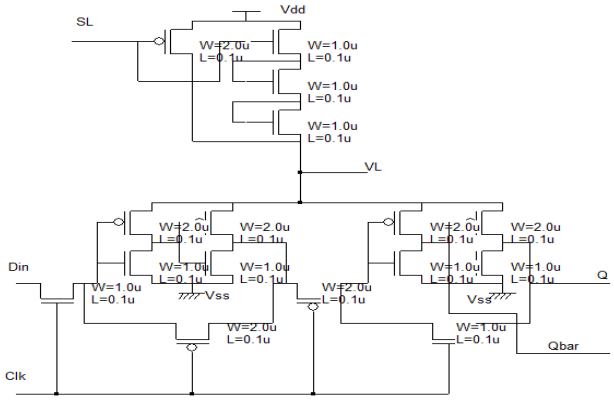


Figure 7. D flip-flop with self-adjustable voltage level circuit

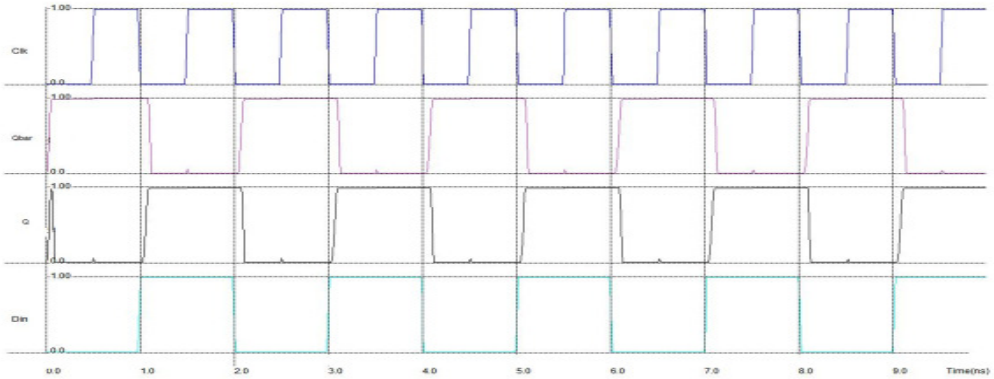


Figure 8. Input –Output Waveforms of DFF

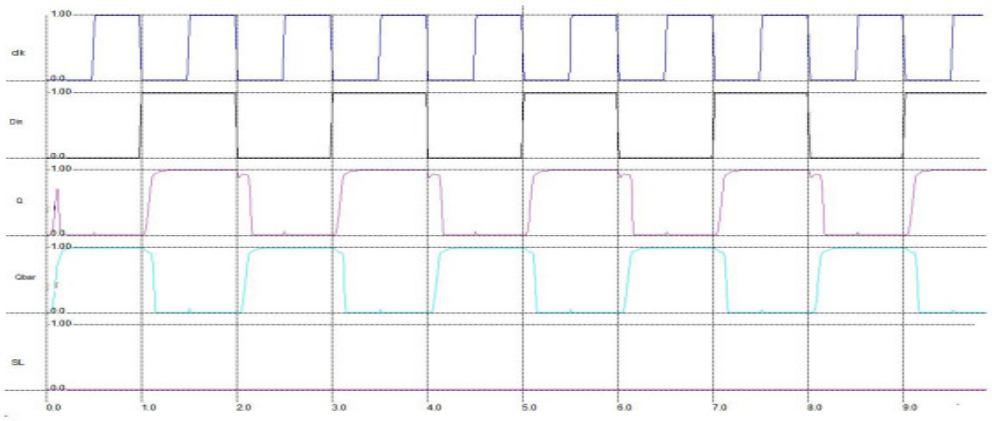


Figure 9. Input –Output Waveforms of D FF with SAL circuit

Table 1. Power dissipation and delay of DFFs at 1 GHz clock frequency

DFF Design using	No. of transistors	Delay (nS)				Max. delay (nS)	Avg. power (nW)
		CLK-Q		CLK-Q'			
		L-H	H-L	L-H	H-L		
Pass transistors	12	34	68	54	27	68	110.68
Transmission gates	18	39	36	47	51	51	150.56
GDI gates	18	67	104	80	112	112	157.70

Table 2. Leakage power of DFFs with transistor stacking technique

DFF Design using	P_{leak} (nW)		% Reduction in P_{leak}
	Without stack	With stack	
Pass transistors	11.59	10.60	8.54
Transmission gates	21.58	18.93	12.27
GDI gates	17.66	15.77	10.70

Table 3. Leakage power of DFFs with self-adjustable voltage level circuit

DFF Design using	P_{leak} (nW)		% Reduction in P_{leak}
	Without SAL	With SAL	
Pass transistors	11.59	9.13	21.23
Transmission gates	21.58	13.61	36.93
GDI gates	17.66	14.19	19.65

Table 4. Leakage power and delay comparison of D FFs with reduction techniques

DFF Circuit	PT+Stack	PT+SAL	TG+Stack	TG+SAL	GDI+Stack	GDI+SAL
P_{leak} (nW)	10.60	9.13	18.93	13.61	15.77	14.19
Delay (nS)	144	77	97	62	183	151

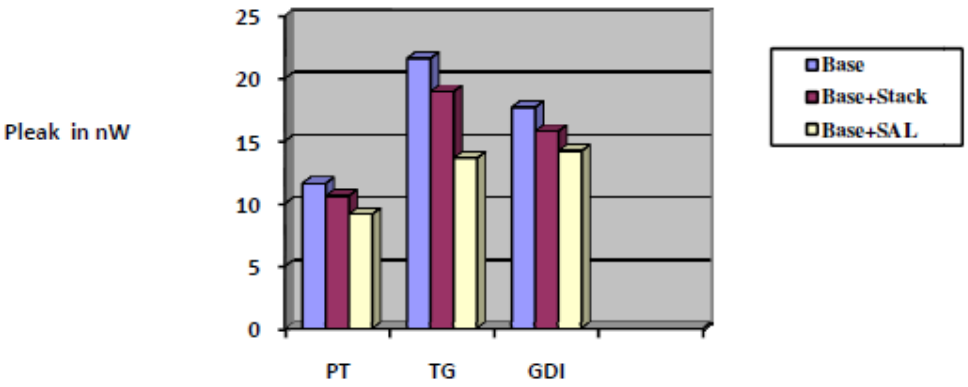


Figure 10. Leakage power in D flip-flops

6. CONCLUSIONS

In this paper three CMOS implementations of DFFs using pass transistors, transmission gates and GDI gates are proposed. The average power and delay (CLK-Q & CLK-Q') of the designs at 1 GHz clock frequency are presented .The DFF design using GDI gates has the maximum delay (112nS) and maximum average power (157.7nW). The leakage power of all the designs decrease when reduction techniques are applied. The percentage reduction of leakage power is more with the proposed SAL technique. The design of DFF using pass transistors with SAL technique gives the minimum leakage power of 9.13 nW. The design using TG+SAL gives least delay of 62 nS. Therefore for low leakage power applications PT+SAL design can be used in 90 nm technology.

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