Giga bit per second Differential Scheme for High Speed Interconnect

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Abstract **:** *The performance of many digital systems today is limited by the interconnection bandwidth between chips. Although the processing performance of a single chip has increased dramatically since the inception of the integrated circuit technology, the communication bandwidth between chips has not enjoyed as much benefit. Most CMOS chips, when communicating off-chip, drive unterminated lines with full-swing CMOS drivers. Such full-swing CMOS interconnect ring-up the line, and hence has a bandwidth that is limited by the length of the line rather than the performance of the semiconductor technology. Thus, as VLSI technology scales, the pin bandwidth does not improve with the technology, but rather remains limited by board and cable geometry, making off-chip bandwidth an even more critical bottleneck.*

In order to increase the I/O Bandwidth, some efficient high speed signaling standard must be used which considers the line termination, signal integrity, power dissipation, noise immunity etc

In this work, a transmitter has been developed for high speed offchip communication. It consists of low speed input buffer, serializer which converts parallel input data into serial data and a current mode driver which converts the voltage mode input signals into current over the transmission line. Output of 32 low speed input buffers is fed to two serializer, each serializer converting 16 bit parallel data into serial data stream. Output of two serializers is fed to LVDS current mode driver.

The serial link technique used in this work is the time division multiplex (TDM) and point-to-point technique. It means that the low-speed parallel signals are transferred to the high-speed serial signal at the transmitter end and the high-speed serial signal is transferred to the low-speed parallel signals at the receiver end. Serial link is the design of choice in any application where the cost of the communication channel is high and duplicating the links in large numbers is uneconomical.

I. INTRODUCTION

The ever-increasing processing speed of microprocessor motherboards, optical transmission links, chip-to-chip communications, etc., is pushing the off-chip data rate into the gigabits-per-second range. While scaled CMOS technologies continue to enhance on-chip operating speeds, off-chip data rates have gained little benefit from the increased silicon integration. In the past, off-chip high data rates were achieved by massive parallelism, with the disadvantages of increased complexity and cost for the IC package and the printed circuit board (PCB). Therefore, it is beneficial to move the off-chip data rate to the range of Gb/s-per-pin or above. Reducing the power consumption is also critical for battery-powered portable systems as well as some other

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systems in order to extend the battery life and reduce the costs related to packaging and additional cooling systems [8].

The increasing demand for more bandwidth to support inter-device communication or, from a more general viewpoint, to provide advanced voice, data and video applications via media interconnect is continuing to drive the development of high-speed serial transceivers. There are two methods for data transmission using transceivers - Single-Ended transmission and Differential transmission. Both of them have their benefits & disadvantages.

Single-ended transmission is performed by using one signal line for each information channel and a common ground return path shared among numerous information channels. The advantages of single-ended transmission are simplicity and low cost of implementation. A single-ended system requires only one line per signal. It is therefore ideal when cabling and connector costs are more important than the signaling rate or transmission distance. The main disadvantage of the single-ended solution is its relatively poor noise performance at high signaling rates or long distances. Because the noise coupled to the circuit adds to the signal voltage, it is susceptible to data errors.

Differential transmission addresses many of the shortcomings of single-ended solutions by using a pair of signal lines for each information channel. Differential signal pairs that are close together are generally exposed to the same noise sources. In addition to noise immunity, differential circuits radiate substantially less noise to the environment than single-ended circuits. This is primarily due to the complementary current in each line of the signal pair canceling each other's generated fields.

Differential signaling adds cost and complexity in silicon and interconnecting hardware where it is roughly double that for a single-ended interface but signal integrity and signaling rate is much more superior as compared to single ended signaling.

II. OVERVIEW

The overall block diagram with the internal modules is shown in Fig. 1.

The whole operation of the Serializer is controlled by the 16 clock phases that are generated from a reference clock using a Delay Lock Loop (DLL) module. The serializer receives 16 external inputs through low speed input buffer. The serializer converts the parallel data into serial data. During one clock cycle each input parallel data is present in the serial output for equal amount of time. This can be also be viewed as the low speed parallel data is getting converted to high speed serial data, the frequency of the data being increased by a factor of 16. The two serial data output from serializer is fed to current mode driver which converts the voltage mode input data into different current levels on the transmission line.

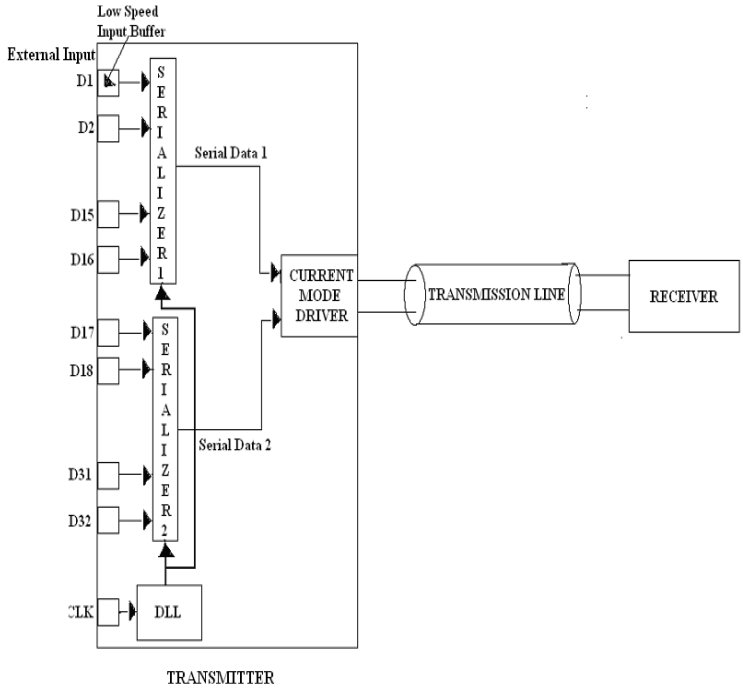

Figure 1 : Block Diagram

There are four different current levels over the transmission line corresponding to four possible combinations of input to current mode driver i.e – 00, 01, 10 and 11.

Low Speed input Buffer

Input buffers protect the internal circuit from sudden fluctuations in the input lines form the interface.

It should have high input impedance to avoid loading of the previous stage. Secondly, it must have hysteresis in its input output voltage characteristics, i.e. the maximum input voltage at which the output goes high when input changes from low to high must be greater than the minimum input voltage at which output goes low when input changes from high to low. This is to avoid unnecessary fluctuations in the input supply due to noise in the external input lines. The input buffer is implemented in fig 2.

The input buffer consists of 2 stages. The first stage provides the necessary hysteresis required by the buffer. The second stage is a simple CMOS inverter which improves the transition time.

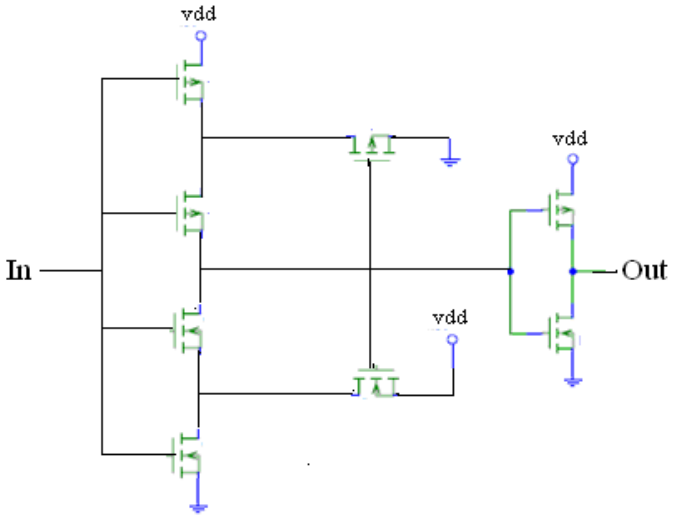

Figure 2 : Low speed input buffer

The input and output waveforms for the low speed input buffer at 500 Mhz are shown in fig 3

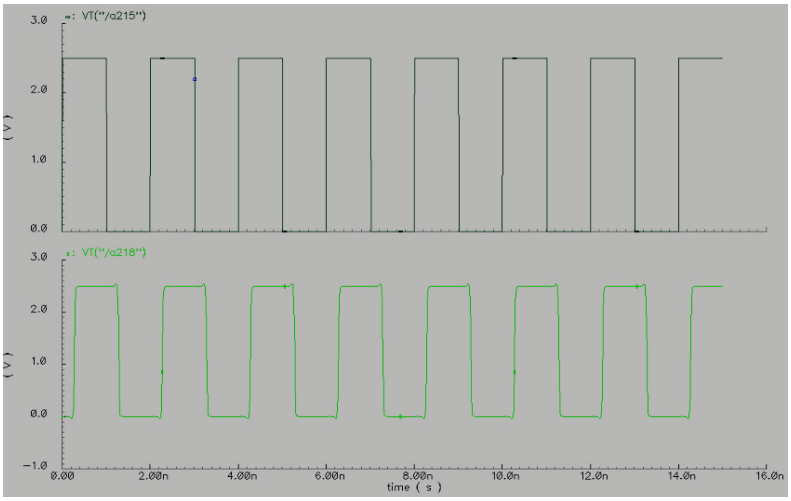

Figure 3 : Input and output waveforms

Figure 4 shows that the input buffer has a hysteresis of about 0.5V, with V_{ih} = 1.39 and V_{il} = 933 mV.

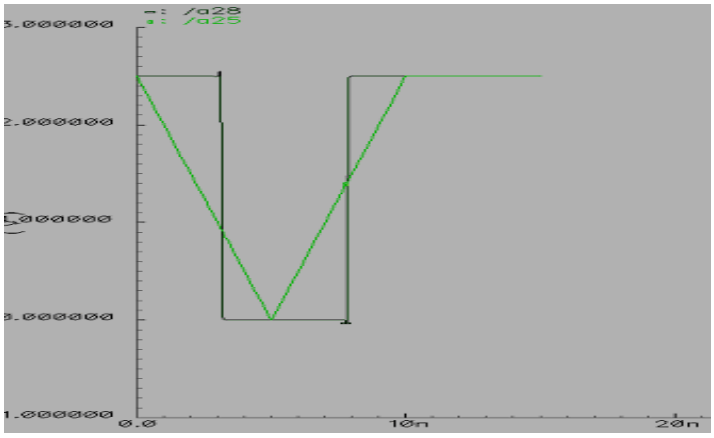

Figure 4 : Hysteresis in low speed input buffer

Serializer

The serializer converts the 16 parallel input data to serial data using the different phases of the clock generated by the DLL. It helps to generate the high-speed data for the current mode driver from the low speed data.

This is achieved by sampling and transmitting each of the low speed parallel bits over the serial link in independent and non-overlapping time intervals as shown in fig 5. In other words, in each clock cycle each of the parallel data is present once and for equal duration of time. So the high-speed data is 16 times faster than the low speed data.

The underlying logic to convert the parallel data ((D (1), D (2), … D (16)) to serial data (S) can be shown as:

S = (CLK (1). ~CLK (2). D (1)) + (CLK (2). ~CLK (3). D (2)) + …… + (CLK (16). ~(CLK (1) .D (16))

where (. ~ +) denote logical AND, NOT and OR operations respectively.

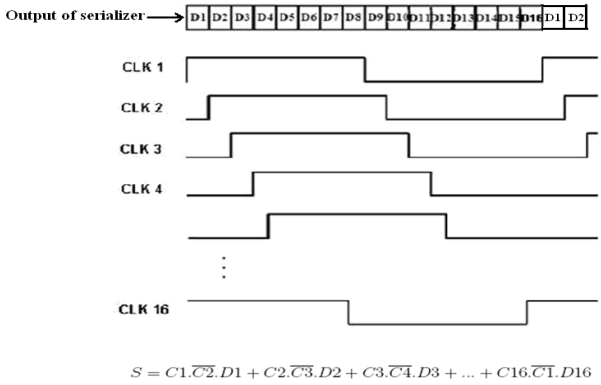

Figure 5: Parallel to serial conversion

Block Level Diagram:

At the block level, the serializer consists of 4 main blocks as shown in fig 6:

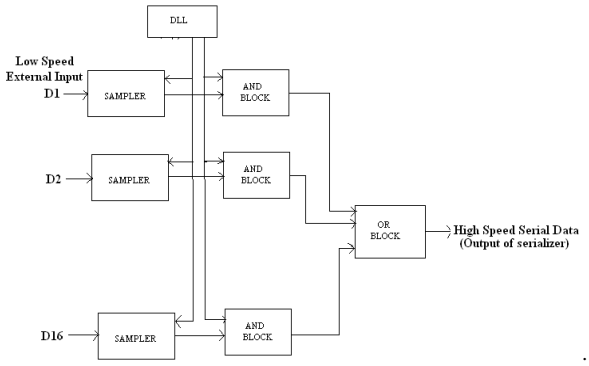

Figure 6 : Block level diagram of serializer

The first block is the sampling block where each of the parallel inputs are sampled and held in order to avoid any error in the subsequent stages due to fluctuation in the input signal. Each parallel input is sampled by using a positive edge-triggered flip-flop as shown in fig 7. The positive edge-triggered flip-flop is implemented by cascading a negative latch with a positive latch. The negative latch acts as the master while the positive latch acts as the slave. CLK refers to the clock phase used for sampling while CLK_INV is its inverted phase.

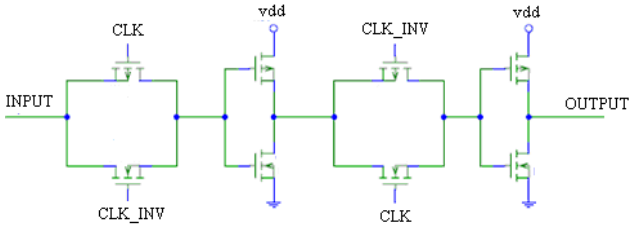

Figure 7 : Positive Edge-triggered flip-flop

The second block consists of 16 identical sub-blocks corresponding to each input and is implemented using CMOS logic to implement the AND logic:

(CLK (i). ~CLK (i+1). D(i)).

The AND gates are constructed by using NAND gates followed by inverters to increase the driving capability of this stage. Figure 8 shows the NAND gate for the first parallel data D1. Sixteen such blocks are placed to obtain 16 terms, which are further used by OR block to perform the addition of 16 terms corresponding to each external input D1 till D16.

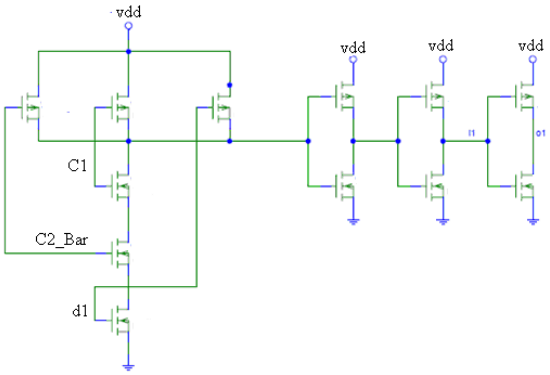

Figure 8 : AND logic implementation

The third block is implemented using pseudo nmos logic with feedback as shown in figure 9. This topology is preferred over other topologies since it is able to meet the speed requirements at all process corners without the need for any tuning options. OR operation is implemented by inverting the logic obtained from NOR gate.

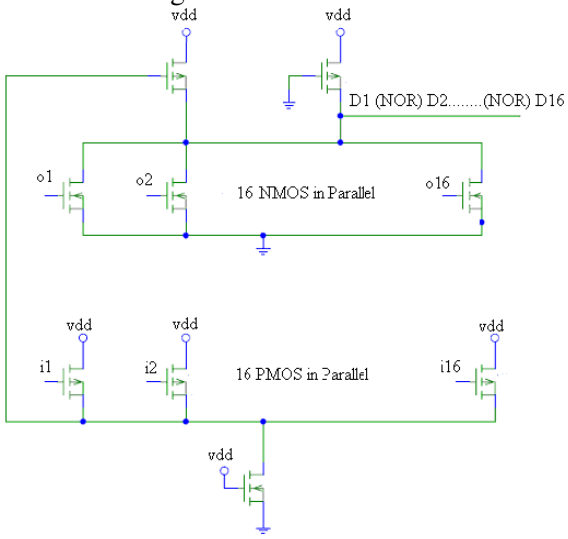

Figure 9 : OR Block

o1 till o16 is output of 16 AND blocks and i1 till i16 is inverted output of 16 AND Blocks.

The fourth block is implemented using a series of inverters as shown in figure 10. This is placed after the OR block so as to increase the driving power of the serial data.

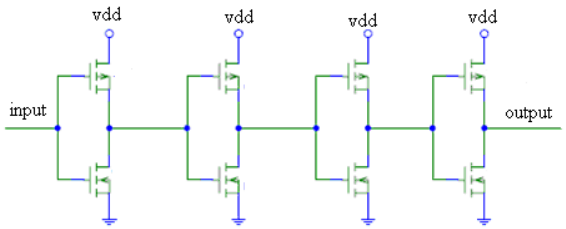

Figure 10: Inverter chain

The performance results of the serializer at 5 Gbps – output of third and fourth block for typical, fast, slow process corners are as shown in fig 11, 12, 13 respectively. Inverter chain improves transition time of the signal i.e reduces the rise time and fall time. It also helps to maintain the signal amplitude level at constant level.

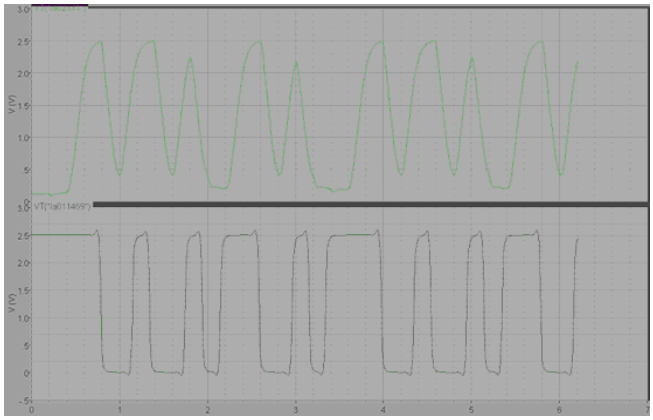

Figure 11: Output waveform of Serializer for typical process corner

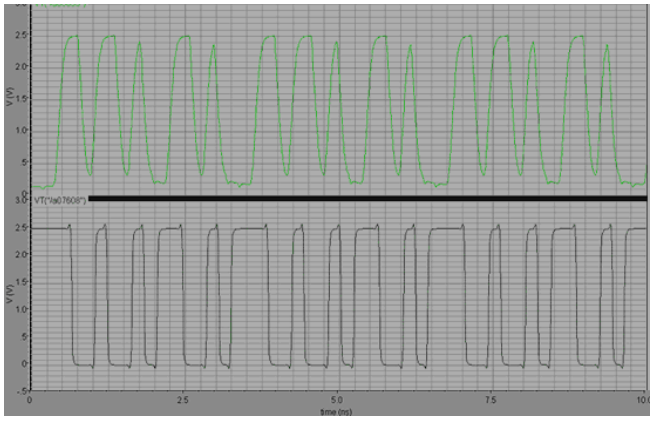

Fig 12: Output waveform-Both PMOS and NMOS fast

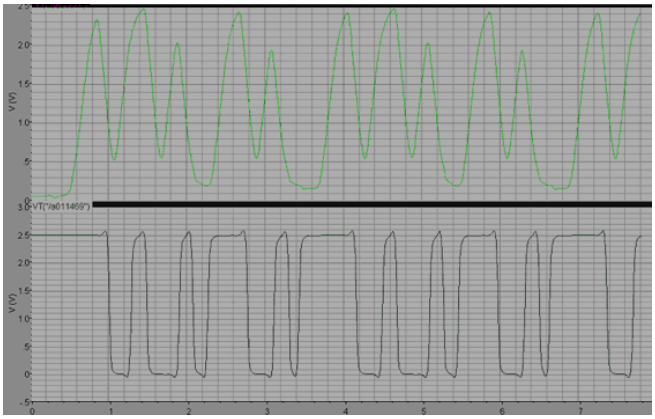

Fig 13: Output waveform-Both PMOS and NMOS slow

Current Mode Driver

In order to maintain compatibility between the transmitting and receiving ends several signaling standards (PECL, ECL, CML etc) have been developed and adopted in the industry for high speed communication. Of all the existing standards, LVDS is the most popular standard. An LVDS interface [1] [5] has a low-voltage swing (250–400 mV); it is connected point-to-point and achieves very high data rates (up to 500 Mb/s per signal pair) and reduced power dissipation [1] [9].

In this scheme, data is represented by multi-level currents on the transmission line instead of multi-level voltages. The current mode scheme [3] [4] consumes less power and is faster by reducing the voltage swing on the transmission line [6] [10].

The current mode driver as shown in fig 14 converts voltage mode input bits b1 and complement b1" into current mode signals over the transmission line. A and B are connected to transmission line.

If b1=0, current flows from M1 to A and is sinked from B through M4. Similarly if b1=1, current flows from M2 to B and is sinked from A through M3.

Circuit shown in fig 15 consists of 3 current mode drivers connected to common transmission line. All the 3 current mode drivers are identical with each other. Serial data 2 controls second driver while serial data 1 controls first and third driver. 100 ohms differential resistance is connected because if some reflection takes place at the receiver then that reflected wave could not be further re-reflected at the transmitter side.

Depending on the four combinations of serial Data 1 & Serial Data 2- 00, 01, 10, 11, four different currents [6] [7] will flow in transmission line corresponding to each combination. It is shown in Table 1.

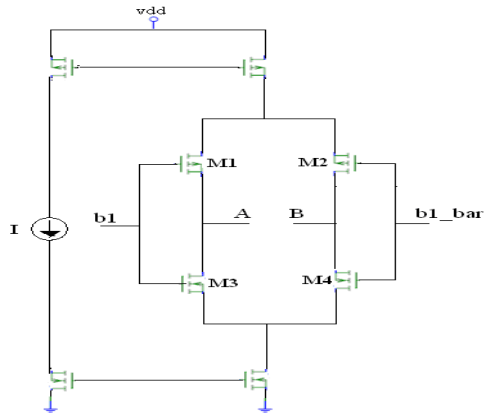

Figure 14. Current Mode Driver

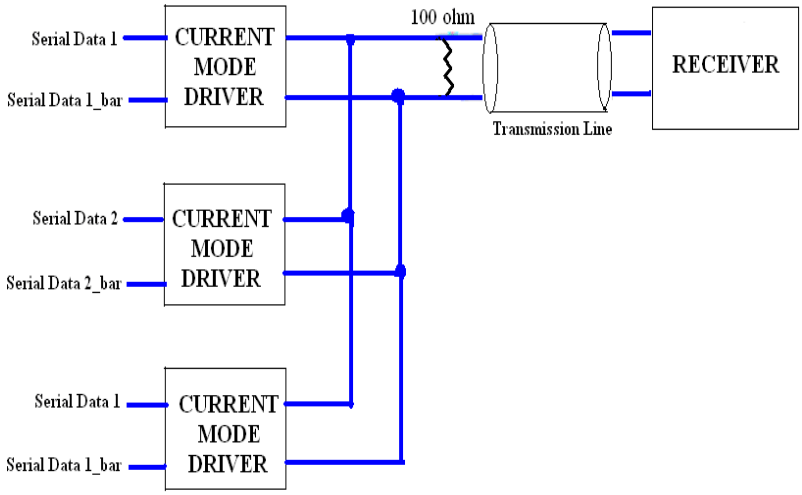

Figure 15. Complete Circuit

Serial Data 1	Serial Data 2	Current
0	*0*	*120uA (3I)*
0	*1*	*40uA (I)*
1	*0*	*-40uA (-I)*
1	*1*	*-120uA (-3I)*

TABLE 1 : DIFFERENT CURRENT LEVELS OVER TRANSMISSION LINE

As seen, the 4 different levels of current[10] are flowing in transmission lines (3I, I, -I,-3I). The maximum level of current is 120uA which corresponds to 00 combination

For 00 combination, PMOS transistors receiving 0 bit are ON. So current on transmission line will be equal to 120uA ((80u A + 80uA + 80uA)/2)=(240uA / 2).The total current of 240uA will be divided into two equal parts since there is a resistance of 100 ohms between the drivers & also the differential input impedance of receiver is 100 ohms. Similarly for 11 combination,

NMOS transistors receiving 1 bit are ON. So the polarity of current will be negative as the current is sinked from top branch of transmission line. Hence -120uA is flown.

Current mode receiver will receive these 4 different current levels and will convert current into four different voltage level. The maximum voltage level will be produced by 00 combination and minimum voltage level will be produced for 11 combination.

Current Levels over Transmission Line

The multiple current levels on the transmission line [6] [7] are as shown below in the figure 16. There are 4 different current levels. The peak current corresponds to b1b2=00 and minimum current corresponds to b1b2=11 combination. The input data rate of bits b1 and b2 is 5 Gbps.

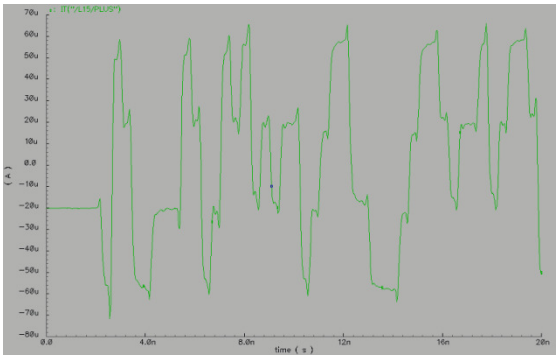

Figure 16. Eye Diagram (5Gbps)

Channel Characteristics

The channel is a low pass backplane channel. The line attenuation increases with increase in frequency and hence the channel acts as a Low Pass filter. The backplane is a fixed differential transmission line. The models for simulations are usually captured in s4p type of files. These files are s-parameter files. As the link is a differential link, it has 4 ports, two at the input and two at the output. Thus we have a file which gives information about the s-parameters of the 4-port link. All the effects like cross-talk, signal loss due to skin effect and other high frequency effects are captured by s-parameters.

The step response of channel for two different lengths of transmission line is shown in Fig 17.

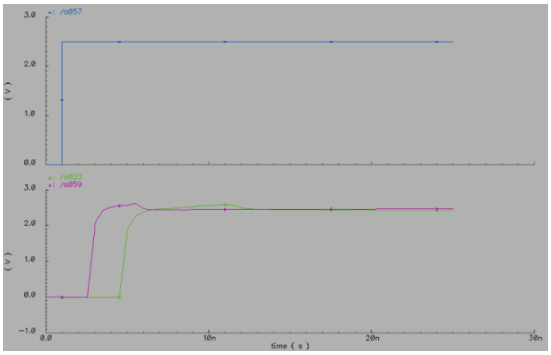

Fig.17: Step response of the link for 7.5 inch, & 18.5 inch

As seen, delay of transmission line with length 18.5 inches is more than that of line with length 7.5 inches.

The impulse response of the channel with 50 ohm termination at the transmitter end for 7.5 inch and 18.5 inches of transmission line is shown in figure 18. As seen from the figure, the attenuation provided by 18.5 inch transmission line is more than that of 7.5 inch line.

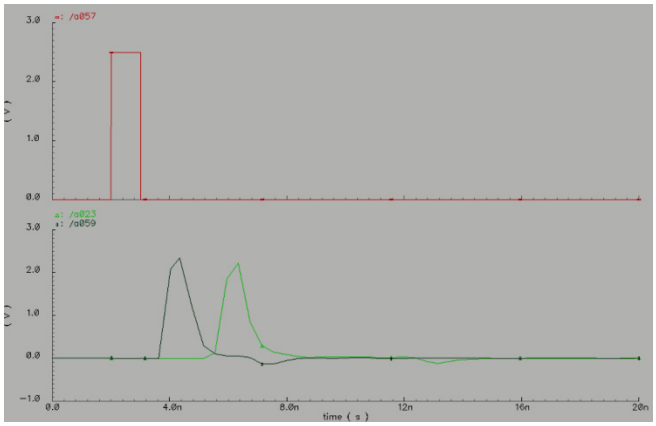

Fig.18: Impulse response of the link

The impulse response without termination at the transmission line is shown in fig 19.

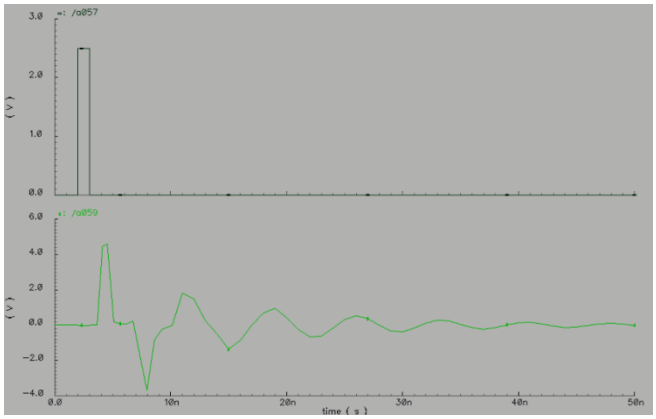

Fig.19: Impulse response without termination at transmitter end

If any signal is reflected, the signal would travel all the way back to the source. If there is no terminator at the source, there too it will undergo a reflection. This signal would again travel to the receiver and interfere with the fresh input signal. Hence, there will be ISI. Therefore it is necessary to use 50Ω termination at the transmitter side too. The source terminator prevents subsequent reflections keeping the signal at the receiver clean.

Pre Layout Simulation Results

Full chip simulation has been carried out, by integrating the serializers with current mode driver.

Full chip simulation results at 5 Gbps (2.5 Gsps) are shown in Fig 20 and 21 corresponding to 7.5 and 18.5 inch transmission line.

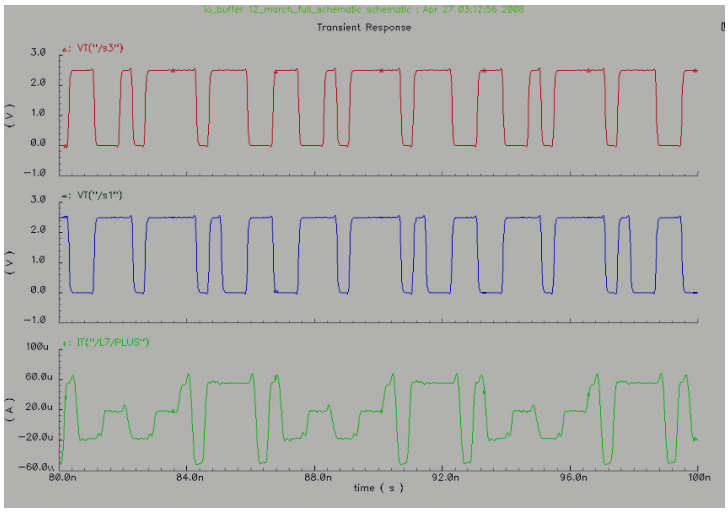

Figure 20. Serializer 1, serializer 2 output, current over 7.5 inch transmission line

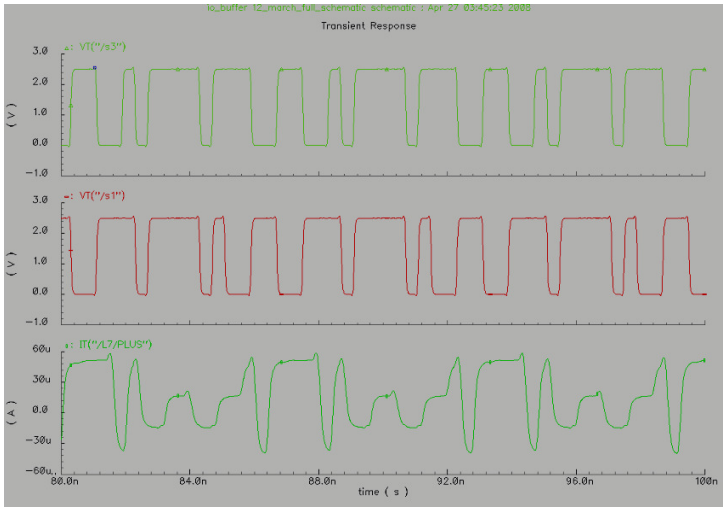

Figure 21. Serializer 1, serializer 2 output, current over 18.5 inch transmission line

Eye diagram:

The eye diagram [2] for input data at 5Gbps, 10Gbps respectively is as shown in fig 22, 23 respectively. The eye Diagram is taken by terminating the transmission line by a differential resistance of 100 ohms at the receiver.

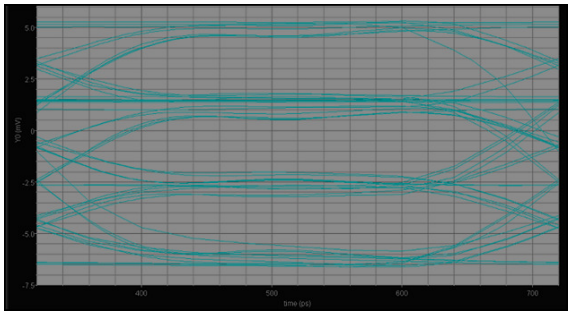

Figure 22. Eye Diagram at 5 Gbps

The eye width is a measure of timing synchronization and jitter effects. Eye opening (height, peak to peak), is the measure of the additive noise in the signal. Distortion of the signal waveform due to intersymbol interference and noise appears as closure of the eye pattern. As expected eye width is more for data at 5Gbps than at 10 Gbps.

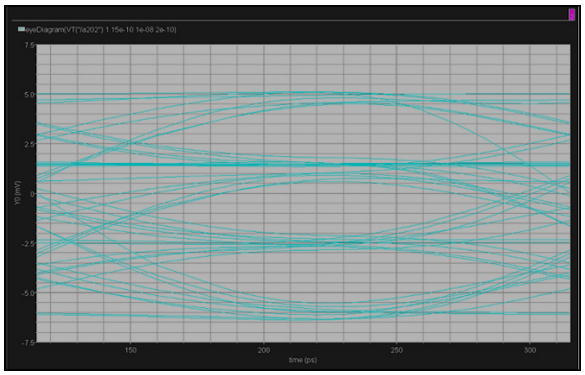

Figure 23. Eye Diagram at 10Gbps

III. CONCLUSION

Traditionally, the exchanges of data in a digital system have followed the bus technique. In the bus system, several parallel wires is used to interconnect a string of IC's. In order to synchronize the transmission and reception of data, a global bus clock is distributed to all the IC's. The operation cycle of the bus is divided into read period and write period. Based on the decision of the master, a given bus cycle is allocated so that a single IC in the system called "bus-slave" transmits data on the bus, while one or more receiver IC's capture the transmitted data. This system provides a shared communication resource, through which each IC can communicate with all the other IC's in the system.

Although this communication system was adequate in the past, increasing speeds are less immune to the transmission line effects thereby limiting the performance of conventional bus systems. In the past the length of the bus conductor was short to the rise time of the signals. In this case transmission line effects are insignificant. The interconnection can be modeled as an a distributed RC line. However, increasing signal speeds magnifies the effect of the final propagation velocity of the signal energy on the line, creating both signal integrity and timing uncertainty problems.

When signal rise times are comparable to the back and forth time of pattern of the signal through the line, distributed transmission line characteristics become important.

The intrinsic limitation of conventional buses has been removed by point-to-point links. From a circuit design view, the use of point-to-point transmission lines offers greater flexibility in the physical construction of the system. A point-to-point link has potential for higher communication bandwidth than a bus, due to its reduced signal integrity problems. Moreover, there are no skew related problems & efficient termination techniques avoid any reflection and hence can be used for multi Gbps applications.

Parallel low speed data inputs are serialized into a high speed serial data using a *serializer* such that each of the parallel data input is present in serial data only once during every clock cycle. The serial link technique is the time division multiplex (TDM) and point-to-point technique. Serial link is the design of choice in any application where the cost of the communication channel is high and duplicating the links in large numbers is uneconomical. The dominant design goal is to maximize the data rate across each link, and in some cases to extend the transmission range. As compared to parallel links, Serial links are more applicable to inter-system interconnects such as high speed off chip communication.

Topologically, the current mode driver is similar to *LVDS* (*Low voltage differential signaling*) [5] [11]. Being differential in nature, it has excellent noise immunity & reduced amount of noise immusion. Other advantages include low power consumption, & ability to integrate many channels per chip.

Current mode signaling [6] has been used in this work. As compared to voltage mode signaling, it offers many advantages like small propagation delay, signal integrity, low switching noise, and ability to operate effectively in presence of low supply voltage.

In order to avoid any reflection at the transmitter end, an internal 100Ω resistance is connected between the two output signal nodes of the driver. This resistor works as floating terminator across the differential signaling port and hence reduces reflection which otherwise might lead to signal integrity problem.

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