Dual Metal Gate and Conventional MOSFET at Sub nm for Analog Application

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Abstract

The use of nanometer CMOS technologies (below 90nm) however brings along significant challenges for circuit design (both analog and digital). By reducing the dimensions of transistors many physical phenomenon like gate leakage, drain induced barrier lowering and many more effects comes into picture. Reducing the feature size in the technology of device with the addition of ever more interconnect layers, the density of the digital as well as analog circuit will increase while intrinsic gate switching delay is reduced . We have simulated conventional and DMG MOSFET at 30nm scale using Silvaco TAD tool and obtained result. A two dimensional device simulation was carried out and observed that DMG MOSFET has a low leakage current as compared to conventional MOSFET and find suitable application in analog circuits.

Keywords

Gate leakage, DMG MOSFET, Silvaco TCAD tool, work function, trans-conductance, gain, Moore's Law.

1. Introduction

The evolution in CMOS technology is motivated by decreasing price-per-performance for digital and analog circuitry; its pace is determined by Moore's Law. CMOS evolution has come to a point where for analog circuits new phenomena need to be taken into account. A major issue is the decreasing supply voltage. Although the supply voltage has dropped from 5 V in the early nineties down to 1.2 V today. However, a further drop in supply voltages is expected to cause serious roadblocks for analog circuits, because the signal headroom becomes too small to design circuits with sufficient signal integrity at reasonable power consumption levels. Gate leakage will increase drastically when migrating to newer technologies. When the gate oxide thickness is reduced with the equivalent of one atomic layer, the gate leakage current increases by approximately one order of magnitude. Another issue is gate leakage current mismatch. For over thirty-five years, the integrated circuit (IC) industry has rapidly and consistently scaled (reduced) the design rules, increased the chip and wafer size, and improved the design of devices and circuits. In doing so, the industry has been following the well-known Moore's Law [1], which in its simplest form states that the number of functions per chip is doubled while the cost per function is halved every one-and-a half to two years. As a result of following Moore's Law, chip speed [2] and functional density have increased exponentially with time while average power dissipation per function and cost per function have decreased exponentially with time.

2. Conventional and Dual Metal Gate Mosfet

The SILICON industry has been scaling silicon dioxide (SiO_2) aggressively for the past 15 years for low-power, high-performance CMOS transistor applications. As we down scaling the MOSFET dimensions, gate dielectric thickness reduces and hence, gate leakage problem becomes major issue. So we need high gate dielectric thickness to reduce gate leakage. For that we go beyond the conventional MOSFET. If high gate dielectric is used then polysilicon depletion width effect is observed. To eliminate polysilicon depletion width effects and polysilicon dopant penetration, polysilicon gates need to be replaced by metal gates. The dual-metal-gate (DMG) MOSFET was proposed and fabricated, taking two different metal gates as gate electrode. DMG MOSFET has two laterally contacting gate materials with different work functions to achieve threshold voltage modulation and improved carrier transport efficiency. A proposal of new field-effect transistor (FET) where the gate voltage swing (i.e., the difference between the gate voltage and the threshold voltage) is varied along the channel in such a way that the charge carriers are accelerated more rapidly and the average carrier velocity in the channel is increased. If a more positive gate voltage is applied near the drain side than the electric field distribution along the channel is modified such that the electric field near the source becomes larger causing an increase in the gate transport efficiency.

DMG-MOSFET [3], in which two different materials having different work functions are placed together horizontally to form a single gate of a bulk MOSFET. In the DMG structure, the work function of the gate material (M1) close to source is chosen higher than the one close to drain end (M2) for n-channel MOSFETs. As a result, the electric field and electron velocity along the channel suddenly increases near the interface of the two gate materials which results in increased gate transport efficiency. This shows that the threshold voltage under gate material M1 is higher than that of under gate material M2. In this structure, the peak electric field at the drain end is reduced, which ensures that the average electric field under the gate is increased. This enables an increased lifetime of the device, minimization of the ability of the localized charges to raise drain resistance and more control of gate over the conductance of the channel so as to increase the on current. The improvement of on-state current is due to the existence of the extra electric field peak near the interface of both metals.

In the conventional MOSFET, electrons enter the channel with a low initial velocity, gradually accelerating toward the drain, and the maximum electron drift velocity is reached near the drain. Hence, the speed of the device is affected by a relatively slow electron drift velocity in the channel near the source region. Work function difference of the two metal gates causes an abrupt change in the conduction band energy, which provides an electric field peak in the channel, and gives greater acceleration to the carriers. Such high electric field accelerates the injected electrons. Therefore, the carrier injection effect is enhanced.

3. Simulation Study

For the computer simulations of the conventional and dual metal gate device, we used Silvaco TCAD programs. The main program used in the simulation was Atlas [4], which was used to actually simulate the conventional and DMG device and to extract the data. ATLAS allowed us to create a simplified version of these device in which it was easy to vary parameters such as gate length and doping, among others.

Gate length	30nm
Junction depth	13nm
S/D doping	1×10^{18} cm^{-3}
Substrate doping	1×10^{16} cm^{-3}

Table-1 List of various parameters

For N-channel MOSFET p-type doping is done in channel of same p-type dopant as used in substrate. Generally we can alter the doping concentration in channel region according to threshold voltage adjustment. A boron impurity of concentration 3.7e18cm^{-3} is used in this structure. The source and drain electrodes are of Aluminum. For conventional MOSFET structure the gate oxide thickness is 1nm. The other parameters are from the above table. The poly-silicon is used as gate material and it is heavily n-type doped of concentration 1e20cm^{-3} and is of thickness of 5nm.
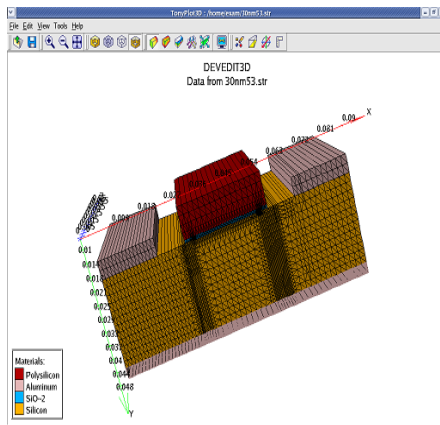

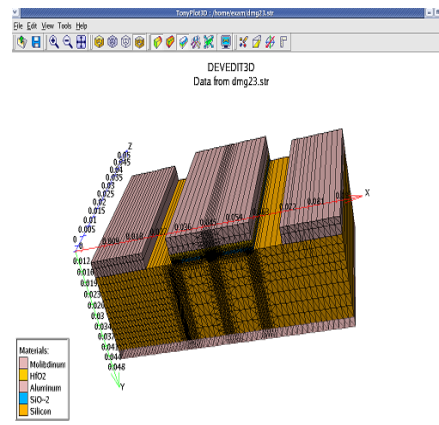
Fig-1 Structure of conventional MOSFET   Fig-2 Structure of DMG MOSFET

In DMG-MOSFET, high-K material is used to eliminate poly depletion effects. Hafnium Oxide is used as high-k material having permittivity of 24 and of thickness 2nm. The other parameters are from the above table. Silicon Dioxide is also used as interfacial layer between Hafnium Oxide and Silicon to improve interface properties and of thickness 1nm. Two metals are merged together to form a single gate electrode. Two metals in gate electrode are M1 and M2. M1 is of high work function metal i.e. molybdenum having work function of 4.55eV and M2 is of low work function metal i.e. Aluminum having work function of 4.1eV. The lengths of two metals are same. DMG-MOSFET having an advantage of lightly doped channel so as to reduce the mobility degradation and improved mobility and hence, improved trans-conductance. The doping in channel region is nearly 3.7e17cm^{-3}.

4. Results and Discussions

Fig-3 and Fig-4 shows the sub-threshold slope of conventional and DMG MOSFET. These results are obtained by using a two dimensional analysis using ATLAS, Silvaco TCAD tool. Using Silvaco TCAD tool, device characteristics are obtained.
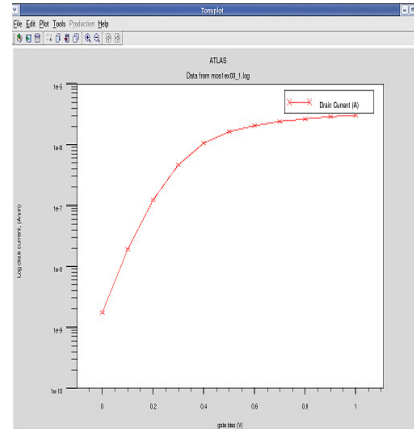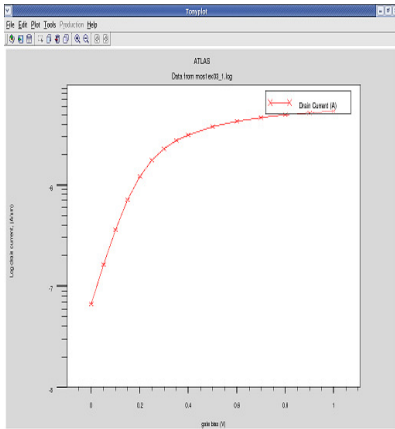
Fig-3 Sub-threshold slope of conventional MOSFET   Fig-4 sub-threshold slope of DMG MOSFET

Parameter/Device type	30nm conventional MOSFET	DMG-MOSFET
Sub-threshold slope(mV/decade)	127.3	94
Gate current(A/µm)	1.01×10^{-3}	9.13×10^{-8}
ꞇ =CV/I(ps)	0.7	2.14
µ(mobility)(cm²/Vs)	210.3	253.18

Table-2 List of observed parameters

5. Vital Parameters for Analog Application

5.1 Transconductance and Gain

The MOSFETs Transconductance gm is a key device parameter, determining the gain of MOSFET amplifiers. Transconductance defines the variation of drain current with gate source voltage. The transconductance plays a vital role in determining the switching speed of a circuit. It also defines the capability of device to drive the load efficiently. With the scaling of MOSFET [5], one can get higher transconductance.

Important device parameters are the channel conductance,

$g_d = \partial I_d / \partial V_{DS}$ with constant VGS
  $\{\beta(V_{GT} - V_{DS}),$ for $V_{DS} \leq V_{SAT}$
$\{$ 0, for $V_{DS} > V_{SAT}$

and the transconductance,

gm = ∂Id/∂VGS with constant VDS

{βVDS, for VDS ≤ VSAT

{βVGT, for VDS > VSAT

where β = $W\mu_nC/L$ is called the *transconductance parameter*. As can be seen from these expressions, high values of channel conductance and transconductance are obtained for large electron mobilities, large gate insulator capacitances (i.e., thin gate insulator layers), and large gate width to length ratios.

From above results shows that mobility is high in case of Dual Metal Gate MOSFET as compared to conventional MOSFET. Hence, the channel conductance and transconductance is high for DMG MOSFET. It determines that gain of DMG MOSFET is high as compared with conventional MOSFET which is key parameter for most analog devices.

5.2 *Gate Leakage And f_{gate} (fi)*

Besides its impact on conventional properties of circuits and devices, CMOS evolution introduces several new problems in analog design. One of the new phenomena is gate leakage [6]. Gate current due to direct tunneling through the thin gate oxide. This leakage depends mainly on gate-source voltage bias and gate area.

The 2001 ITRS utilizes the transistor intrinsic switching frequency, *fi*, as the figure of merit for transistor speed, *fi* is defined as the reciprocal of the transistor intrinsic delay:-

$$Ti = 1/fi = \{CgVdd)/I$$

where *Cg* is the gate capacitance per micron of transistor width for a MOSFET of gate length *Lg*, and Ion is the transistor saturation drive current (in units of amperes per micron of transistor width). *Ti* can be understood as approximately the time required for the MOSFET to charge or discharge the gate of an identical MOSFET through a potential difference of *Vdd* . Alternatively, *Ti* is approximately the switching delay of an inverter for a capacitive load *(CL)* equal to the gate capacitance of one transistor, (i.e., C L = *WCg,* units are farads). As from above equation, *fi* is dependent only on the transistor parameters and characteristics, and to maximize *fi, Ion* must be maximized, *fi* is a good figure of merit for the transistor intrinsic speed in dense logic circuits, where the interconnect wire lengths are short and load capacitance is dominated by the gate capacitance of the transistors in the fan out path. In contrast, for logic circuits with long interconnect wires, load capacitance is dominated by the wiring capacitance. For signal frequencies higher than this the input impedance is mainly capacitive and the MOSFET behaves as a conventional MOSFET. Otherwise, below it is mainly resistive and the gate leakage is dominant.

It follows that in this technology the gate appears to be capacitive for signal frequencies higher than roughly 0.1 Hz, while it appears resistive only at very low signal frequencies. Analog applications typically apply transistors biased at low and moderate gate-overdrive voltage.

DMG MOSFET has a high value of intrinsic delay (Ṭ) and hence a corresponding low value of intrinsic frequency as compared to conventional MOSFET of same technology. This implies that it is suitable for various analog applications which need transistors to be biased at relatively low voltage.

5.3 Impact of Gate Leakage

The new effects in ultra-deep submicron CMOS is the significant gate-leakage. In low frequency applications this become prominent because of long time constant [7]. In nowadays sub-micron CMOS gate-leakage may be a serious problem for analog circuit design because:

1. It poses a lower limits to the usable frequency range for integrator circuits; e.g. for filters and hold-circuits.

2. It introduces a strong relation

3. n between DC current gain and transistor length, which effectively limits accuracy.

4. Shot noise is due to gate-current.

5.3.1 The impact of gate-leakage on filters, integrators and hold circuits

The *fgate* gives the frequency below which the input impedance appears to be mainly resistive. For frequencies higher than *fgate* the gate appears to be mainly capacitive . For filters this simply implies that a MOS capacitance can be used as capacitance only for frequencies much higher than the *fgate*. Iin switched-current circuits and sample-and-hold circuits this behaviour limits its application. So, DMG MOSFET process to be better for filters and integrators and hold circuits because the gate leakage is very less as compared to conventional MOSFET at 30nm scale.

5.3.2 Gate-Leakage Matching and Its Implications

Gate leakage is caused by quantum-mechanical tunneling and depends on the layer thickness and the field strength. As such, it also exhibits spread. Relative spread, or matching, usually limits the achievable level of performance of analog circuits: it sets a lower bound on figures such as offsets in amplifiers and the accuracy in A/D converters.

Because spread and mismatch are dc effects, they do not (from a fundamental point of view) require any additional power. However, in practice they prove to be a major implementation problem [8]. Gate-leakage mismatch is an extra mismatch source with an area-dependency *different* from that of conventional matching [9]. Mismatch of gate leakage current is proportional to the gate current level.

5.3.3 The impact of gate-leakage on noise

Just as any current across a junction, gate leakage exhibits shot-noise with current density

$$S_{IG} = 2q * I_G$$

As such, it is equivalent to base-currents in bipolar transistors. This shot noise comes on top of the induced gate noise [10]. Noise in the gate current therefore limits noise performance in analog circuits in sub-micron CMOS.

6. Summary

The evolution of CMOS technology will continue for many years to come, which is beneficial for digital circuits but which is not so for analog. An extensive discussion of relatively new non-ideal effects such as gate-leakage and trans-conductance is given in this paper. The transconductance plays a vital role in determining the switching speed of a circuit. With the scaling of Mosfet one

can get higher transconductance. As the technology is scaled down, the device speed and performance will increase but at the cost of more leakage current. At 30nm scale, a comparison between conventional and DMG MOSFET was performed and observed that DMG MOSFET has a less value of gate leakage and high value of transconductance due to which it can be applicable in various analog applications like in filters, integrators and hold circuits.

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