LOW POWER FOLDED CASCODE OTA

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ABSTRACT

Low power is one of the key research area in today's electronic industry. Need of low power has created a major pattern shift in the field of electronics where power dissipation is equally important as area, performance etc. Several low power portable electronic equipments, low voltage design techniques have been developed and have driven analog designers to create techniques eg. Self cascode mosfet and stacking technique. For this aim in mind we designed a Folded Cascode using low power techniques and analyzed its various properties through the Spice simulations for 0.13 micron CMOS technology from TSMC and the supply voltage 1.8V.

Keywords

Folded Cascode OTA, Self Cascode, Stacking Technique

1. INTRODUCTION

Folded Cascode OTA[1] has been chosen since it allows shorting of input and output terminals with extremely negligible swing limitations. Folded cascode OTA[2] is used for high speed applications thanks to its capability to provide high gain and large bandwidth. The application of Low Power Consumption to the OTA structure provides significant decrease in power with increase in gain. Comer[3,4], In 2004 has explained an approach which may results in very high gain and low power dissipation[5,6] by discussing the effects on the overall composite cascode circuit performance with one device operating in the sub threshold and the other device operating in the active region. To have high output impedance and thereby high gains, cascoding is done, where two MOSFETs are placed one above the other [7-10]. The regular cascode structures are avoided as their use increases the gain of the structure. Sub threshold leakage is exponentially related to the threshold voltage of the device, and the threshold voltage changes due to body effect. From these two facts, one can reduce the sub threshold leakage in the device by stacking two or more transistors serially. The transistors above the lowest transistor will experience a higher threshold voltage due to the difference in the voltage between the source and body. In stacking technique, a transistor splits into two transistors having half the width preserving the total width same and same gate length. When gate voltage is below $V_{TH,}$ then sub-threshold or weak inversion conduction current between source and drain in an MOS transistor occurs.

2. LOW POWER TECHNIQUES

There are various low power techniques. In this paper we are going to explain two low power techniques.

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2.1. Self Cascode Technique

Self-cascode[11-15] is the new technique, which does not require high compliance voltages at output nodes. It provides high output impedance to give high output gain and so it is useful in low-voltage design. A self-cascode is a 2-transistor structure as shown in Figure 1[11], which can be treated as a single composite transistor. By using the composite structure, it has much larger effective channel length and the effective output conductance is much low. The lower transistor M1 is equivalent to a resistor, whose value is input dependent. For optimal operation, the W/L ratio of upper transistor M1 is kept larger than that of lower transistor M2, i.e., m>>1. For the composite transistor to be in saturation region M2 have to be in saturation and M1 in linear region. The effective g_m for the composite transistor is approximated as

$$g_m(\text{effective}) = \left(\frac{g_{m2}}{m}\right) = g_{m1} \tag{1}$$

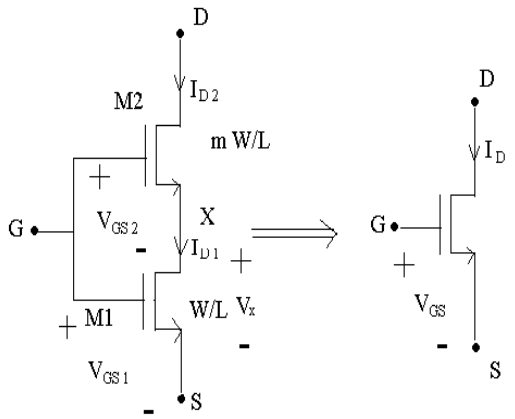

Figure 1. (a) Self Cascode NMOS transistor.

(b) Equivalent NMOS transistor.

For the composite transistor to be in saturation region M2 have to be in saturation and M1 in linear region. For these transistors, the currents I_{D1} and I_{D2} are given as

$$I_{D1} = \beta_1\left(V_{in} - V_{TN} - (V_X/2)\right)V_X \quad \text{(Ohmic)} \tag{2}$$

$$I_{D2} = \left(\beta_2/2\right)(V_{in} - V_X - V_{TN})^2 \quad \text{(Saturation)} \tag{3}$$

and from this we get

$$I_{D2} = \left[\left(\beta_2\beta_1\right)/\left(2\left(\beta_2 + \beta_1\right)\right)\right][V_{in} - V_{TN}]^2 \tag{4}$$

$$\beta_{\text{effective}} = \left(\beta_2\beta_1\right)/\left(\beta_2 + \beta_1\right) \tag{5}$$

for

$$\beta_2 = m\beta_1 \tag{6}$$

$$\beta_{\text{effective}} = [m/(m+1)]\beta_1 \;=\; [1/(m+1)]\beta_2 \tag{7}$$

and for m >> 1,

$$\beta_{effective} \approx \beta_1 \tag{8}$$

where $\beta = \mu C_{OX}(W/L)$ and is called the trans-conductance parameter.

M1 operates in linear region, while M2 operates in saturation or linear region. Hence voltage between source and drain of M1 is small. There is not much difference between the V_{Dsat} of composite and simple transistors and therefore, self-cascode can be used in low voltage operation.

For a self-cascode

$$V_{Dsat} = V_{Dsat-M2} + V_{DS-M1} \tag{9}$$

The operating voltage of regular cascode is much higher than that of self-cascode and hence a self-cascode structure can be used in the low voltage design. The advantage offered by self-cascode structure is that it offers high output impedance similar to a regular cascode structure while output voltage requirements are similar to that of a single transistor.

2.2. Stacking Technique

In stacking technique[17] a transistor splits into two transistors having half the width preserving the total width same and same gate length to reduce power consumption with increase in gain as shown in Figure 2. The sub-threshold leakage current is given as:

$$I_{SUB} = I_0 e^{\left(\frac{V_{GS}-V_{TH0}-\eta V_{DS}+\gamma V_{SB}}{nV_T}\right)}\left(1 - e^{\frac{-V_{DS}}{V_T}}\right) \tag{10}$$

$$I_O = \mu C_{OX}\left(\frac{W}{L}\right)V_T^2 e^{1.8} \quad , \quad V_T = \frac{KT}{q} \tag{11}$$

μ = carrier mobility, C_{ox} = gate oxide capacitance per unit area, W and L = width and effective length of the transistor, K = Boltzmann constant, T = absolute temperature, and q = electrical charge of an electron. In addition, V_{TH} = zero biased threshold voltage, γ = body effect coefficient, η = drain-induced barrier lowering (DIBL) coefficient, n = slope shape factor sub-threshold swing coefficient.

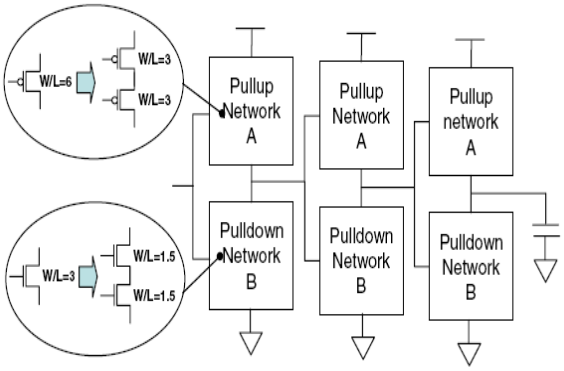

Figure 2. Stack

As with the increase of the V_s of the transistor, the sub-threshold leakage current reduces exponentially. This would happen due to the following reasons:

- The Gate-to-Source voltage (V_{GS}) would reduce and if the input applied is grounded, it would turn negative .This would reduce I_{SUB} exponentially Threshold voltage increases due to body effect.
- The DIBL coefficient decreases due to lower drain to source potential thereby further reducing leakage.

3. PROPOSED FOLDED CASCODE OTA

By using low power techniques i.e Self Cascode technique and Stacking Technique, proposed Folded Cascode OTA is designed and then the comparison is shown between these two techniques.

3.1. Proposed Folded Cascode using Self Cascode Technique

The Proposed Folded Cascode OTA using Self Cascode is shown in Figure 3. At input terminals self cascode is not used but on rest of the circuits self cascode is used because this whole circuit works as load. In this proposed circuit we take the value of m=2. In this circuit each transistor splits into two so that upper transistors are working in saturation region while other is in linear region to work this circuit properly. And that of proposed folded cascode using stacking technique is shown in Figure 4.

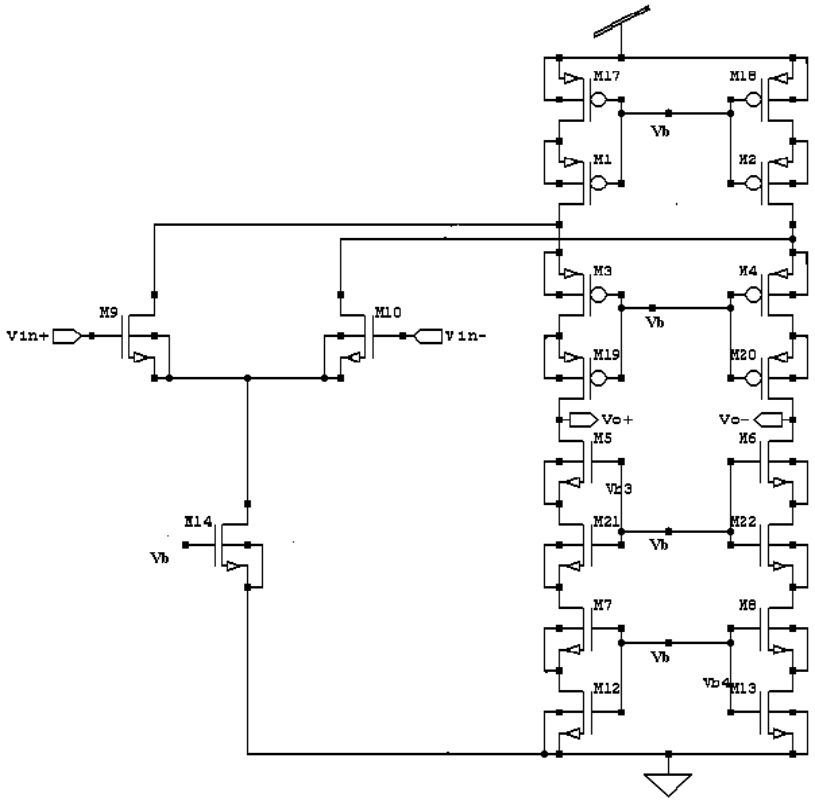

Figure 3. Proposed Folded Cascode OTA with Self Cascode Technique

3.2. Proposed Folded Cascode using Stacking Technique

The Proposed Folded Cascode OTA using Stacking Technique is shown in Figure 4. At input terminals stacking is not used but on rest of the circuits stack is used because this whole circuit works as load. All the transistors are working in saturation region.

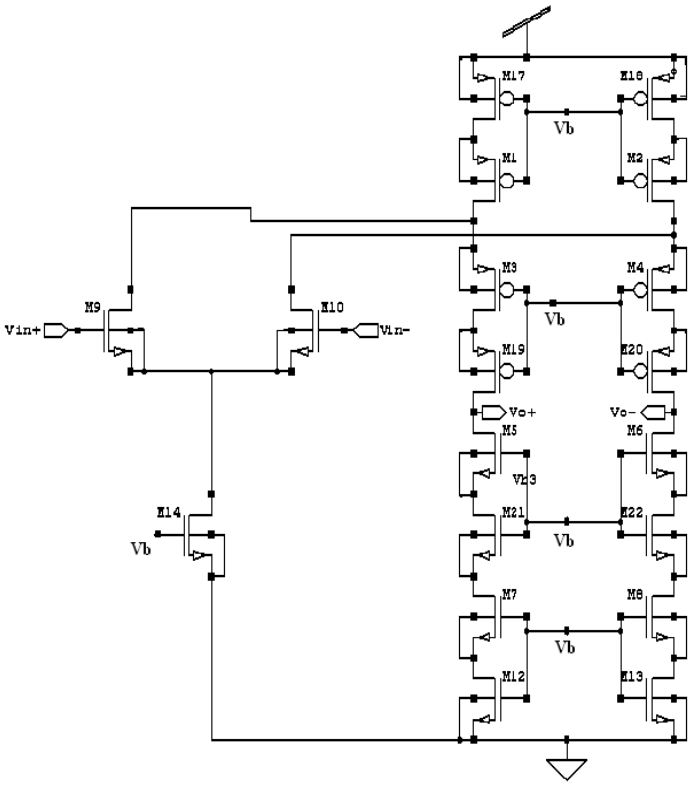

Figure 4. Proposed Folded Cascode OTA with Stacking Technique

4. CHARACTERISTICS OF PROPOSED FOLDED CASCODE OTA

The simulations are done with the help of Tanner EDA tool T-SPICE and waveforms are analyzed on W-Edit. Some of the characteristics of Proposed Folded Cascode OTA are discussed below.

4.1. Gain

Gain is a measure of the ability of an op-amp to increase the power or amplitude of a signal from the input to the output. Gain is the ratio of the output voltage and the differential input voltage. The dc gain of Proposed Folded Cascode OTA using Self Cascode is 49.91 db as shown in Figure 5. And by using Stacking Technique is 68.32db as shown in Figure 6.

$$A_v = \frac{\text{Output Voltage}}{\text{Differential input Voltage}}$$

$$A_v = \frac{V_o}{V_{in}}$$

$$A_v = 20 \log\left(\frac{V_o}{V_{in}}\right) db$$

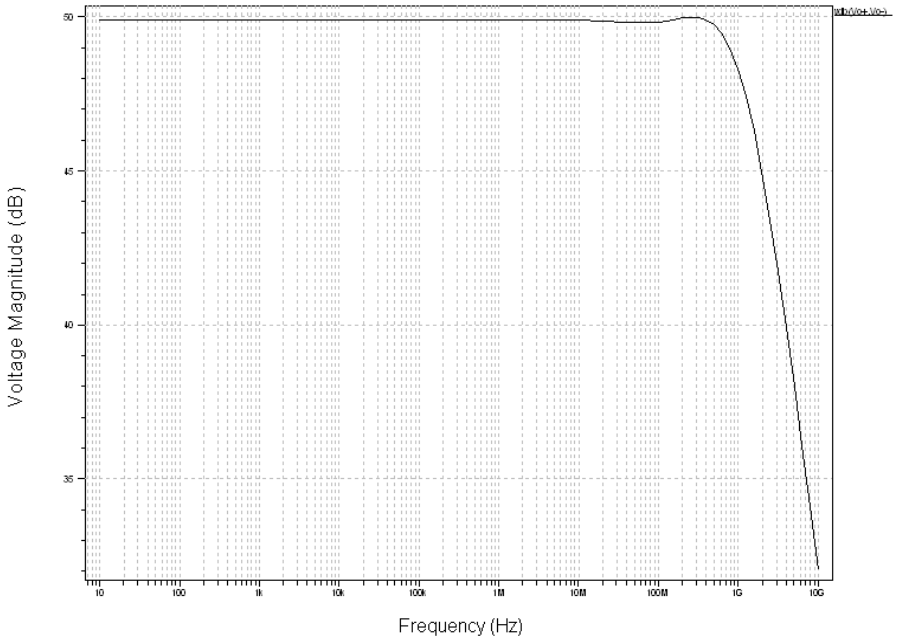

Figure 5. Voltage Gain of Proposed Folded Cascode OTA using Self Cascode

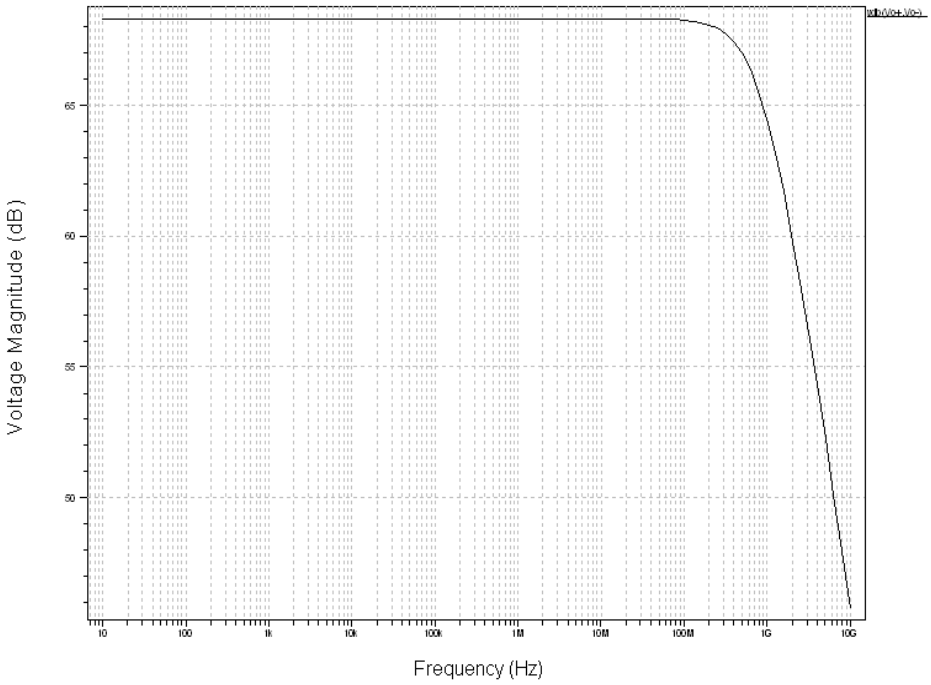

Figure 6. Voltage Gain of Proposed Folded Cascode OTA using Stacking

4.2. Effect of Temperature

For a system to be stable, its performance must remain constant with the variation in temperature. The effect of temperature variations on Proposed Folded Cascode OTA using Self Cascode Technique and Stacking Technique is shown in Figure 7 and Figure 8 respectively.

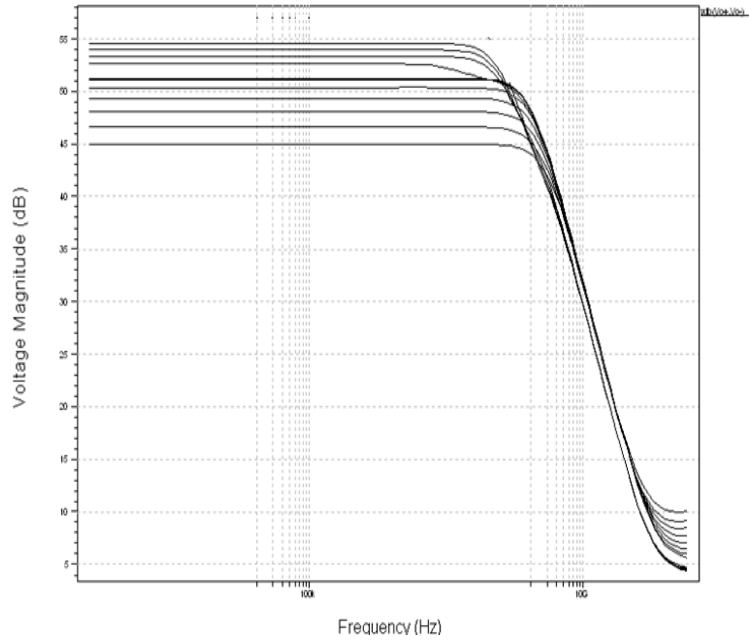

Figure 7. Effect of Temperature on Proposed Circuit using Self Cascode.

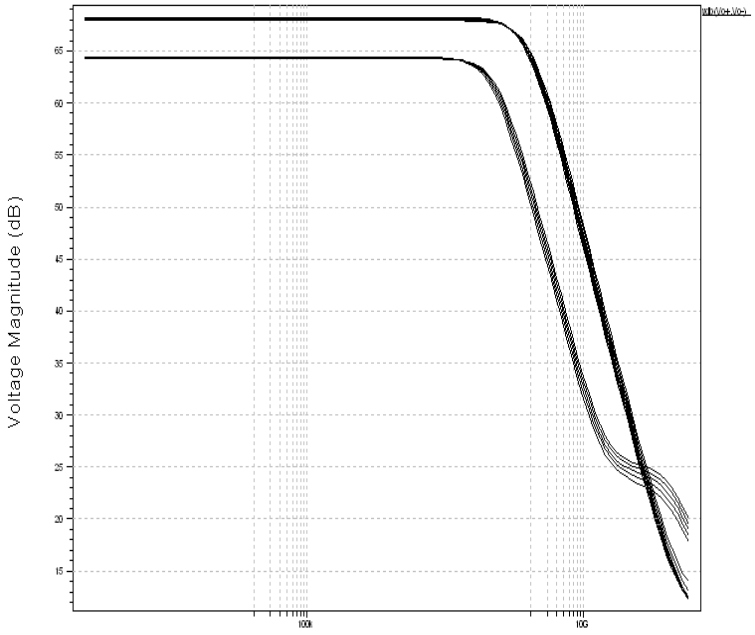

Figure 8. Effect of Temperature on Proposed Circuit using Stacking.

4.3. Power Consumption

Power consumption (PC) is defined as the amount of quiescent power (v_{in}= 0V) that must be consumed by the OTA in order to operate properly. The amount of average power consumption of Proposed Folded Cascode OTA using Self Cascode Technique and Stacking Technique is 4.442021e-002 Watts and 1.189980e-002 Watts respectively.

5. SIMULATION RESULTS

Simulation has been done on tanner EDA tool at TSMC 130nm technology with 1.8 V supply voltage. TSPICE simulation results of the circuit confirm the effectiveness of the approach. Proposed FCA shows better performance when circuit area is not a major concern. The design specifications and the summary of simulation results are shown in Table 1. The size of all devices is shown in Table 2.

Table 1. Simulated Results of Proposed Folded Cascode OTA

Characteristics	**Self cascode**	**Stacking**
Power Supply	1.8V	1.8V
Power consumption	4.442021e-002 W	1.189980e-002 W
Open loop gain	49.91 db	68.32 db
Temperature Effect	Less	Very Less

Table 2. W/L for various transistors (µm)

DEVICE	**Type**	**Proposed FCA with Self Cascode**	**Proposed FCA with Stacking**
M1/M2	PMOS	105.6/0.5	52.8/0.5
M3/M4	PMOS	105.6/0.5	26.4/0.5
M5/M6	NMOS	28/0.5	7/0.5
M7/M8	NMOS	20.8/0.5	5.2/0.5
M9/M10	NMOS	10/0.18	10/0.18
M12/M13	NMOS	10.4/0.5	5.2/0.5
M14	NMOS	19.8/0.5	19.8/0.5
M17/M18	PMOS	211.2/0.5	52.8/0.5
M19/M20	PMOS	52.8/0.5	26.4/0.5
M21/M22	NMOS	14/0.5	7/0.5

6. CONCLUSION

In this paper, we have presented low power techniques which promise low voltage design with high gain. We can use these techniques where area factor is not considered. By using self cascode technique the gain of proposed folded cascode is increased about 9db with decrease in average power consumption. And by using stacking technique gain is increased about 27db with decrease in average power consumption. The regular cascode structures are avoided as their use increases the gain of the structure, but decreases the output signal swing. Self-cascode is the new technique, which does not require high compliance voltages at output nodes. It provides high output impedance to give high output gain and so it is useful in low-voltage design. By increasing the value of m, we can further increase the gain of the folded cascode OTA with average low power consumption. But the condition of self cascode should be maintained. The effect of temperature is comparatively less in comparison to the conventional folded cascode OTA. Noise effect is also less in proposed Folded Cascode OTA. This folded cascode circuit have been employed in a variety of situations from increasing the gain in amplifiers with medium available bandwidth. The

channel lengths and widths of the two transistors can be optimized for the largest increase in the output resistance. These techniques can extensively be applied where power supply and area requirements are not the constraint and that high gain and average power dissipation is of utmost importance.

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