

# BUS ENCODER FOR CROSSTALK AVOIDANCE IN *RLC* MODELED INTERCONNECTS

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## **ABSTRACT**

*Most of the encoding methods proposed in recent years have dealt with only RC modeled VLSI interconnects. For deep submicron technologies (DSM), on-chip inductive effects have increased due to faster clock speeds, smaller signal rise times and longer length of on-chip interconnects. All these issues raise the concern for crosstalk, propagation delay and power dissipation of overall. Therefore, this research work introduces an efficient Bus Encoder using Bus Inverting (BI) method. The proposed design dramatically reduces both crosstalk and power dissipation in RLC modeled interconnects which makes it suitable for current high-speed low-power VLSI interconnects. The proposed model demonstrates an overall reduction of power dissipation and crosstalk induced delay by 55.43% and 45.87%, respectively.*

## **KEYWORDS**

*Inductance effects, Bus-invert, Crosstalk, Power dissipation.*

## **1. INTRODUCTION**

The performance of a high-speed chip in deep sub-micron technology is largely dependent on interconnects which connect different macro cells within a VLSI/ULSI chip [1]. With ever-growing length of interconnect and on chip clock frequency, the effects of interconnects cannot be restricted to *RC* models. The importance of on-chip inductance is continuously increasing with faster rise time, wider wires, and introduction of new materials for low resistance interconnects. It has become well accepted that interconnect delay dominates gate delay in current deep sub micrometer VLSI circuits. Inductance can increase the interconnect delay [2, 3] per unit length and can cause ringing in the signal waveforms, which can adversely affect signal integrity. Furthermore, inductive effects in global interconnects are more severe due to lower resistance per unit length of line, as a result interconnect impedance becomes comparable to the resistive component. On the other hand, longer current return path has been achieved due to the presence of mutual inductive coupling between interconnects.

There are different methods for the reduction of crosstalk such as repeater insertion, shielding line ( $V_{dd}/GND$ ) insertion between two adjacent wires [4], optimal spacing between signal lines and lastly the most effective Bus encoding method [5]-[10]. This paper uses bus invert method for the reduction of power dissipation, crosstalk, propagation delay and chip size of encoder and decoder of *RLC* modeled interconnects. Here, the proposed method reduces two undesirable types of crosstalk i.e., Type-0 and Type-1 couplings which are worst case scenarios observed in *RLC* type of interconnects. Furthermore, the proposed design reduces the power dissipation by reducing switching activity.

The paper is organized in five sections. The present Section 1 introduces to the critical research scenario in VLSI interconnects. Section 2 describes crosstalk and power dissipation expression and their dependency on different parameters. The working of proposed design is discussed in section 3. Section 4 discusses the results obtained for encoder driving *RLC* modeled interconnects. Finally, section 5 draws important conclusions.

## 2. POWER AND CROSSTALK IN *RLC* MODELED INTERCONNECTS

The parasitic capacitance model of an interconnect consists of three parts, the ground capacitance ( $C_G$ ), the fringe or side-wall capacitance to substrate ( $C_F$ ) and coupling capacitance ( $C_C$ ).

Coupling capacitance becomes dominant when adjacent wire tend to switch from 1 to 0 or 0 to 1, resulting in delay penalty which is called crosstalk delay. There are two important effects due to this crosstalk i.e., noise on non-switching wires and increased delay on switching wires.

Assume two lines namely *A* and *B* and their associated capacitances. According to the behavior of neighboring wires, effective coupling capacitance ( $C_{eff}$ ) can be evaluated. Table 1 shows the dependence of effective capacitance of line *A* ( $C_{eff(A)}$ ) on line *B* (assuming line *A* is switching).

Table 1. Dependence of Effective Capacitance of Line ‘A’ on Line ‘B’

Line ‘B’	$\Delta V$	$C_{eff(A)}$	Miller Coupling Factor (MCF)
Switching with ‘A’	0	$C_G$	0
Constant	$V_{dd}$	$C_C + C_G$	1
Switching oppositely with ‘A’	$2 V_{dd}$	$2C_C + C_G$	2

Firstly, it is observed that when both adjacent lines are switching in the same direction the Miller Coupling Factor (MCF) is ‘0’ which indicates that there is no coupling capacitance. Secondly, if one line is switching and the other is quiet then MCF is ‘1’ whose coupling capacitance is greater than the case of MCF=0. Finally, when two adjacent lines are switching in opposite direction then the coupling capacitance is highest (MCF is ‘2’) due to which crosstalk effect becomes dominant. In a data bus there will be adjacent lines to the left and right side of the line. Therefore, various coupling capacitances associated with the 3-bit configuration must be considered. Line *B* is line of interest whereas *A* and *C* are adjacent lines to it. Coupling factor associated with line *B* depends on the switching configurations of lines *A* and *C*.

All possible switching configurations can be classified to Type-0, Type-1, Type-2, Type-3 and Type-4 depending on the value of MCF as shown in the Table 2.

Table 2. Classification of Crosstalk

Type-0	Type-1	Type-2	Type-3	Type-4
---	--↑	-↑-	-↑↓	↑↑↑
↑↑↑	-↑↑	↑-↑	-↓↑	↓↑↓
↓↓↓	↑--	↑-↓	↑↓-	
	↑↑-	↑↑↓	↓↑-	
	--↓	↑↓↓		
	-↓↓	-↓-		
	↓--	↓-↓		
	↓↓-	↓-↑		
		↓↓↑		
		↓↑↑		

↑: switching from 0 to 1, ↓: switching from 1 to 0, -: no transition

In *RC* model, the dominant factor is coupling capacitance, but for *RLC* model, mutual-inductance coupling is considered to be dominant. Mutual-inductance [11, 12] coupling takes worst form when both of the interconnect lines which are adjacent have same transition (i.e., either from 0 to 1 (↑↑) or from 1 to 0 (↓↓)). In this case leftmost aggressor wire induces magnetic field on the victim wire which tends to flow a current that is in opposition to the original current [5, 11]. Thus, crosstalk occurs between the two interconnects which is presently the major design problem in DSM technology. Therefore, the lines switching in the same direction (↑↑ or ↓↓) for *RLC* modeled interconnects generate worst case coupling [12]. Contradictorily, for *RC* interconnects, the worst case crosstalk delay occurs when the adjacent wires switch in opposite direction. However, the worst case pattern is the best case for *RLC* model [5]. Most existing works focus on reducing the effects resulting from coupling capacitance [13] only in the bus structure by introducing bus encoding techniques.

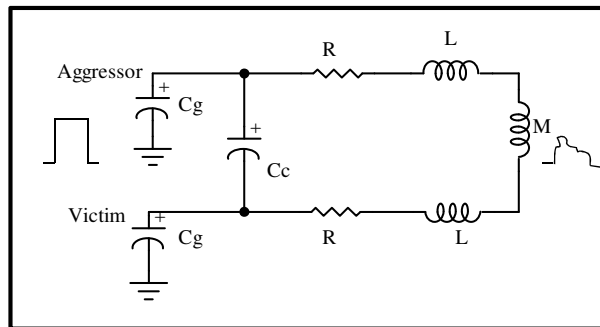


Figure 1. *RLC* equivalent of an interconnect

Power dissipation is expressed as [7]:

$$P = \alpha * V_{dd}^2 * f * C_L \quad (1)$$

where  $C_L$  is load capacitance,  $V_{dd}$  is supply voltage,  $f$  is the clock frequency and  $\alpha$  is the average switching activity which lies between 0 and 1.

For reducing power dissipation in VLSI circuits one or more factors such as  $V_{dd}$ ,  $f$ ,  $C_L$  and  $\alpha$  must be minimized. Here,  $V_{dd}$  and  $f$  are assumed to be already optimized for low power. Therefore, dynamic power dissipation is proportional to the number of signal transition. Symbols and terminologies used throughout this paper are as follows:

$d(t)$ : Bus value at the input of encoder.

$D(t)$ : Encoder output which is transmitted.

$D(t-1)$ : Encoder output which was latched up.

$inv(t)$ : Invert line at the input of encoder which is preset to '0'.

$INV(t)$ : Invert line for the encoded data sent at time  $t$ .

$INV(t-1)$ : Invert line for encoded data sent at time  $t-1$ .

### 3. IMPLEMENTATION OF PROPOSED DESIGN

This section presents proposed encoder and decoder using Bus Invert technique. The results obtained using proposed method is compared with previously published outcomes.

#### 3.1. Proposed Encoder

The proposed encoder is a modified and improved version of the design proposed by Fan *et al.* [7] to reduce crosstalk, delay and power dissipation of *RLC* modeled interconnect instead of *RC* model. In this proposed method, data bus is divided into different clusters, where each cluster contains 4 data bits and one extra control bit. Basically, bus invert method [8, 9] utilizes an extra

control bit i.e.,  $INV(t)$  to differentiate the transmission of original data and inverted data. In this method, if the number of transitions are more than half of the size of bus width, then original data is inverted and control line ( $INV(t)$ ) is set to 'high' whereas in other case original data is transmitted with  $INV(t)$  at logic 'low'.

The block diagram of proposed encoder is shown in Fig. 2 [10]. The 5-bit bus encoder architecture is composed of inverter, CNT0, CNT1\_1, CNT1\_2, 2-bit comparator, XOR stack and latch. CNT0 and CNT1 (CNT1\_1 and CNT1\_2) are crosstalk modules used to count Type-0 and Type-1 couplings respectively. Two type-1 counters viz., CNT1\_1 and CNT1\_2 are used which counts the number of type-1 couplings with original data and inverted data respectively. Brief description of the block diagram is as follows.

The data to be transmitted ( $d(t), inv(t)$ ) through encoder is simultaneously inverted to obtain ( $\overline{d(t)}, \overline{inv(t)}$ ) as shown in Fig.2. Here the value of  $inv(t)$  in the data to be transmitted is assumed to be at logic 'low' initially. Now, the original data ( $d(t), inv(t)$ ) and the previously latched data ( $D(t-1), INV(t-1)$ ) are fed as inputs to CNT0 and CNT1\_1 counters. The outputs of CNT0 (1 bit) and CNT1\_1 (2 bits) are  $N0$  and  $K_1K_0$  respectively. The inverted data ( $\overline{d(t)}, \overline{inv(t)}$ ) and the data stored ( $D(t-1), INV(t-1)$ ) are fed as inputs to CNT1\_2 whose output (i.e., of 2 bits) is  $L_1L_0$ . The counts of two type-1 counters are compared in 2-bit comparator. The inputs of 2-bit comparator are  $K_1K_0$  and  $L_1L_0$  (which are having 2-bits) whereas the output of the comparator is  $N1$ (1-bit). Next,  $N0$  and  $N1$  are fed as inputs to an OR gate whose output is  $INV(t)$ . This  $INV(t)$  and the original data ( $d(t), inv(t)$ ) are given as inputs to XOR stack. The output of XOR stack can be inverted data (if  $INV(t)$  is '1') or the original data (if  $INV(t)$  is '0'). The output of the XOR stack is the encoded data ( $D(t), INV(t)$ ) which is finally fed to interconnects. This encoded data is stored in latch for one clock cycle ( $D(t-1), INV(t-1)$ ), after which it is fed back for comparison with ( $d(t), inv(t)$ ). Finally, at the receiving side, decoder retrieves the original data with the help of  $INV(t)$  line.

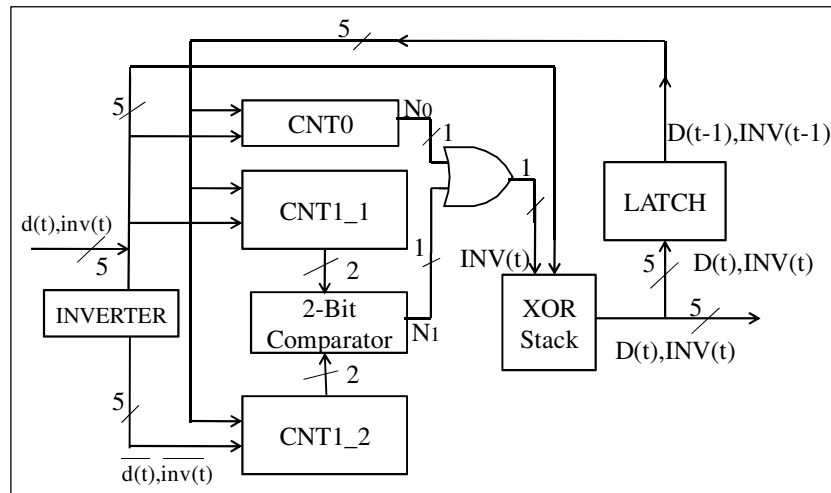


Figure 2. Block diagram of 5-bit bus encoder

**CNT0:** Type-0 coupling occurs if three adjacent lines have the same transition (i.e.,  $\uparrow\uparrow\uparrow$  or  $\downarrow\downarrow\downarrow$ ). CNT0 counts the number of type-0 couplings whose internal circuit diagram is shown in Fig. 3. There are two type-0 couplings (one is of 'low to high' transition and the other is of 'high to low' transition) which can be merged to only one coupling. As 'low to high' transition ( $\uparrow$ ) and 'high to low' transition ( $\downarrow$ ) are detected separately, it is concluded that there is only one type-0 coupling. First, the design checks the occurrence of transition by using level-1 AND gates. The top five AND gates detect 'high to low' transition whereas bottom five will detect 'low to high' transition. A 'high' logic is present at output if there is a transition (if not logic 'low' is present). The output signals from level-1 AND gates  $S_a, S_b, S_c, S_d, S_e$  ('high to low' transition) signals are grouped into

three different combinations as  $(S_a S_b S_c, S_b S_c S_d, S_c S_d S_e)$ . These signals are fed to three different AND gates to detect  $\downarrow\downarrow\downarrow$  condition as shown in Fig.4. Similarly, the output signals of ‘low to high’ detector  $(S_f S_g S_h S_i S_j)$  are given to another set of AND gates to detect  $\uparrow\uparrow\uparrow$  condition. Finally, all these signals are fed to OR gate, whose output ( $No$ ) becomes ‘high’ if any one of the combination satisfies the type-0 coupling condition.

**CNT1\_1:** Type-1 coupling occurs when one or two lines are having transition in the same direction while the rest (i.e., remaining two or the third one respectively) are idle. There are eight conditions of type-1 coupling which can be placed in two different groups with each group having four switching conditions that depends on high to low and low to high transitions. CNT1\_1 counts the number of type-1 couplings with original data whose circuit diagram is shown in Fig.4. Level-1 AND gates of CNT1\_1 detects the transitions as discussed in the above section. The outputs of level-1 AND gates are fed to OR gates. Type-1 coupling occurs when the first line is having transition and third line is idle and vice-versa, which clearly assures that these lines, must be inserted as inputs to an XOR gate to verify this condition. These five OR gate outputs are divided into 3 groups i.e.,  $m_0$  and  $m_2$ ;  $m_1$  and  $m_3$ ;  $m_2$  and  $m_4$  which are fed to three different XOR gates. The outputs of these three XOR gates should be added using a full adder. This method implements the full adder using two half adders and an OR gate and output of the full adder represents the number (as there are four in number two bits are sufficient to represent the count) of Type-1 couplings  $K_1 K_0$ .

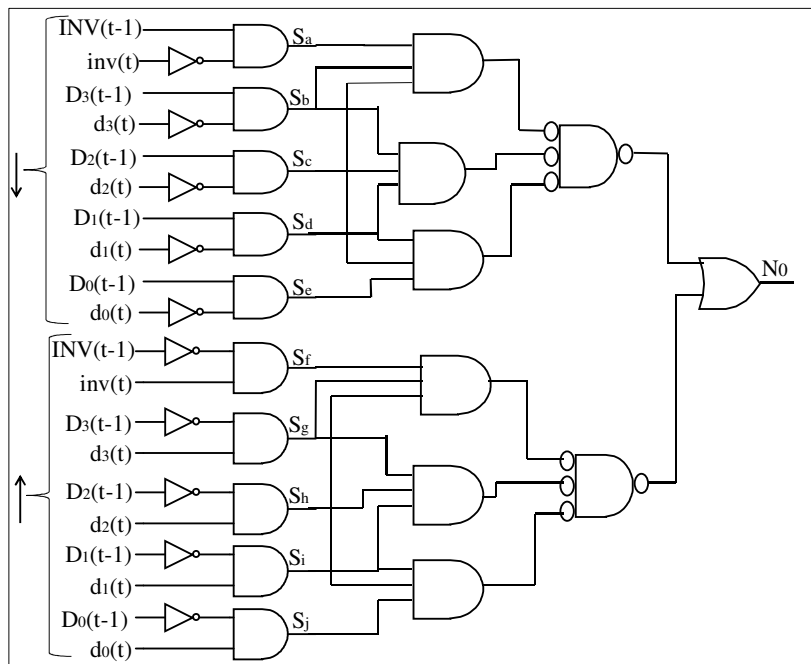


Figure 3. Circuit diagram of CNT0

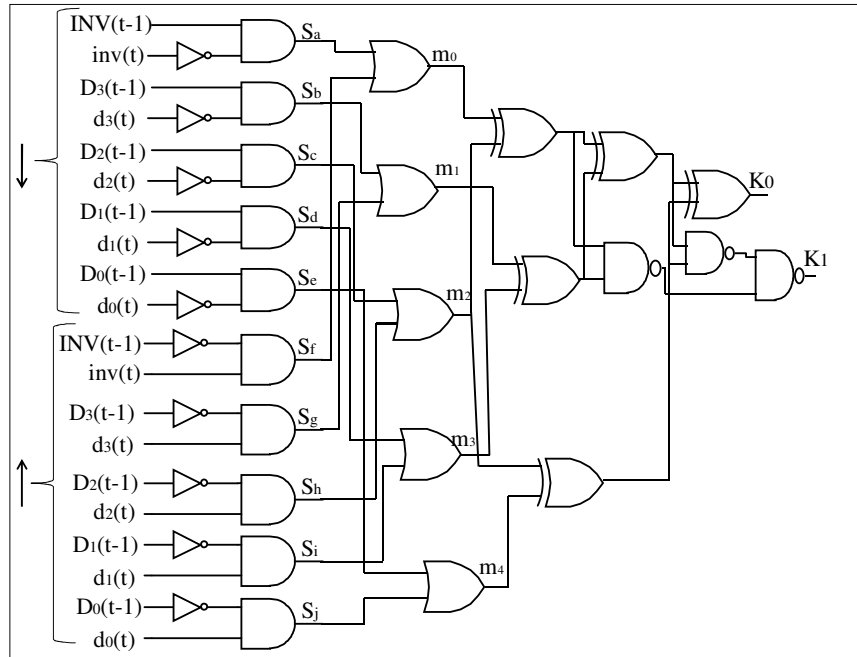


Figure 4. Circuit diagram of CNT1\_1

**CNT1\_2:** CNT1\_2 counter counts the number of type-1 couplings with the inverted data. The inputs of CNT1\_2 are  $(\overline{d}(t), \overline{inv}(t))$  and  $(D(t-1), INV(t-1))$  whereas the output is  $L_1L_0$ . The circuit diagram of this counter is shown in Fig.5.

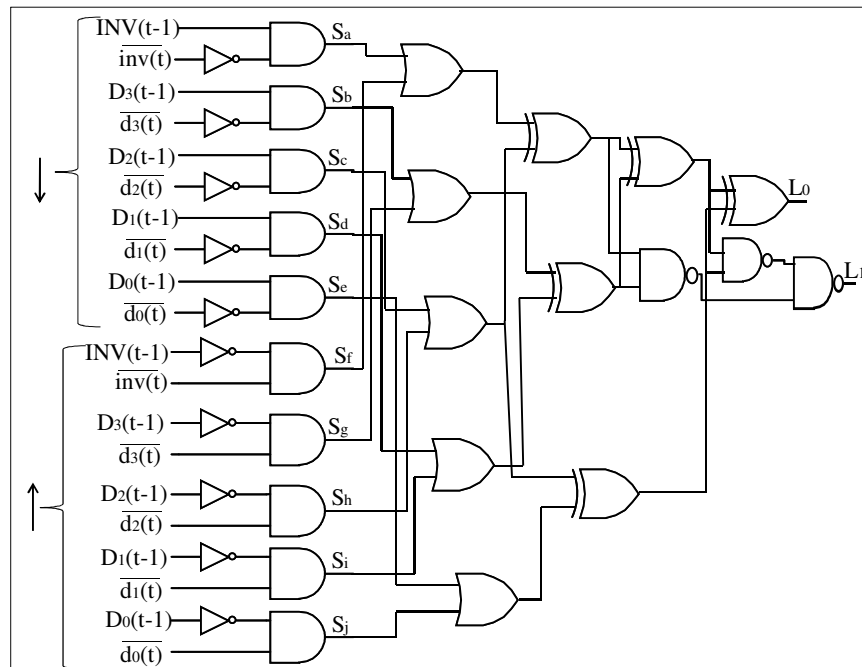


Figure 5. Circuit diagram of CNT1\_2

**2-Bit Comparator:** The next block is a 2-bit comparator which compares the count of two type-1 counters (i.e., CNT1\_1 and CNT1\_2). The internal logic diagram is shown in Fig.6. After comparing  $K_1K_0$  and  $L_1L_0$ , it generates an output  $NI$  as logic 'high' when the count of CNT1\_1 is

greater than CNT1\_2 whereas logic 'low' in the converse situation. The output of 2-bit comparator is fed as one of the input of the OR as shown in the block diagram (Fig.2).

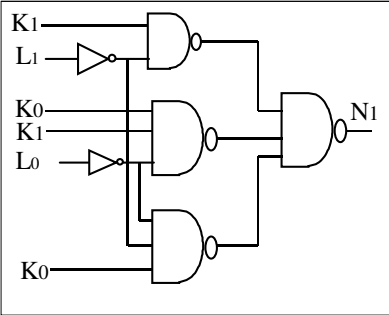


Figure 6. The 2-bit comparator

**XOR Stack:** When either of  $N1$  or  $N0$  is 'high', the output of OR gate i.e.,  $INV(t)$  becomes 'high' indicating a Type-1 or Type-0 switching condition. The truth table of XOR stack is shown in Table 3. The original data is transmitted only if both  $N1$  and  $N0$  are 'low'. For all other cases inverted data is transmitted to eliminate crosstalk.

Table 3. Truth table of XOR stack

$N1$	$N0$	OR gate output $(INV(t))$	Encoded Data $(D(t), INV(t))$
0	0	0	$(D(t), 0)$
1	0	1	$(\overline{D(t)}, 1)$
0	1	1	$(\overline{D(t)}, 1)$
1	1	1	$(\overline{D(t)}, 1)$

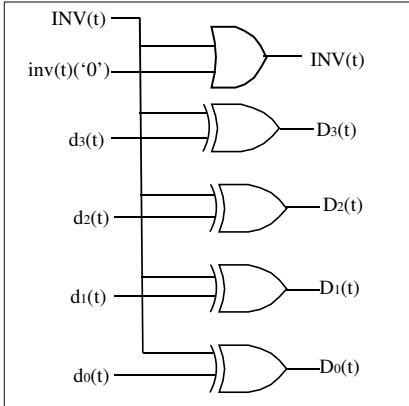


Figure 7. XOR Stack

Both XOR stack and decoder uses XOR gates which is having a property of transmitting the input directly if the other input is 'low' and on contrary transmitting complemented input if the other input is 'high'. The circuit diagram of XOR stack is shown in Fig.7. The data bit is fed as one of the input and control line  $INV(t)$  is given as other input for the 2-input XOR gate. If the  $INV(t)$  line is 'high' then it indicates that the inverted data must be transmitted to avoid the crosstalk and if it is 'low' then original data is to be transmitted.

**Latch:** As proposed design is comparing the present data with the previously transmitted data there is a necessity for storing the previously transmitted data. For this purpose latches are necessary that are implemented using transmission gates [14,15].

### 3.2 Decoder

The decoder is used to decode the encoded data. Encoded data  $D(t)$  and control line ( $INV(t)$ ) fed to 2-input XOR. If  $INV(t)$  line is 'high' then it indicates that inverted data has been transmitted and so decoder inverts  $D(t)$  to obtain original data. If it is 'low' indicating transmission of original data, decoder transmits the data without any inversion.

## 4. RESULTS

The proposed encoder is simulated to find power dissipation and propagation delay of the bus codec. Simulation results were obtained using H-SPICE in 0.18, 0.13, 0.09 and 0.07 $\mu$ m technologies. Although internal diagrams of encoder has been shown for only 4-bit, the model is also extended to 8-bit and 16-bit using shielding method.

The power dissipation and crosstalk delay of the circuitry (Encoder, Interconnects and Decoder) are obtained. Total power dissipation includes the power dissipated in encoder, interconnects and decoder (i.e.  $P_{enc} + P_{dec} + P_{interconnect}$ ).  $P_{D,coded}$  is the dynamic power dissipation (which depends on the switching activities of the data) of the encoded data. For 0.18 $\mu$ m technology, when the load capacitance is lesser than 0.1pF/bit, then coding method consumes more power than un-coded method. But as the load capacitance is increased i.e., beyond 1.5pF/bit, then coded data consumes lesser power than the uncoded data. Using proposed design for a load capacitance of 4pF/bit, a reduction in power dissipation ranging from 33.2% to 42.6% is achieved.

The crosstalk effect is reduced by inverting the original data and which in turn also reduces the switching activity. Here, the proposed method reduces both the Type-0 and Type-1 coupling. Type-0 and Type-1 coupling is caused in two and eight cases respectively. Therefore, switching activity reduces by 40.7% which is substantially more as compared to Fan *et al.* [7].

The proposed method greatly reduces the chip area by reducing number of transistors in comparison to Fan *et al.* [7] (Table 4). By reduction in chip area the complexity of circuit is also reduced by more than 25%.

Table 4. Comparison of proposed model with Fan *et al.* [7]

Component	Fan <i>et al.</i> [7]	Proposed Method
AND gate	4-input	2-input
6-bit adder	2	0
CNT0	2	1
XOR gate	18	8
Total no. of transistors	664	472

The encoder proposed by Fan *et al.* [7] uses four input AND gates whose input capacitance is very high and which in turn increases the propagation delay also. However, the proposed design uses only 2-input AND gates in majority (except for just six number of 3-input NAND gates) which effectively reduces the encoder propagation delay. Moreover, Fan *et al.* [7] design uses two 6-bit adders comprising of four full adders and four half adders thus making the circuit bigger and complex which results in longer delay and higher power dissipation.

#### A. Total Power Reduction

Total power dissipated by the system includes the power dissipated by encoder, decoder and interconnects. The total power dissipated for different technology nodes and bus width is shown in Table 5. It is observed that as feature size reduces for same bus width, the overall power dissipation also reduces. However, for same technology node, power dissipation increases with rise in data width.



Table 5. Power dissipation for different technology nodes and bus widths

Technology ( $\mu\text{m}$ )	Power Dissipation ( $\mu\text{W}$ )		
	4 bit	8 bit	16 bit
0.18	21.426	44.127	86.954
0.13	10.243	19.547	37.684
0.09	7.418	15.214	29.298
0.07	5.854	10.642	21.786

### B. Total Propagation Delay Reduction

Propagation delay on a victim line increases with crosstalk. The encoder that is used to reduce crosstalk, also introduces some delay itself. Although there is a reduction in the propagation delay with the reduction of crosstalk, the overhead delay due to encoder should also be considered. The propagation delay introduced by the proposed design is shown in Table 6. The delay is caused by the whole circuit (encoder + interconnects + decoder). It is observed that as technology goes on shrinking, the overall delay increases, which therefore acts as a trade off parameter for the power dissipation. However, the overhead delay introduced by proposed design is lesser compared to other designs.

Table 6. Propagation Delay of worst case for different technologies

Technology ( $\mu\text{m}$ )	V <sub>DD</sub>	Propagation Delay (ps)
0.18	1.8	1658
0.13	1.5	2135
0.09	1.2	2536
0.07	1	2764

## 5. CONCLUSIONS

This paper demonstrated a reduction in power dissipation, total propagation delay and crosstalk for *RLC* modeled interconnects by using low complexity encoder. This encoder consumes very less power compared to the existing encoders which are being used for crosstalk avoidance. The results show a reduction of 100% in Type-0 and 82.8% in Type-1 couplings. The encoding system consumes 21.496 $\mu\text{W}$ , 44.127 $\mu\text{W}$ , 86.954 $\mu\text{W}$  power for 4-bit, 8-bit and 16-bit line codec system respectively in 0.18 $\mu\text{m}$  technology. This codec system works upto 1GHz frequency without any problem. However, beyond this frequency there is a necessity to use a high speed latch for feedback.

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