HIGH SPEED CONTINUOUS-TIME BANDPASS ΣΔ ADC FOR MIXED SIGNAL VLSI CHIPS

P.A.HarshaVardhini[1] and Dr.M.MadhaviLatha[2]

[1]Ph.D Scholar, Dept. of ECE, J.N.T.U, Hyderabad, A.P, India.
pahv19@rediffmail.com
[2]Professor and Head, Dept. of ECE, J.N.T.U, Hyderabad, A.P, India.
mlmakkena@yahoo.com

ABSTRACT

With the unremitting progress in VLSI technology, there is a commensurate increase in performance demand on analog to digital converter and are now being applied to wideband communication systems. sigma Delta (ΣΔ) converter is a popular technique for obtaining high resolution with relatively small bandwidth. ΣΔ ADCs which trade sampling speed for resolution can benefit from the speed advantages of nm-CMOS technologies. This paper compares various Band pass sigma Delta ADC architectures, both continuous-time and discrete-time, in respect of power consumption and SNDR. Design of 2nd order multi-bit continuous time band pass ΣΔ modulator is discussed with the methods to resolve DAC non-idealities.

KEYWORDS

CMOS, Over sampling, Noise shaping, Sigma Delta Modulation, Bandpass ΣΔ modulator, Dynamic element matching, Data weighted averaging.

1. INTRODUCTION

As mixed signal VLSI technologies rapidly advance, complexity of implementing signal processing functions is drastically increased and a larger microelectronic system is integrated into a single IC chip. Every design engineer is challenged to develop products that are more power efficient by reducing power consumption and extending battery life in portable multimedia systems. ADCs are one of the most essentially used mixed signal functions creating an interface between sensing and actual devices in the industrial control, transportation, consumer electronics and conversion of analogue voice and video data in the computing and communication communities.

In the last two decades, two architectures of CMOS ADCs are monopolizing most of the applications where medium/high precision is required. One is sigma delta (ΣΔ) ADC based on the oversampling and noise confirmation. Another is the pipeline architecture based on the subdivision in the cascade of conversion process. In control applications, the trend is towards medium speed (10-100KHz) and high resolution (>16 bits). In communication application trends are similar but dynamic performance tends to be critical, especially in voice processing applications. Consumer goods are another important application where high conversion speed (upto 100's of MHz) and low-medium resolution (~8 to 12bits) is the norm[1]. A ΣΔ ADC is able to deliver very high resolutions (16 bits-24 bits) with high accuracy, because most of its

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complexity is in the digital filter, and only a coarse single-bit conversion is performed i.e. the circuit is less susceptible to noise.

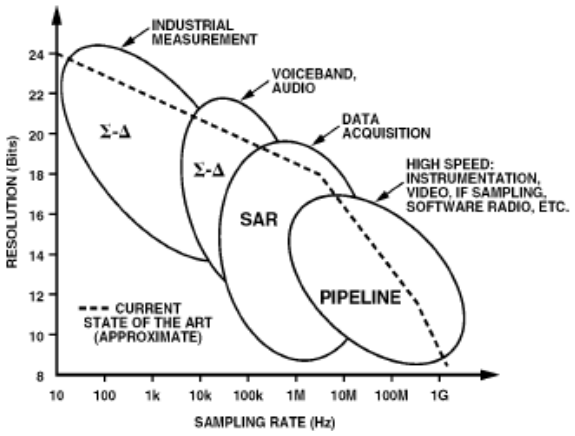

Fig.1 ADC architectures state-of-art.

With the continuing scale down of CMOS technology feature size with architectural advances and ever increasing operation speed ΣΔ ADCs work at higher frequencies up to several hundred to few Gs/s nyquist rate. The resolution of Sigma-Delta type converters can be very good compared to other ADC converters of similar complexity as in figure 1. ΣΔ ADCs which trade sampling speed for resolution can benefit from the speed advantages of nm-CMOS technologies.

Section II of this paper reviews the oversampling and noise shaping techniques. ΣΔ ADC architectures are then described in section III followed by the design of band pass ΣΔ ADC and state-of-art band pass ΣΔ ADCs in section IV. Section V concludes the paper.

2. OVER SAMPLING AND NOISE SHAPING

2.1. Oversampling

ΣΔ ADC implement an oversampling approach with a much higher sampling frequency of the analog input voltage than the achieved multi-bit output rate. Oversampling occurs at a sample rate $f_S > 2\ f_o$ ($2f_o$ being the Nyquist rate or minimum sampling rate for signals band limited to f_o).

Increasing the sampling rate ensures the benefits:
1. The transition band of the analog filter preceding the digitizer is now much wider, providing an opportunity for a drastic reduction in circuit complexity. In ΣΔ converter, filter is as simple as a mere RC stage.
2. The quantization noise is now spread over a wider band

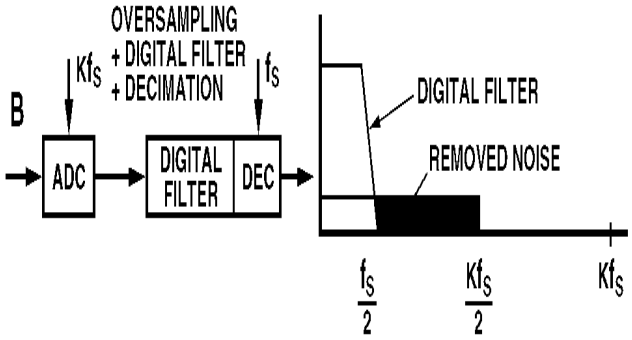

Fig.2 Effect of increasing sampling frequency

As in figure 2, as the sampling frequency is increased by a factor, K, (the oversampling ratio), but the input signal bandwidth is unchanged. The quantization noise falling outside the signal bandwidth is then removed with a digital filter. The output data rate can now be reduced (decimated) back to the original sampling rate, f_S. This process of oversampling, followed by digital filtering and decimation, increases the SNR within the Nyquist bandwidth (dc to f_S /2). For each doubling of K, the SNR within the dc-to- f_S /2 bandwidth increases by 3 dB. Due to this oversampling operation of ΣΔ ADCs, the sampling frequencies are in the order of GHz.

2.2 Noise Shaping

Noise shaping is a technique typically used in digital audio, image, and video processing, usually in combination with dithering, as part of the process of quantization or bit-depth reduction of a digital signal. Basic ΣΔ architecture as in figure 3, shape the quantization noise so that most of it occurs outside the bandwidth of interest, thereby greatly increasing the SNR in the dc-to f_S/2 region.

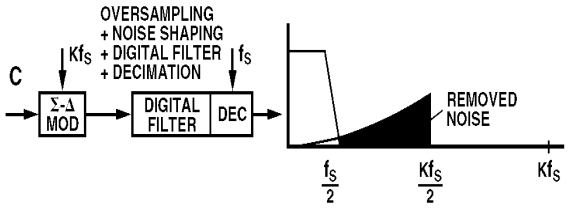

Fig .3 Noise shaping with ΣΔ Modulator

2.3. Advantages of oversampling and noise shaping

Dynamic range (DR) increase by a value of 3 dB for every doubling of the sample rate which means that extra dynamic range can be obtained by spreading the quantization noise power over a larger frequency range. Noise shaping through the use of feedback can be used at increased sampling rates to obtain higher DR improvements[2].

Oversampling improves signal to noise ratio (SNR). Straight oversampling gives an SNR improvement of 3 dB /octave or equivalently 0.5 bits/octave. A measure of this oversampling is oversampling ratio (OSR) and doubling OSR (i.e. sampling at twice the rate) decreases the quantization noise power by one-half or 3 dB /octave or 0.5 bits/octave. Using high OSRs can relax the clock jitters.

3. SIGMA-DELTA ADC ARCHITECTURES

Sigma-Delta analog to digital converter ease analog-circuitry requirements at the expense of more complex digital circuitry. These converters are ideal for mixed-mode IC fabrication processes. Over sampling and noise shaping benefits relaxed analog- filter requirements and quantization noise reduction, which makes ΣΔ modulators attractive and useful for many single-chip receiver applications.

3.1. Continuous-time versus Discrete-time

Continuous-time (CT) ADCs gain growing interest in wireless applications for their lower power consumption and wider input bandwidth as compared with the discrete-time (DT) counterparts. In contrast with CT converters, DT ΣΔ converters are more accurate and achieve higher dynamic range. However, CT converters allow high speed operation while keeping power consumption and chip area low [3, 4].

3.2. Single loop versus cascaded

The single-loop uses one quantizer and a D/A converter along with a series of integrators while the multi-stage consists of a cascade of single-loop ΣΔ modulators. High order single-loop architectures suffer from potential instability owing to the accumulation of large signals in the integrators**.** Cascade architectures use combinations of inherently stable low order single loops to achieve higher order noise-shaping, but the constraints on circuit imperfection and mismatch will be more severe with the capability of achieving wider bandwidths for given sampling frequency [5]. Single loop architecture can achieve sampling frequencies in the GHz range as it does not require a high speed digital noise cancelling filter and the dc gain requirement of the op-amps in the single-loop architecture is more relaxed. Both architectures can employ either single-bit or multi-bit quantizers and combined D/A converters.

3.3. Single-bit versus Multi-bit

Single-bit oversampling converters have the advantage that they can realize highly linear data conversion but it results in a large amount of out-of-band quantization noise, which must be significantly attenuated using the analog circuitry. The use of a multi-bit D/A converter can significantly reduce the quantization noise, but care must be taken to ensure that the multi-bit converter remains linear. One approach for realizing a multi-bit D/A converter intended for oversampling systems is that of dynamic element matching (DEM).

Unfortunately, single-bit single-stage ΣΔ modulators are potentially unstable systems. Thus the design of their loop filter is a non-trivial task. Due to the stability considerations, the SNR improvement as the modulator order increases is diminished for increasing orders. The single-stage modulators are quite immune to coefficient errors; such tolerated errors have been reported to be larger than 5% [8]. On the other hand, the sensitivity of single-bit single-stage ΣΔ modulators to analog circuit imperfections is considerably reduced compared to their multi-stage counterparts.

3.4. Feedback versus feedforward

Feedforward architecture with one DAC requires a high speed summation node which introduces a parasitic pole at the loop filter output as in figure 4a. Feedback architecture have better anti-aliasing filter but requires n-DACs where n is the order of the filter as in the figure 4b. Both feedback and feedforward architectures are used in high speed ΣΔ ADCs.

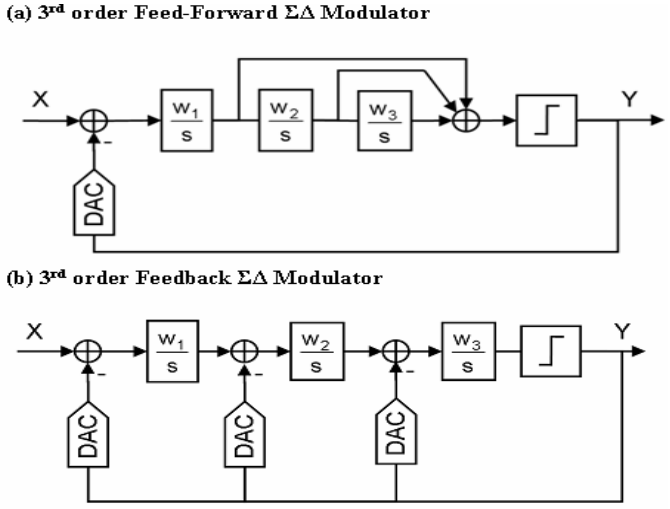

Fig.4 ΣΔ ADC a) with feed-forward structure b) with feed back structure.

4. DESIGN OF BANDPASS ΣΔ ADC

The block diagram of first order ΣΔ ADC is as shown in figure 5. The notch frequency is independent of the sampling clock frequency as a CT filter is used in the band pass converter. The band pass filter removes the signal frequencies above the tuning frequencies because of the CT character of the filter. A CT modulator samples the input signal after the loop filter at the quantizer where feedback will shape noise and distortion out of the desired signal bandwidth. Having the loop filter precede the sampling has the additional benefit of providing intrinsic anti-alias filtering.

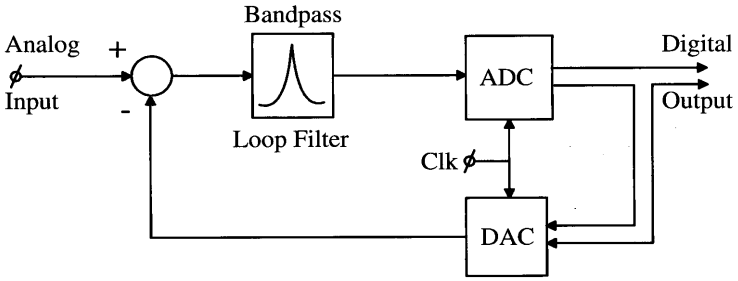

Fig.5 First order Band pass ΣΔ ADC architecture

Figure 6 shows ΣΔ modulator architecture with multi-bit quantization which offers an attractive balance of complexity and performance. In this architecture only two analog integrators are required such that power consumption can be minimized. The use of multi-bit quantization also allows for aggressive noise shaping to be performed beyond the stability limitations of a single-bit design. The signal transfer function (STF) and the quantization noise transfer function (NTF) exhibits a low-pass response and a band stop response respectively due to the feedback coefficient which allows for second-order anti-alias filtering to be achieved while retaining the band stop characteristics of a band pass modulator. Table I reviews few published continuous time band pass ΣΔ ADCs for the 1995-2010 period where we can conclude that multi-bit ΣΔ loops are preferred for bandwidth demanding applications.

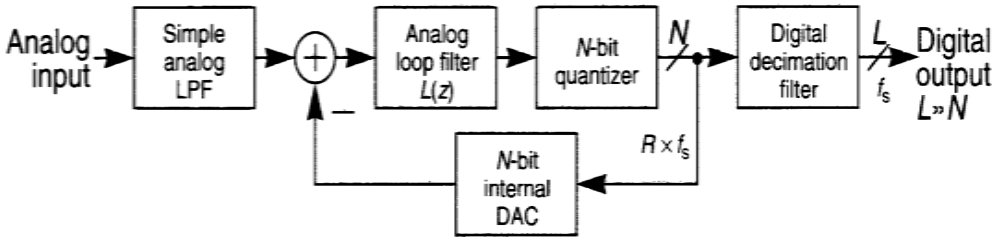

Fig. 6 Multi-bit ΣΔ ADC architecture

4.1. Integrator

There are several integrator choices available which would meet the low power targets of the design including g_mC, MOSFET-C, and active-*RC*. Active-RC integrators provide good linearity when compared to g_mC or MOSFET-C integrators as the passive resistors are inherently linear [9]. The g_mC based integrators are easily tunable and can achieve high unity gain frequency, but these integrators are sensitive to the parasitic capacitances and the non-linear voltage-to-current conversion limit the linearity of the integrator. In a continuous-time modulator, high sample rates can be achieved, as the integrators are not limited by charge transfer accuracy requirements. In a modulator employing active-*RC* integrators, the amplifier gain- bandwidth need only exceed the signal bandwidth for purposes of providing enough loop gain to maintain linear operation.

Table 1. STATE-OF-THE-ART BAND PASS ΣΔ MODULATORS

Year	Ref	Order/ Archi-tecture	Technology	Supply Voltage (V)	Sampling frequency	Band width	SNDR (dB)	Power
2010	17	6-CT	0.18µm CMOS	1.8	800 MHz	10 MHz	68	160mW
2008	15	4-DT	0.18µm CMOS	1.8	40 MHz	0.31 MHz	82-71	115mW
2008	16	2-DT	0.18µm CMOS	1.8	60 MHz	1 MHz	65.1	16 mW
2007	14	2-CT	0.13µm CMOS	1.2	160 MHz	5 MHz	34.3	720 µW
2007	22	4-CT	SiGe BiCMOS	2.5	40 GHz	500 MHz	55	1.6 W
2007	6	4-CT	SiGe BiCMOS	1.25	3.8 GHz	1 MHz	59*	75 mW
2006	18	2-CT	0.25µm CMOS	2.5	320 MHz	20 MHz	53.5	32 mW
2006	21	4-CT	HBT	5	4 GHz	180 MHz	40	7.7W
2005	7	2-CT	0.25µm CMOS	1.2	40 MHz	1.25 MHz	89	44 mW
2004	8	4-CT	Inp HBT	5	4 GHz	60 MHz	47.7	3.5 W
2003	10	2-CT	0.18µm CMOS	1.8	48 MHz	1.5-2.5MHz	61	2.2mW
1998	12	3-DT	0.5µm CMOS	0.9	1.538MHz	16 KHz	62	12 mW
1997	19	4-CT	HBT	5	4 GHz	62.5 MHz	44	1.4W
1996	11	2-DT	1.2µmBiCMOS	5	42.8 MHz	200 KHz	46*	30 mW
1995	13	2-DT	0.8µmBiCMOS	5	42.8 MHz	200 KHz	57*	60 mW

* indicates SNR in dB

4.2. Comparator or Quantizer

The purpose of the comparator in a sigma delta modulator is to quantize a signal in the loop and provide the digital output of the modulator. The performance of the sigma delta modulator is relatively insensitive to offset and hysteresis in the comparator as the two level quantizer, because the effects of these impairments are attenuated in the baseband by second order noise shaping that can be filtered by decimation filter [14]. A multi-bit quantizer also reduces the effect of clock jitter in CT ΣΔ ADC.

4.3. DAC

The feedback path in the ADC is implemented by a high-speed DAC which translates the digital output into a continuous time current. Careful implementation of DAC is critical in ΣΔ modulators since nonlinearities, offsets and noise introduced in the feedback are not shaped away from the signal passband. There are two popular DAC implementations: 1) the tri-state DAC and 2) a current steering DAC.

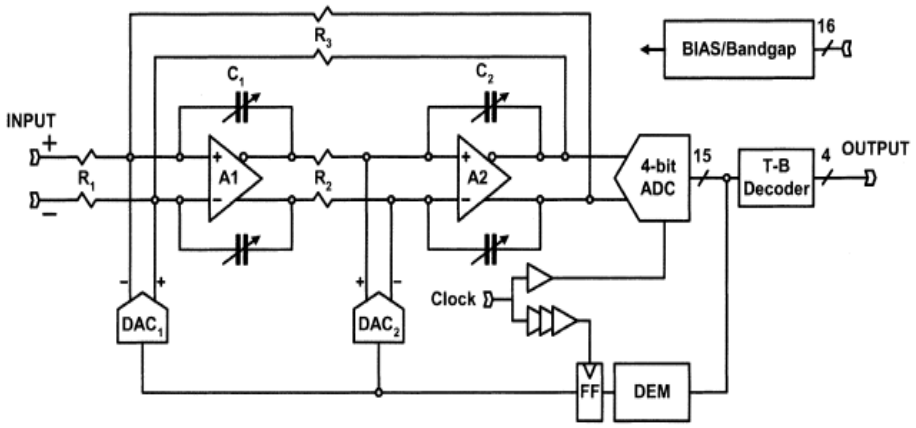

Fig. 7 Second order Continuous time ΣΔ modulator implementing DEM

4.4. DAC architectures for improved linearity

For a high-speed modulator with MHz range input signal, low oversampling ratios are a must for a reasonable high clock frequency. In such cases, a multi-bit quantizer is needed to lower the quantization noise, improve the loop stability and reduce the clock jitter sensitivity for CT ΣΔ modulators. The multi-bit quantizer also means a multi-bit DAC in the feedback path. Problems can occur in ΣΔ modulators because of the non-ideal operation of the local DAC. These depend on whether the ΣΔ modulator is single-bit (when single-bit DAC is used) or multibit (when the local DAC is multibit). Problems arising from the component inaccuracies, like the resistor or capacitor values of the local DAC, may degrade the performance of multi-bit modulators in particular .

Multi-bit DACs results in reduced quantization noise, improved dynarnic range, de-correlated quantization noise spectrum for the input signal, and irnproved stability. Furthermore, the multi-bit output also complicates the digital low-pass filter following the modulator. A multi-bit DAC can utilize the principle of noise shaping to reduce its nonlinearity effects. The procedure of suppressing the mismatch error is the same as that of sigma-delta data conversion: use filtering to suppress the noise spectrum in the signal band and to shift its power to out-of-band frequencies.

There are two signal-processing techniques to enhance the linearity of multi-bit sigma-delta modulators due to DAC element mismatch, dynamic element matching (DEM) and digital calibration. The digital calibration schemes are usually expensive to implement in terms of system design complexity, hardware requirement, and power consumption. The dynamic element matching (DEM) is the most extensively used technique to reduce the DAC mismatch error. DEM is used to randomize or noise shape the mismatch-induced distortion out of band. DEM method is quite attractive and various techniques have been developed for many applications like: i) Dynamic Element Randomization, ii) Dynamic Element Rotation-Barrel Shifter, iii) Individual Level Averaging (ILA), iv) Noise-Shaped Element Usage, v) Data Weighted Averaging (DWA). ILA is more effective for a smaller number of elements while DWA method works well for 7 or more elements [23]. DWA is widely employed DEM algorithm for its simple implementation and good performance for various applications. Figure 7 shows a second order CT ΣΔ modulator implementing DEM algorithm in the feedback loop. DWA reduces the hardware complexity [24].

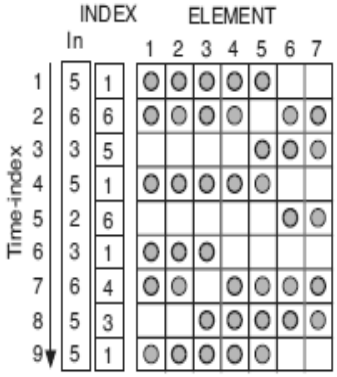

Fig 8 Illustration of DWA – DEM algorithm

DWA uses all the DAC elements at the maximum possible rate while ensuring that each element is used the same number of times. The unit elements participating in the D/A conversion are selected sequentially from the DAC array, beginning with the next available unused element, as it is shown in figure 8. Through such rotational element-selection process, DWA achieves first order high-pass shaping of the DAC mismatch errors. The DAC errors will quickly sum to zero, moving distortion to high frequencies. Besides, compared with other algorithms, DWA algorithm preserves the modulator noise shaping.

5. CONCLUSION

High Speed ΣΔ ADCs in the GHz frequency range designed with nm-CMOS lowers the manufacturing cost and enables additional digital functionality compared to HBT and SiGe process. Band Pass ΣΔ converters seem interesting in all kind of radio applications such as AM/FM radio, GSM, UMTS, Software defined radios. Continuous time higher order multi-bit ΣΔ architecture achieves higher resolution, less clock jitter sensitivity with improved DAC linearity. CT ΣΔ modulators are suited for a low-cost integration because they provide anti-aliasing filtering without silicon-area penalty and can potentially operate with less power consumption than DT implementation and the single loop topology is preferable in low-voltage, low-power designs.

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Authors

P.A. Harsha Vardhini, presently pursuing her Ph.D from JNTU, Hyderabad. Her research interests are in the areas of Mixed signal VLSI Design, Integrated Circuits, Wireless Communication. She has 4 publications in various international journals and conferences.

Dr. M.Madhavi Latha, Professor and Head of Dept. of ECE, JNTU, Hyderabad. Her research interest includes Signal & Image Processing using wavelet transforms, Low Power Mixed Signal Design in VLSI. Specialized in signal and image processing using wavelet. She has 32 publications in various journals and conferences at national and International level and presented papers in conferences held at Lasvegas, Lousiana, USA and Austria. She has conducted Ten UGC refresher Courses and in DSP, VLSI & Embedded systems, workshops in EDA Tools for VLSI, CMOS & ASIC Designs, MATLAB Programming & Applications