FPGA Implementation of ADPLL with Ripple Reduction Techniques

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ABSTRACT

In this paper FPGA implementation of ADPLL using Verilog is presented. ADPLL with ripple reduction techniques is also simulated and implemented on FPGA. For simulation ISE Xilinx 10.1 CAD is used.Vertex5 FPGA (Field Programmable Gate Array) is used for implementation. ADPLL performance improvement, while using ripple reduction techniques is also discussed. The ADPLL is designed at the central frequency of 100 kHz. The frequency range of ADPLL is 0 kHz to 199 kHz. But when it is implemented with ripple reduction techniques, the frequency range observed is from 11 kHz to 216 kHz.

KEYWORDS*: DCO, ADPLL, LOOP FILTER, PHASE DETECTOR*

1. INTRODUCTION

ADPLL is modified form of phase locked loop (PLL).It consists of digital blocks only. It tracks the signal frequency. PLL uses negative feedback concept to make both frequency equal. For locked state PLL has small phase error or zero phase error but exactly the same frequency [1]. As it takes binary signal as input so it can easily implemented on FPGA [3], [5], [6] .It offers many advantages. It has less market cost. It consumes very less power. ADPLL can be used in clock distribution and generation for processors [4]. The first ADPLL was reported in 1980 [12] .With use of 74HC297 IC [3] a modified form of ADPLL is developed. In this design a new digital controlled oscillator (DCO) is developed. This gives very good phase a frequency error tracking that was not implemented with 74HC297 IC. Clock recovery is most important use of ADPLL [7]. Data may affect with noise that noise is called ripple. For reducing ripple in the ADPLL circuit ripple reduction techniques are also reported in different research papers [1], [9], [10], [11].

An example of an ADPLL is implemented [1]. All the components of ADPLL are fully digital. Verilog HDL is used to design an ADPLL. HDL is very flexible for modifying the design parameters. To implement the design 10.1 version of Xilinx is used .To reduce ripple a new ADPLL structure is implemented [1]. Both design of ADPLL is implemented on to FPGA. Linear ADPLL was implemented on FPGA [6]. Recently an all-digital phase-locked loop (ADPLL) having a fault detection of the input reference signal was modelled in Verilog hardware descriptive language (HDL) [7].

This paper is organized as follows: In section 2 we give a brief overview of the ADPLL design. Section 3 describes the ADPLL implementation with ripple reduction techniques. This section

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also presents the Xilinx simulation results. In section 4, the FPGA results have been discussed. Finally, in the section 5 we conclude the research work presented in this paper.

2. ADPLL DESIGN

Figure1 shows the elemental diagram of ADPLL.ADPLL blocks are: 1) Phase detector 2) Loop filters 3) Digital Controlled Oscillator. First component phase detector works as a phase comparator. Phase detector checks phase error among signals produces an error pulses. In our design EXOR gate is used as phase detector (PD).This type of PD produces an error pulses on both the edges. EXOR gate maintain phase tracking in the range of [90,-90] degree [1].

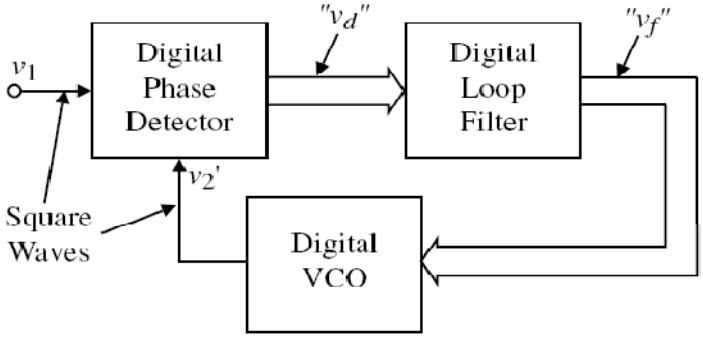

Figure 1. The basic block diagram of ADPLL

Second component loop filter removes high frequency parts of phase error signal [2]. For loop filter k counter is used. It always works with phase detector. Output of phase detector is fed into the k counter.k counter clock is M times multiple of the center frequency. M typically be 8, 16, 32.. [1] .It contains two independent counters. First counter is up counter and second is down counter. But in practice both counts upward. The modulus of counter is k. The range of the both the counters is from 0 to k-1. dn/up signal controls the operation of k counter. If this signal is high, then down counter is active otherwise, if it is low, then up counter is active. The MSB of down counter is borrow and the MSB of up counter is carry.DCO operation is controlled by these two signals.

Third component digital controlled oscillator (DCO) makes the frequency equal to the input frequency. For this increment-decrement counter is used. It has three inputs: (a) Inc, (b) Dec, (c) IDClock. It works together with k counter [1] .It uses id clock, as clock signal. Id clock is multiples of centre frequency and modulus of divide by n.

2.1. ADPLL Implementation

All basic building blocks of ADPLL i.e. phase detector, loop filter and digital controlled oscillator are designed using Verilog. For verifying the design test bench has been created and simulation is done. For designing and simulating Xilinx ISE 10.1 tool is used. Figure 2 [1] shows the implemented ADPLL block diagram.

EXOR is used as PD. Centre frequency is taken as 100 kHz. The simulation output of ADPLL in the locked condition at frequency of 199 kHz is shown in figure 3. In this figure,3. tc represents DCO's output at the last stage. tc1 represents input signal. dn/up signal is represented by updwn.Figure3 shows that frequency of DCO and input are same and very less phase error among them which is satisfying the condition for locking.

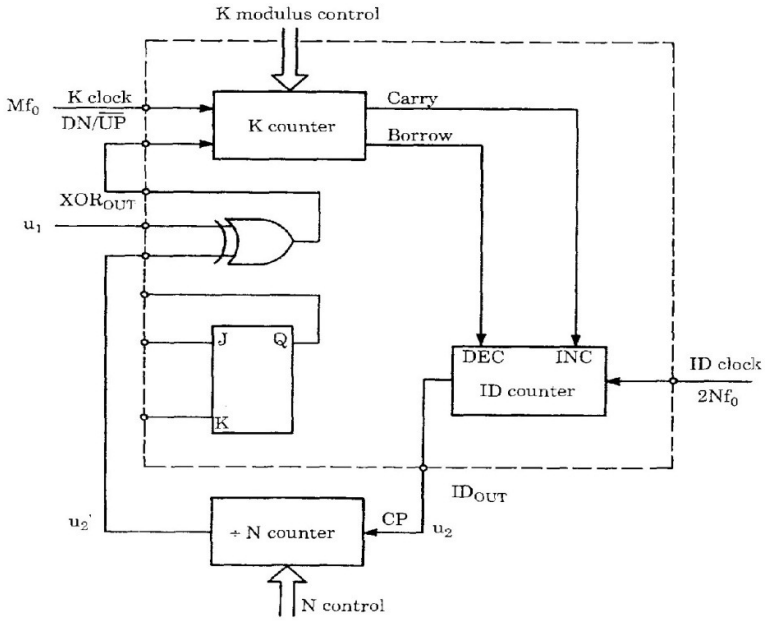

Figure 2. ADPLL circuit diagram

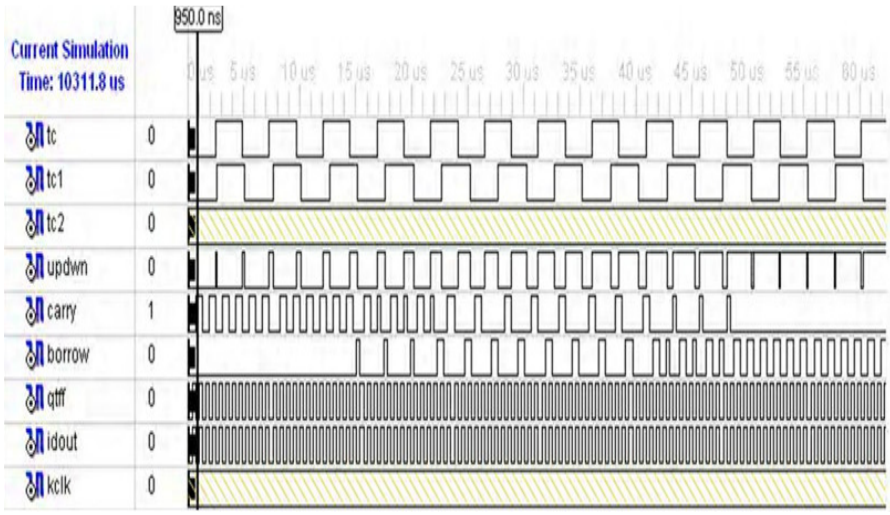

Figure 3. Simulation output of the ADPLL in locked condition at f = 199 kHz

Figure 4 shows simulated waveform of the design for the unlocked case. In this figure tc and tc1 represents DCO and input signal. dn/up signal is represented by updwn. The input frequency of the ADPLL is taken as 200 kHz. Figure 4 represents the conditions for unlocking. Simulation is performed for different frequencies and the hold range of the designed ADPLL is 0 Hz-199 kHz. In the next section the ADPLL is designed with Ripple reduction techniques and simulated in the same way as this ADPLL.

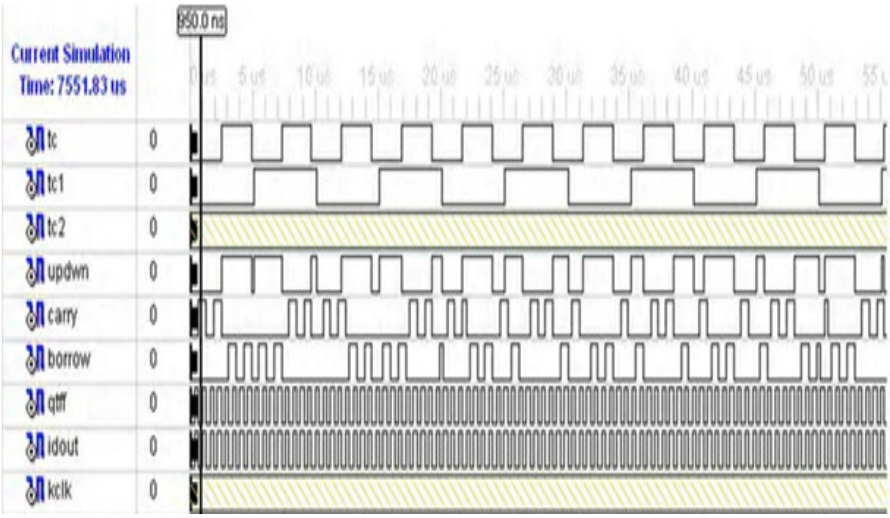

Figure 4. Simulation output of the ADPLL in unlocked condition at f = 200 kHz

3. DESIGN OF ADPLL WITH RIPPLE REDUCTION TECHNIQUE

By using ripple reduction techniques ADPLL performance can be improved. Figure 5, represents ADPLL design with ripple reduction techniques. K counter uses an extra enable signal. Loop filter works only when enable becomes high. For suppressing ripple second MSB is used. en represents enable input for the k counter. The en signal is high about 50% of time. Now, K counter generates maximum number of carries. Divide by n counter output is represented by tc.tc1 represents the input signal.

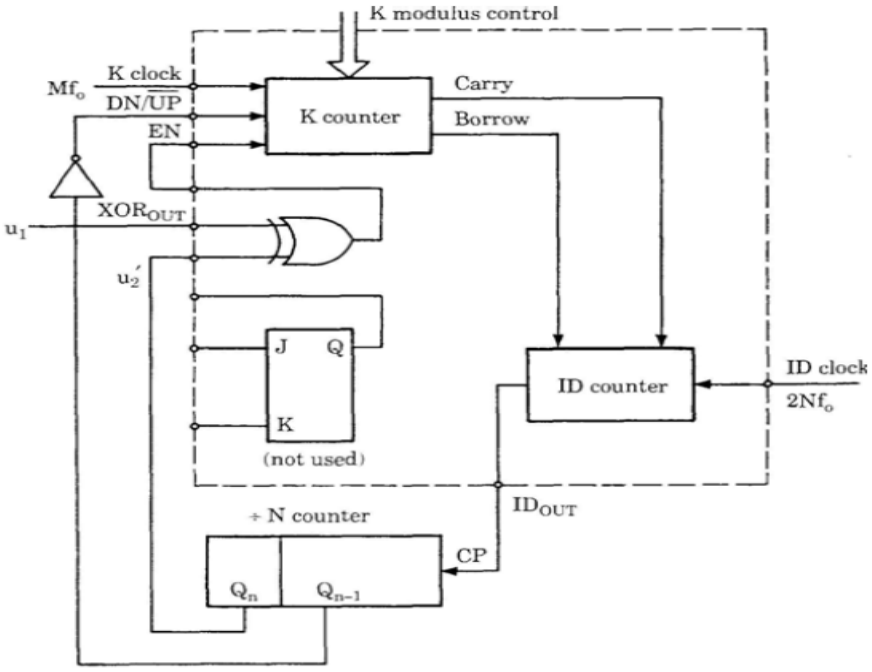

Figure 5. ADPLL design with ripple reduction technique.

Design is implemented with the condition K>M/4 the however, the value of M remains same in both the designs. Other methods are discussed in paper [1], [13] ,Figure 6 represents ADPLL design with ripple reduction technique in locked condition at frequency of 216 kHz. tc1 represents input signal. dn/up signal is represented by updwn. This design uses same center frequency. tc1 is taken as 199 kHz.figure 6, represents the conditions of locking. Figure 7 shows simulated waveform of the design for the unlocked case. In this figure tc represents final output of DCO. dn/up signal is represented by updwn .In this case input frequency is taken as 200 kHz. Figure 7, shows that hold range varies with the ripple reduction technique. This design provides better hold range. The hold range in the case is 11 kHz - 216 kHz.

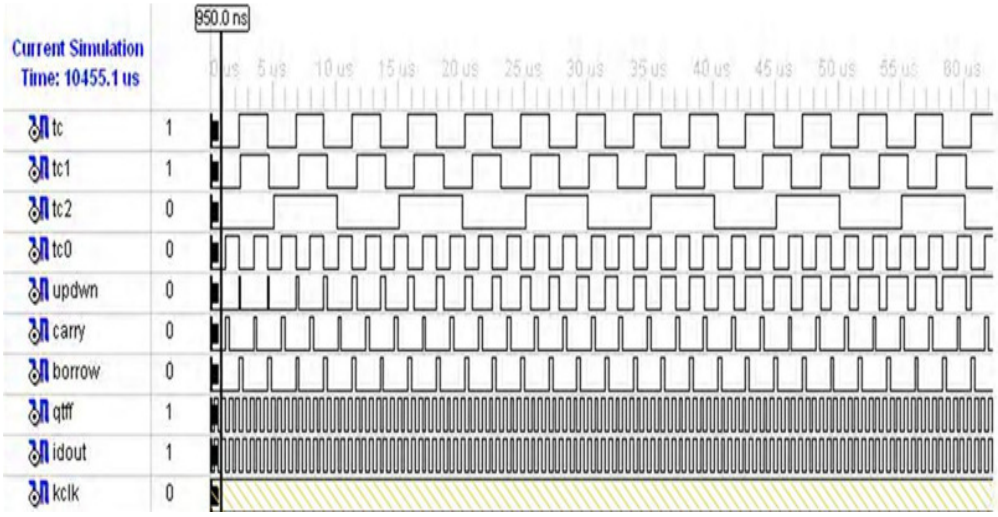

Figure 6. Simulation output of the ADPLL in locked condition at f = 216 kHz

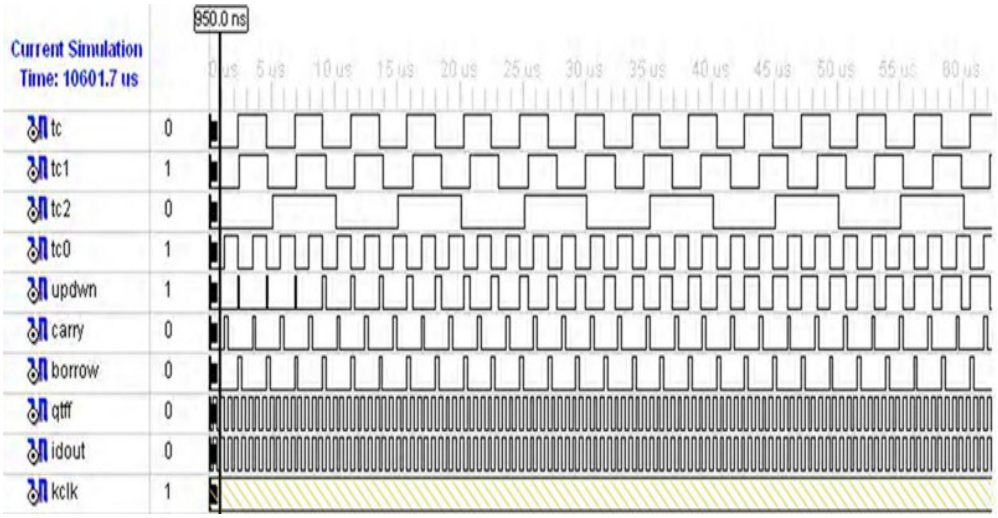

Figure 7. Simulation output of the ADPLL in unlocked condition at f = 217 kHz

4. RESULTS

The ADPLL has been implemented into Xilinx vertex5 xc5vlx110t chip. Chip is having 69,120 LUT's. A maximum of 640 IO's are available.65 nm CMOS technology based FPGA is taken. FPGA system clock is 100mhz.This design is used in high frequency applications. It offers better locking among reference signal and DCO signal. The hold range of design is from 0 Hz-199 kHz. Figure 8 shows the FPGA output for locked case. Figure 9 shows the FPGA output for unlocked case. Figure 10 shows the FPGA output for locked case when ripple reduction technique is used. Figure 11 shows the FPGA output for unlocked cases when ripple reduction technique is considered. The FPGA results are shown with the help of Digital Phosphor Oscilloscope (DPO) from Tektronix i.e. TDS 305 4B DPO. Digital Phosphor Oscilloscope (DPO) having 500 MHz frequency capturing capability. From figure 8, 9, 10 and 11 it can be seen that when ripple reduction technique is used then better capture range is achieved. Thereby, we got better lock range for the ADPLL with ripple reduction technique.

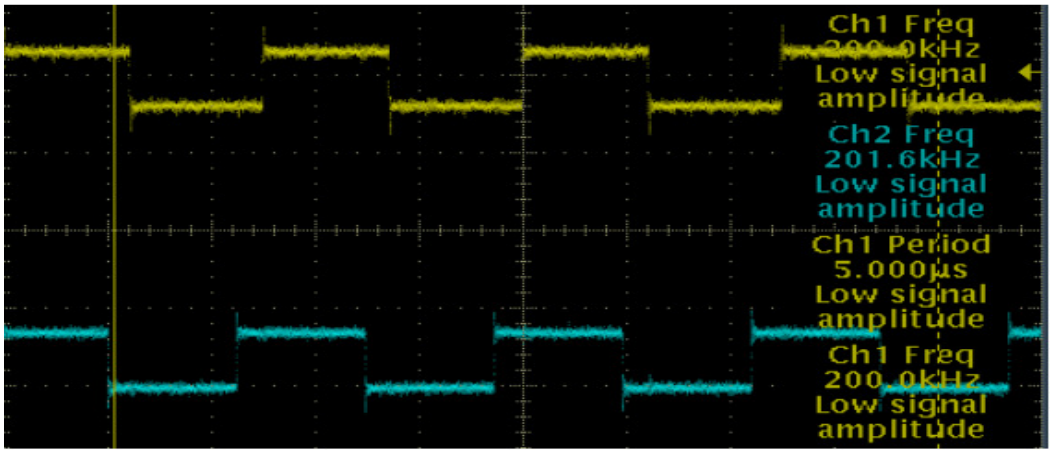

Figure 8. FPGA output of the ADPLL in locked condition at f = 200 kHz

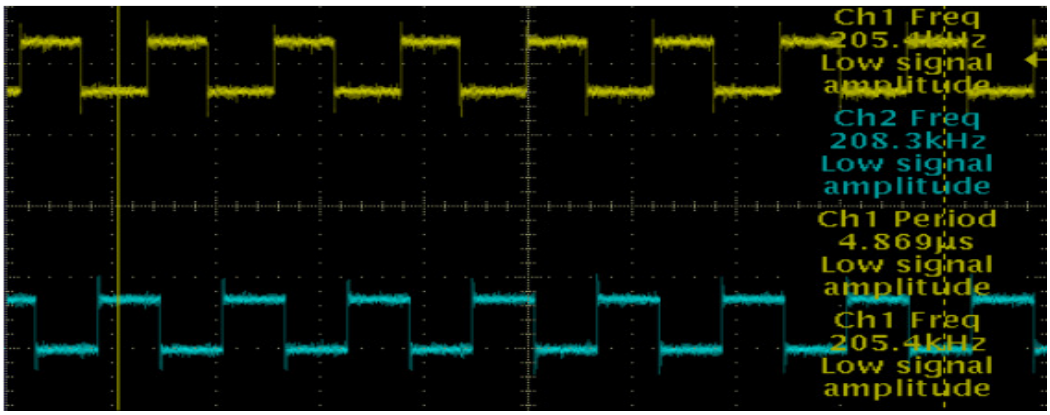

Figure 9. FPGA output of the ADPLL in unlocked condition at f = 205 kHz

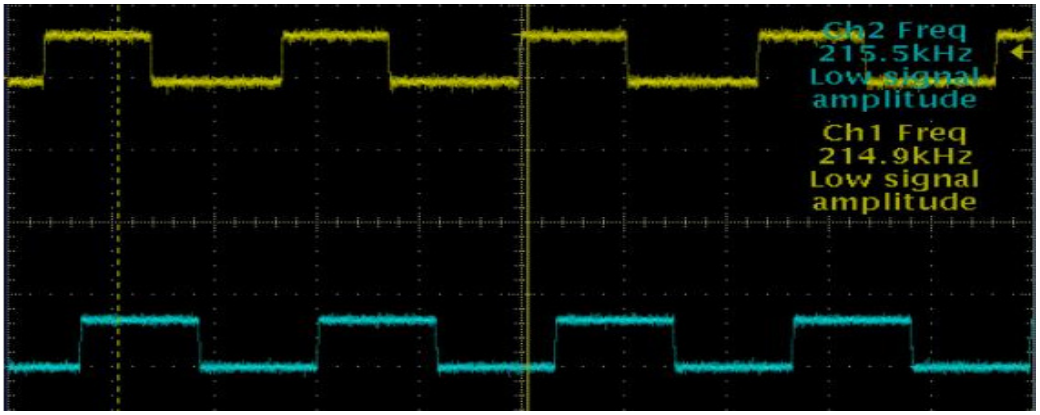

Figure 10. FPGA output of the ADPLL (ripple reduction technique) in locked condition at f =215 kHz

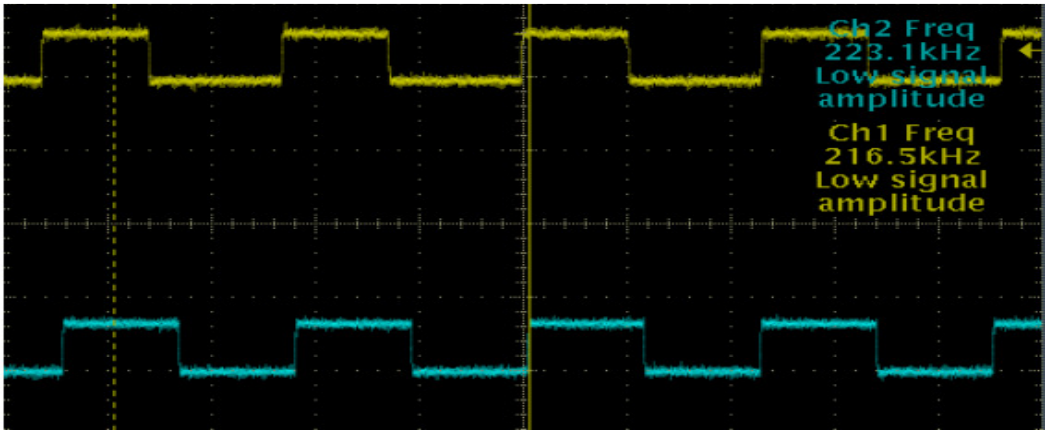

Figure 11. FPGA output of the ADPLL (ripple reduction technique) in unlocked condition at f = 216 kHz

5. CONCLUSIONS

This paper discusses the ADPLL implementation in two ways; viz, basic ADPLL implementation and ADPLL implementation with ripple reduction technique. For ADPLL design and simulation the Xilinx 10.1 is used .FPGA implementation for both the circuit (i.e. with and without ripple reduction techniques) has been presented. Improvement in the performance of an ADPLL with the help of ripple reduction techniques is discussed. ADPLL is implemented with centre frequency of 100 kHz. For the ADPLL the frequency range is from 0 kHz to 199kHz.When ADPLL is implemented with ripple reduction techniques then the frequency range is observed as 11 kHz to 216 kHz. The results as discussed in the previous section, from the FPGA implementation shows that the better lock range can be achieved by reducing the ripples.

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REFERENCES

[1] Roland E. Best, *"Phase Locked Loops Design Simulation and Applications"*, McGraw-Hill, 5th Edition.

[2] Qiang Zhang, "Research and application of all digital phase locked loop", *Intelligent Networks and Intelligent Systems School of Electrical Engineering and Automation,* Hebei University of Technology, Tianjin, China Conf., 2009.

[3] K.T.lbrahim,and A.E Salama, "Digital Of ADPLL for Good Phase and Frequency Tracking Performance", *Nineteenth National Radio Science Conference, Alexandria, March 2002.*

[4] Riad Stefo, Jorg Schreiter, Jens-Uwe SchliiOler and Rene SchiiRny, "High Resolution ADPLL Frequency Synthesizer for FPGA- an based Applications", *Department of Electrical Engineering and Information Technology Dresden University of Technology, Germany.*

[5] Indrani Hatai, and Indrajit Chakrabarti, "FPGA implementation Digital FM Modem", *Information and Multimedia Technology Electronic and Electrical Communication Engineering Indian Institute of Technology, Kharagpur, India, Conf., 2009.*

[6] Martin Kumn, and Harald Klingbeil, "An FPGA-Based Linear All Digital Phase-Locked Loop", *IEEE transaction on circuit and systems, VOL 57, NO.9, September 2010.*

[7] Moorthi S., and Meganathan D. "Low Jitter ADPLL based Clock Generator High Speed SoC Applications", *World Academy of Science, Engineering and Technology 42 2008.*

[8] Sandeep Vallabhaneni, and Sanjay Attri, "Design of an all-Digital PLL core on FPGA", *Sci. /Engr. SF, AISG/AISD, IISU, ISRO India.*

[9] Pao-Lung Chen and Chun-Chien Tsai, "An Interpolated Flying-Adder Based Frequency Synthesizer" Department of Computer and Communication Engineering, *National Kaoshiung First University of Science and Technology,No. 2, Jhuoyue Road, Nanzih District, Kaohsiung City 811, Taiwan.*

[10] Moorthi S, Meganathan D. "Low Jitter ADPLL based Clock Generator for High Speed SoC Applications", *World Academy of Science, Engineering and Technology 42 2008.*

[11] Kwang-Jin, LEE,Hyo-chang, KIM, "A Low Jitter ADPLL for mobile applications" *IEEE transaction, Vol.E88C, No.6, June2005.*

[12] Aniruddha Chandra, "Phase Locked Loop", ECE Department, NIT Durgapur, *Winter School on VLSI Systems Design, WB, Jan24, 2009.*

[13] Rosink,W.B., " All-Digital Phase-Locked loops Using the 74HC/HCT297 ", Philips componenets,1989.*(Available in the United states from Philips Semiconductors),811 east Arques Ave.,Sunnyvale , CA 94088*