DESIGN AND NOISE OPTIMIZATION OF RF LOW NOISE AMPLIFIER FOR IEEE STANDARD 802.11A WLAN

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ABSTRACT

Low noise amplifier is the front end block of radio-frequency receiver system. Its design required various characteristics such as power gain, noise figure, insertion losses and power consumption. In this paper we have proposed a single stage low noise amplifier design with high gain and low noise using inductive source degeneration topology for frequency range of 3 GHz to 7 GHz and also use the active biasing devices. A range of devices like inductors and capacitors are used to achieve 50 Ω input impedance with a low noise factor. The design process is simulated process is using Advance Design System (ADS) and implemented in TSMC 0.18 μm CMOS technology. A single stage low noise amplifier has a measured forward gain 25.4 dB and noise figure 2.2 dB at frequency 5.0 GHz.

KEYWORDS

Advanced design system, Low noise amplifier, Radio-frequency, Noise figure, Wireless network, CMOS, RF switch, VLSI.

1. INTRODUCTION

The low noise amplifiers (LNA) are key components in the receiving end of the communication system. Its performance is measured in a number of figures which are most notable while dynamic range, return loss and stability are examples of others. Signal received from the antenna is directly given to the low noise amplifier then external as well as internal noise of the circuit is reduced. In reference [1] two MOSFETs are used in cascode topology which has little effects with each other. Therefore, the device parameters of these two MOSFETs in cascode topology can be design separately, with almost no trade-off [2, 3]. But this topology requires more area with complexity.

References [4-6] presented that LNA which are able to provide gain to input signal powers up to -15 dBm without degrading linearity or adding much noise. Such properties enable the wireless receiver to operate in hostile communication environments. In low noise amplifier design, the most important factors are forward gain, low noise, matching and stability. In this paper, we design a CMOS LNA using single stage inductive source degeneration topology with respect to impedance matching and noise optimization. Generally the cascoded topologies are used in the

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designing of CMOS LNA. Here we have used the inductive degeneration common source topology with active device biasing. The use of active devices increases the temperature sensitivity. Major applications of the LNAs [7-9] are to increase the signal power as well as minimizing the noise. *Srivastava et. al.* [10] have proposed a model of the double-gate CMOS for double-pole four-throw RF switch design at 45-nm technology, which is also an application for the LNA. The proposed LNA operates at 5.0 GHz frequency used in IEEE standard 802.11a WLAN.

2. LOW NOISE AMPLIFIER CIRCUIT SYNTHESIS

Selection of the devices is an important task for designing process, because the noise and impedance matching conditions are highly related to each other. In reference [11-13], a common-gate topology has been used to realize wide-band characteristics but the common-gate topology usually has related higher noise figure (NF) than common-source topology. We have used a single stage inductive source degeneration topology as shown in Fig. 1, which uses only one MOSFET with source degeneration.

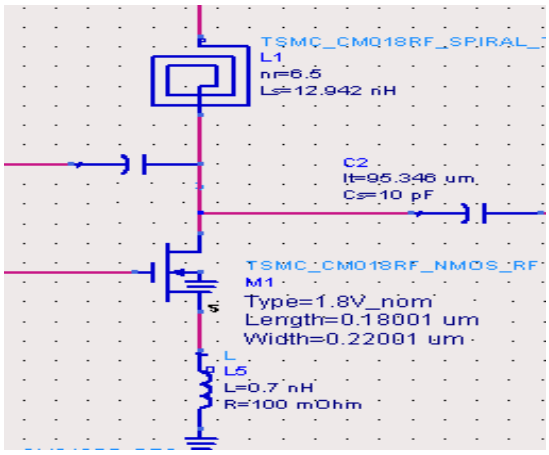


Figure 1. Single stage inductive source degeneration LNA.

The minimum NF can be made independent of the transistor width by selecting the source degeneration reactance [14]. The input impedance is given by:

$$Z_{in} = \frac{V_{in}}{I_{in}} = S(L_G + L_s) + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}} \tag{1}$$

when we use 50 Ω impedance then Ls is solved as:

$$L_s = \frac{C_{gs}}{g_m} Z_o \tag{2}$$

The LNA design formula and equation were referred to [15]. A low-noise amplifier is designed using a device's noise modal or noise parameters and S-parameters [16]. In a low noise amplifier, the transistor's input is matched for optimum noise figure and the transistor's output is conjugate matched with 50 Ω system impedance for a maximum gain. The output noise of a two-port network with noise figure is given by:

$$N_o = FGKTB \tag{3}$$

If minimum detectable input signal is X dB above the noise floor, then

$$P_{in}^{\min} = N_o - G + X \tag{4}$$

$$P_{out}^{\min} = N_o + X \tag{5}$$

3. DC BIASING

The proper bias or quiescent point for the application to maintain constant current over transistor parameter variations is required due to the process and temperature. The most critical device parameter commonly used in biasing is I_{dss}, the saturated current at zero gate bias. The change of I_D with V_G voltage is transconductance and is given by:

$$g_m = \left.\frac{\Delta I_D}{\Delta V_G}\right|_{V_{ds}} \tag{6}$$

Generally the active or passive type biasing is used. In this paper, we also used active component for biasing at 2.14 V and DC biasing network shown in Fig. 2.

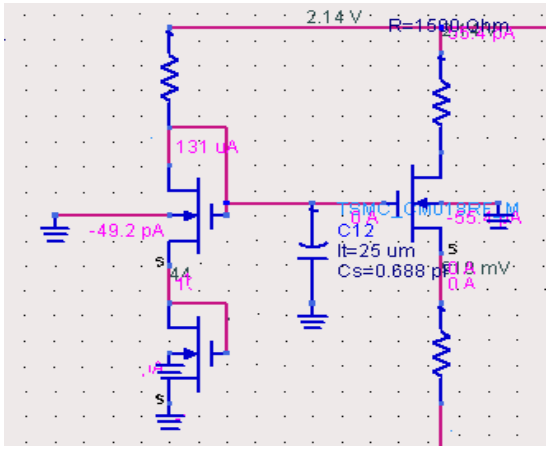


Figure 2. Active device DC biasing network.

4. SINGLE STAGE AMPLIFIER

The amplifier consists of a transistor, the circuit for matching the source termination and the transistor, and that for matching the load termination and the transistor. The source and load terminations are usually 50 Ω. The useful gain to design an amplifier is transducer power gain, which accounts both source and load mismatching. The function of the matching circuits is to provide suitable source and load conditions for the transistor such that the transistor can generate power gain for the input signal under a stable condition which is shown in Fig. 1. Matching occurs when $Z(j\omega_o) = R_s$.

$$(L_G + L_S)W_o = \frac{1}{W_o C_{gs}} \tag{7}$$

$$R_S = \frac{g_m L_s}{C_{gs}} \tag{8}$$

where R_s is the resistor associated in the input voltage source. LNA circuit of Fig. 1 is implemented in 0.18 μm CMOS technology and then characterized.

4.1. Noise Figure

The total noise power consists of amplified input noise entering the amplifier and the noise generated in the amplifier itself. The total noise bandwidth (NBW) is selected to make the total noise power correctly as:

$$NBW = \frac{\int_0^\infty T_A(w).G_A(w)dw}{T_A.G_A} \tag{9}$$

The range of 'w' is limited by other components in the system, or by the gain response of the amplifier. The noise figure is given as:

$$F = F_{\min} + \frac{R_n}{G_s}(G_s - G_{opt})^2 \tag{10}$$

The total equivalent input current noise is the sum of the reflected drain noise contribution and the induced gate current noise. Other parameter of two-port noise is shown as:

$$G_u = \frac{i_u^2}{4KT\Delta f} \tag{11}$$

And the minimum noise figure is given by

$$F_{\min} = 1 + 2R_n(G_o + G_{opt}) \tag{12}$$

If there were no gate current noise, the minimum noise figure would be 0 dB.

4.2. Stability

The stability of a circuit is characterized by stern stability factor (K), Circuit is stable when K>1 and Δ<1.

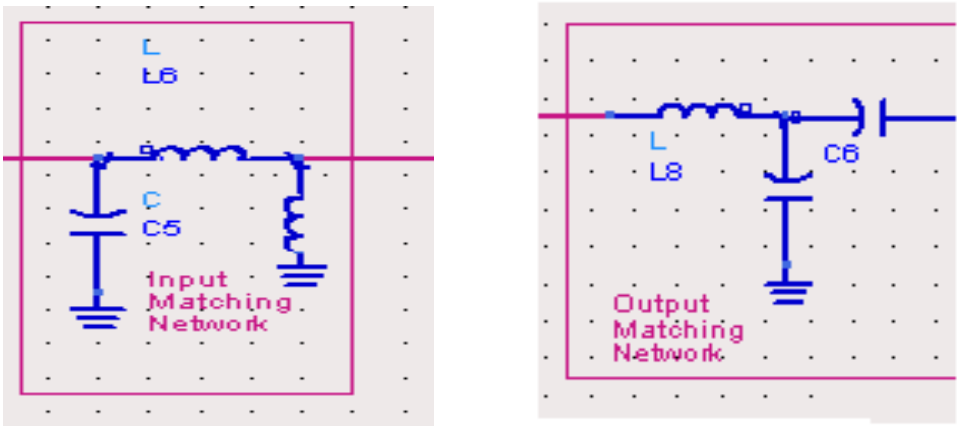
$$K = \frac{1 + \Delta^2 - S_{11}^2 - S_{22}^2}{2S_{11}S_{22}} \tag{13}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{14}$$

Absolute stability is then determined when the input reflection coefficient Γ_{in}<1 and output reflection coefficient Γ_{out}<1. This is a very important consideration in a design and can be determined from the S-parameters, matching networks, and terminations [17].

5. MATCHING NETWORK

To design the input and output impedance matching to maximize the power transfer and minimize the reflections we required the idea of matching network [18]. According to maximum power transfer theorem, the maximum power will be delivered to the load when the impedance of load is equal to the complex conjugate of the impedance of source means Z_s=Z_L^*. The Smith chart is used to visualize the interactive process of impedance matching. Impedance matching network are shown in Fig. 3. Conjugate matching will satisfy the optimal noise condition and impedance matching simultaneously as a result of transistor sizing and bias condition. The ccomparison of LNA performance with other published data is shown in Table 1.



(a) (b)

Figure 3. (a) Input and (b) Output impedance matching network.

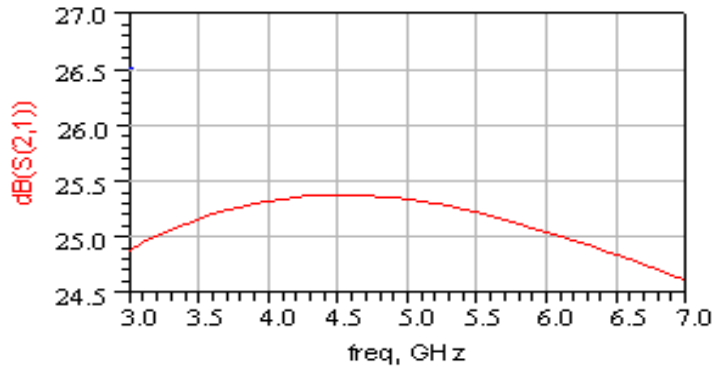


Figure 4. Simulated S_{21} forward power gain at the frequency 5.0 GHz.

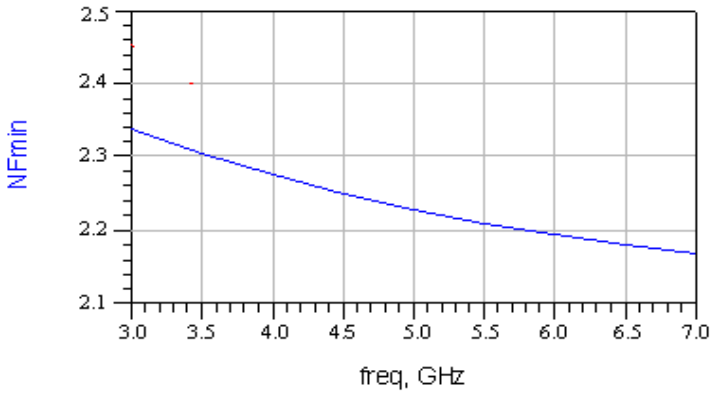


Figure 5. Simulated noise figure at 5.0 GHz.

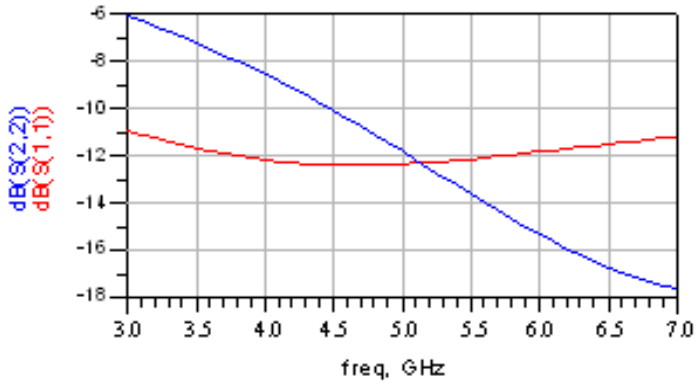


Figure 6. Simulated input and output return losses.

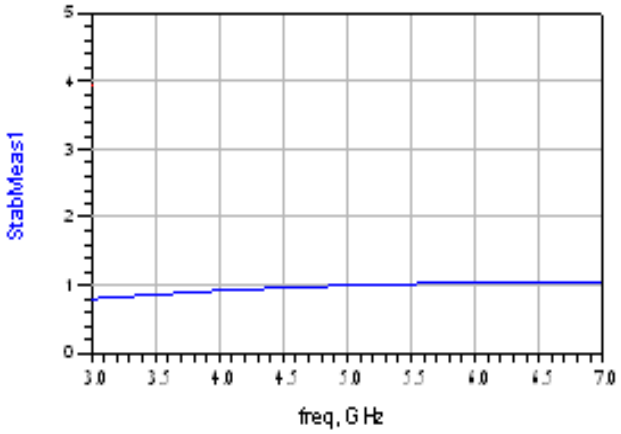


Figure 7. Stability factor vs. frequency.

6. SIMULATION RESULTS AND CONCLUSIONS

The designed LNA with matching network at 5.0 GHz is obtained. The proposed LNA is implemented in TSMC 0.18 µm CMOS technology. The simulation recorded that the amplifier gain S_{21} is 25.3 dB. The input insertion loss S_{11} is -12.2 dB, overall noise figure (NF) is 2.2dB and the output insertion loss S_{22} is -12 dB. The best impedance matching for the high power gain and low noise in frequency range 3 GHz to 7 GHz shown in Fig. 4 to Fig. 7. Here a low noise amplifier circuit design for frequency of 3 GHz to 7 GHz has been presented and circuit simulations were done in ADS. LNA with 25.3 dB gain and 2.2 dB noise figure at frequency 5 GHz to 6 GHz. A 5.0 GHz single stage low noise amplifier is used in IEEE 802.11a standards for wireless local area network (WLAN). We can use this technology with the CMOS and the latest technology of double-gate MOSFET for designing a RF CMOS switch [24-26].

Table 1. Comparison of LNA performance

References	Frequency	Gain (S_{21})	NF	S_{11}
[19]	5.5 GHz	10	6.2	-12
[20]	5.7 GHz	16.4	3.5	-11
[21]	5.6-5.8 GHz	21.4	4.4	Better than 7
[22]	5.3 GHz	13	2.1	-13
[23]	5 GHz	18.3	1.63	--
This Work	5 GHz	25.3	2.22	-12.2

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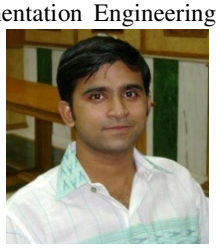

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