PERFORMANCE EVALUATION OF CDMA ROUTER FOR NETWORK - ON - CHIP

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Abstract

This paper presents the performance evaluation of router based on code division multiple access technique (CDMA) for Network-on-Chip (NoC). The design is synthesized using Xilinx Virtex4 XC4VLX200 device. The functional behavior is verified using Modelsim XE III 6.2 C. The delay and throughput values are obtained for variable payload sizes. Throughput-Power and Delay-Power characteristics are also verified for NoC.

Keywords

CDMA, Walsh Code, Router, NoC

1. INTRODUCTION

Traditionally, ICs have been designed with dedicated point-to-point connections, with one wire dedicated to each signal. Now with new developments in chip manufacturing technologies several Intellectual Property (I.P.) blocks such as processor cores, memories, dedicated hardware can be built on single chip with high increase in computation performance. For such rising computation performance the communication bandwidth requirement also increases with same rate.[1][3]

The traditional bus based system is not suitable for communication, among these increasing on-chip resources. The wires occupy much of the area of the chip and wiring delays are becoming dominant over gate delays. [4][5]. Networks are generally preferable to such buses because they have higher bandwidth and support multiple concurrent communications. [6]

Network-on-Chip (NoC) is an approach to designing the communication subsystem IP-cores in a System-on-Chip (SoC). NoC applies networking theory and methods to on-chip communication and brings notable improvements over conventional bus and crossbar interconnections. NoC improves the scalability of SoCs. Network-on-Chip (NoC) is an emerging paradigm for communications within large VLSI systems implemented on a single silicon chip. Network-on-Chip is spreading rapidly with the development of new architectures and new efficient routing techniques.

Although NoCs borrows the concepts and techniques from the well-established domain of computer networking, it is impractical to blindly reuse features of classical computer networks. With NoC-

DOI : 10.5121/vlsic.2012.3307

[i] It is possible to take advantage of part of the technology developed for packet switched networks in the field of communication theory and computer networks, adapting those concepts to the particular constraints of on chip interconnection.

[ii] It is possible to achieve a very high grade of flexibility.

[iii] It is possible to make design modular by extensive use of parameterized independent functional blocks.

[iv] Functional blocks can be reconfigured by mutually connecting them in different manners in order to create particular topology needed for a given application.

[v] It is possible to easily integrate IP cores developed by different people or companies, provided that this modules share a common interface for communication with the external environment.

[vi] Computing and communication environments are separated.

We have proposed a NoC router based on CDMA technique. Mostly the CDMA technique is widely used in wireless communication but some researchers have proposed various ways of applying CDMA technique for on chip wired communication. We have proposed the packet switched CDMA router which handles the issues - flow control and contention resolution. The rest of the paper is organized as follows. Section 2 gives brief idea about CDMA technique. Section 3 deals with the architecture of CDMA router. Synthesis results are summarized in section 4. Finally conclusion is drawn in section 5.

2. CDMA Technique

CDMA is a spread spectrum technique that uses a set of orthogonal codes to encode the input sequence from different sources before transmission. The encoded data from different senders are added together for transmission without interfering with each other, which is achieved by the orthogonal property of spreading code. The orthogonal property means normalized autocorrelation and cross correlation values of spreading codes are 1 and 0 respectively. Auto correlation of spreading codes refers to the sum of the product of codeword with itself whereas cross correlation refers to the sum of product of two different codewords.

At the receiving end the data can be decoded from received sum signals by multiplying the received signals with spreading codes used for encoding. This is possible because of the orthogonal property of spreading codes.

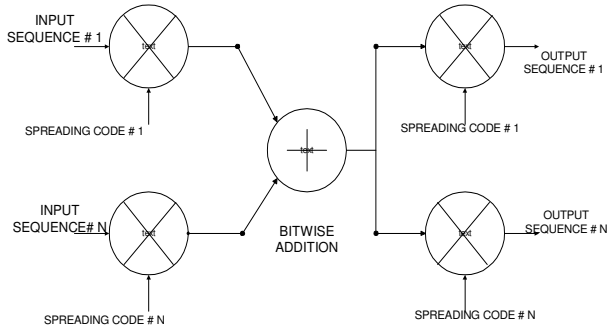


Figure 1. CDMA Communication

3. CDMA Router Architecture

The CDMA router using three IP cores is shown in figure 2.Router architecture consists of six basic functional blocks- FIFO Buffer (BUF), Walsh Code Generator (WCG), Scheduler, Modulator (MOD), Code Adder, and Demodulator (DEMOD). The input packets from different IP Cores are stored in FIFO buffer of depth four. The packet consists of two-bit destination address, two-bit source address and a variable length payload. The two-bit source address is also transmitted to the destination along with the payload.

We have used Walsh code of length four as a spreading code for modulation. Each resource is assigned a fixed source address and corresponding fixed Walsh code as indicated in Table 1.

Table 1. Walsh Codes assigned to resources

Resource	Source Address	Walsh Code
(Reserved)	00	0000
IP1	01	0101
IP2	10	0011
IP3	11	0110

The all zero Walsh Code is reserved for the condition when there is no data to transmit with the resource. The Walsh code is generated from the source address. The router design is scalable as by selecting the Walsh code of higher length, number of IP cores attached to the router can be increased.

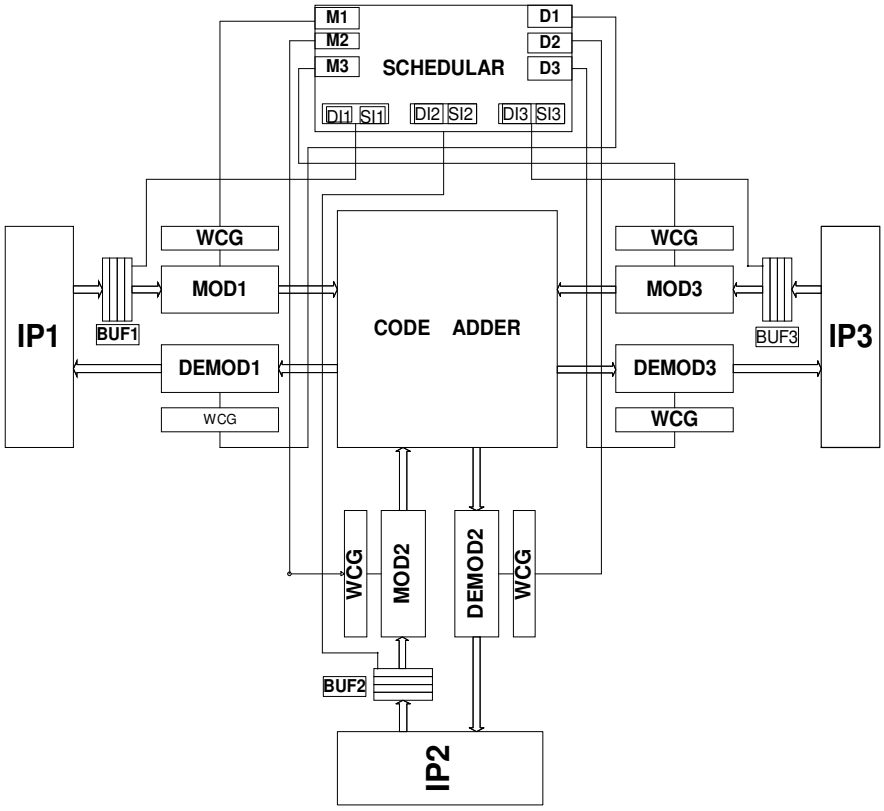


Figure 2. CDMA Router Architecture

3.1 FIFO Buffer

The input buffering is used in the design. The length of the buffer is equal to the packet size and it is having a depth of four that holds four packets. When clock and enable are at logic high, the complete input packet is shifted to next memory slot. Thus minimum four clocks are required for the packet to come out of the buffer.

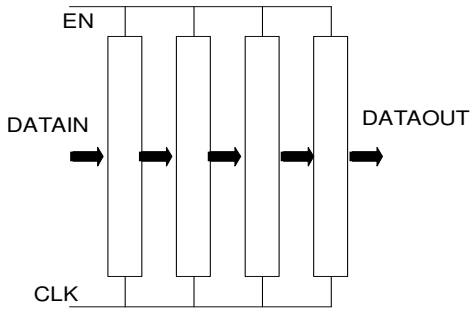


Figure 3. FIFO Buffer

3.2 Scheduler

Contention resolution is an important task in router. If two or more resources are sending data to one destination at same time then there is contention for destination. This contention is resolved by assigning priorities to the resources based on different requirements. Since we have implemented the router for three resources there can be contention for destination due to maximum of two resources. The scheduling algorithm is designed by observing different conditions for contention. All the possible conditions for contention are summarized in Table 2.

Table 2. Conditions for contention

case	source	destination	Contention
1	01	10/11	D1
	10	01	
	11	01	
2	01	10	D2
	10	01/11	
	11	10	
3	01	11	D3
	10	11	
	11	01/10	
4	01	10/11	No Contention
	10	11/01	
	11	01/10	

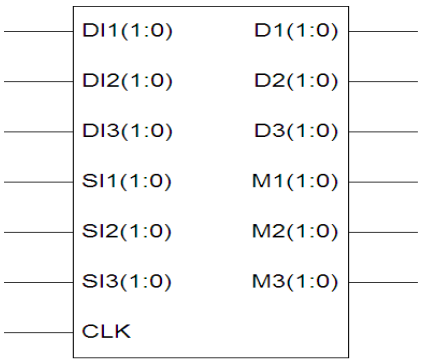


Figure 4. Conceptual Diagram of Scheduler

Figure 4 shows the conceptual diagram of scheduler. The four bit headers from all the resources which include two bit source address and two bit destination address are input to the scheduler. As per the scheduling algorithm, scheduler outputs source addresses and destination addresses to the Walsh Code Generators both at source and destination sides.

3.3 Walsh Code Generator

The Walsh code possesses the orthogonal and balance property which is essential for the CDMA communication. The Balance Property of Walsh code indicates equal number of 1's and 0's in the code.

Table 3. Truth table for Walsh Code Generation

INPUT		OUTPUT			
S0	S1	W0	W1	W2	W3
0	0	0	0	0	0
0	1	0	1	0	1
1	0	0	0	1	1
1	1	0	1	1	0

Table 3 indicates truth table for generation of Walsh Code of length four from two bit source addresses.

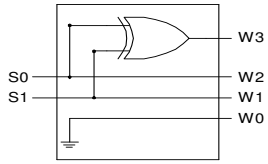


Figure 5. Walsh Code Generator

Figure 5 indicates the circuit realized from the truth table which is used for the generation of Walsh Code.

3.4 Modulator

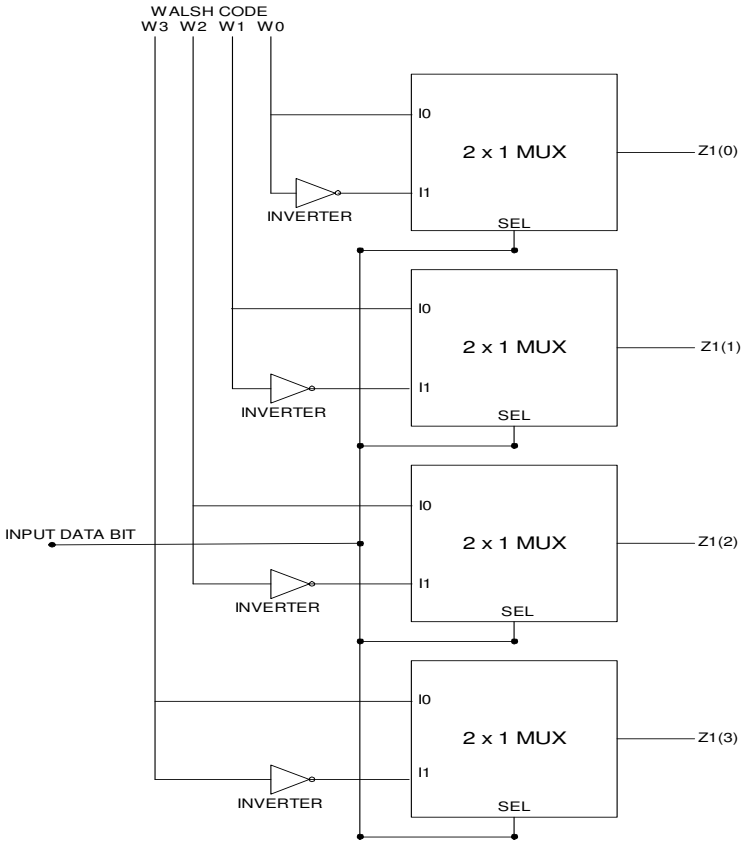


Figure 6. Modulator for 1 Bit

Figure 6 indicates the modulator for one bit. The four bit Walsh Code from Walsh Code Generator is assigned to the four MUXes as indicated in figure. Data bit is assigned to the select line of all the four MUXes. Modulation is carried out in parallel. The pseudo code of modulation algorithm is given bellow.

```
IF  (data bit = = 0)   THEN
        { Transmit Codeword Itself }
ElSIF  (data bit = = 1)  THEN
        { Transmit Inverted Codeword }
END IF
```

3.5 Code Adder

The modulated data bits from all the three resources are added together in code adder. This added data is transmitted to the demodulators of all the three resources simultaneously in parallel.

Figure 7 shows the code adder for 1 bit data from all the three resources.

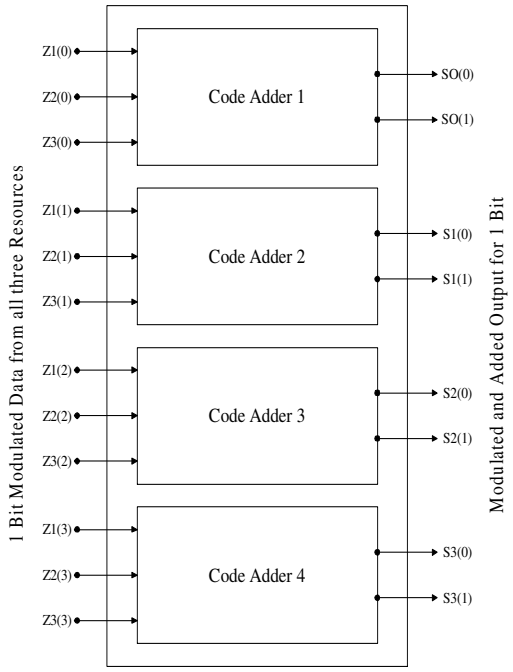
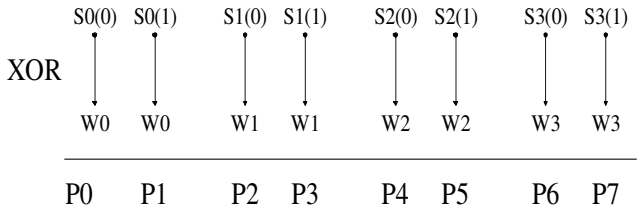


Figure 7. Code Adder for 1 Bit

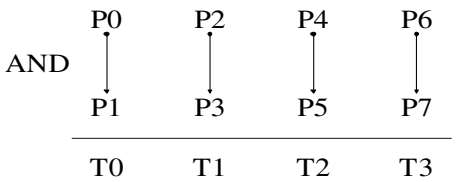
3.6 Demodulator

The modulated and added data is simultaneously sent to the demodulators of all the three resources. The data intended for particular demodulator is recovered with the help of Walsh Code. The demodulation algorithm is illustrated bellow. The demodulation is carried out in completely parallel manner. The demodulation algorithm given bellow decodes 1 bit of data. The algorithm is used in parallel to decode all the data bits.

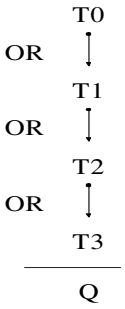
Step 1:



Step 2:



Step 3:



4. SYNTHESIS RESULTS

The CDMA NoC router architecture was synthesized on Xilinx Virtex4 XC4VLX200 device with the FF1513 package and the -10 speed grade. The functional behavior of CDMA router architecture was verified using Modelsim XE III 6.2 C.

Table 4 summarizes the optimal frequency and total delay for various payload sizes. The total delay is distributed in logic and route delay. The delay is constant for variable range of payload.

Table 4. Synthesis Results

Payload Size	Optimal Frequency	Throughput	Total Delay	= Logic	+ Route
8 Bit	233.781 MHz	5.610 Gbps	4.277 ns	1.485 ns(34.7%)	2.793 ns(65.3%)
16 Bit	233.781 MHz	11.221 Gbps	4.277 ns	1.485 ns(34.7%)	2.793 ns(65.3%)
24 Bit	233.781 MHz	16.83 Gbps	4.277 ns	1.485 ns(34.7%)	2.793 ns(65.3%)
32 Bit	233.781 MHz	22.442 Gbps	4.277 ns	1.485 ns(34.7%)	2.793 ns(65.3%)
40 Bit	233.781 MHz	28.05 Gbps	4.277 ns	1.485 ns(34.7%)	2.793 ns(65.3%)

Since the complete communication is in parallel the throughput is computed as (3 Resources) *(Number of payload bits)*(Clock Frequency). [2] The throughput values are obtained in Gbps.

Figure 8 shows throughput for different payload sizes. Since overall delay is constant and hence the optimal frequency, throughput is found to be the function of number of payload bits by keeping number of resources constant.

Figure 9 shows delay for different values of computed throughput. The delay is constant for all the values of throughput.

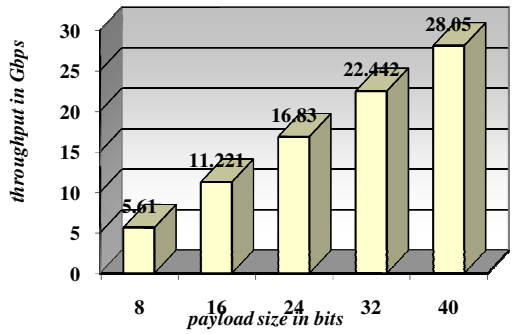


Figure 8. Payload Vs Throughput

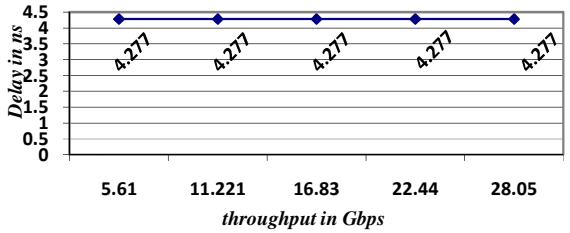


Figure 9. Throughput Vs Delay

Figure 10 and 11 gives throughput-Power and Delay-Power characteristics

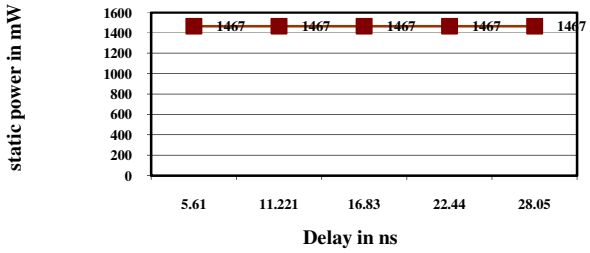


Figure 10. Throughput Vs Static Power

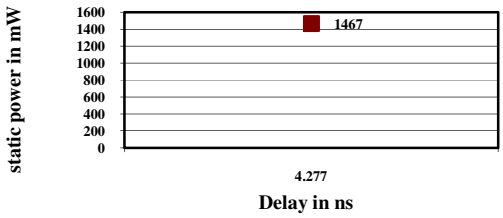


Figure 11. Delay Vs Static Power

5. CONCLUSION

The proposed CDMA is scalable, modular and reusable which satisfies the basic requirements of NoC. In the proposed CDMA router scheme for NoC it has been observed that delay is constant for various ranges of payloads. The concurrent transmission of data increases overall throughput.

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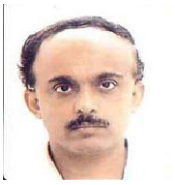

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After working there for three years he moved Institute of High Performance Computing Singapore where he carried research work in the area of CAD for VLSI and nano-electronics. He has published about 30 papers International Journals, international conferences and also filed one patent in USA in the area of VLSI Currently he is working as a professor & Dean (academic) at VNIT Nagpur.