DELAY ERROR WITH META-STABILITY DETECTION AND CORRECTION USING CMOS TRANSMISSION LOGIC

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ABSTRACT

The new technologies are giving the advance systems which are capable to perform multiple operations simultaneously. This all is possible by the scaling technology where the overall chip size get reduced but due to manufacturing and fabrication defects, certain design uncertainty arises thereby affecting the transistor performance by timing related effect. The robust circuit where sufficient margins are given sometime is nothing but a wastage of power to overcome this, hybrid technique called Razor was innovated which scaled the voltage dynamically and automatically detect and correct the timing related defects. This paper proposed a new design for the razor flip flop with CMOS transmission logic. The traditional design used the dynamic logic approach which has the drawback of threshold voltage attenuation which is removed by CMOS transmission logic and the transparency of the logic data at input and output is highly achieved. The overall purpose for such design is to reduce the power and delay of the circuit which is reduced by 0.6mW and 12.11ns respectively and thus increased the overall performance. The complexity of the circuit is also reduced. The analyses of the circuit is done using Cadence virtuoso tool with 45n technology.

KEYWORDS

Razor, CMOS transmission logic, meta-stability detector, DVS

1. INTRODUCTION

The emerging technology has introduced the new smart systems that are capable to perform multiple operations simultaneously. The new hand held device like mobile can perform parallel operation such as playing music, video, gaming, internet access and even can interact with the environment for different application. These all get possible by the scaling technology. The size of the transistor gets reduced so that numbers of chips are fabricated on a same die. The manufacturing and fabrication process has certain limitations which cause the dimension variation and design uncertainty in the system [1]. The uncertainty results the process variation, temperature fluctuation, glitches, inductive and capacitive noise and variation in supply voltage are the basic cause for frequency variation which results the timing relate defects. These variations can be static or dynamic that depends on its rate of change with time [2]. The static variations generally come after the fabrication process and remain fixed with time such as process variations, temperature fluctuation etc [3], [4]. It occur due to ageing effect and thus are very slow variations whereas the dynamic variation occurs at the execution period such as hot spots due to temperature affect which is slow variation and jitter in the supply voltage due to induction that are very fast variations [5], [6].

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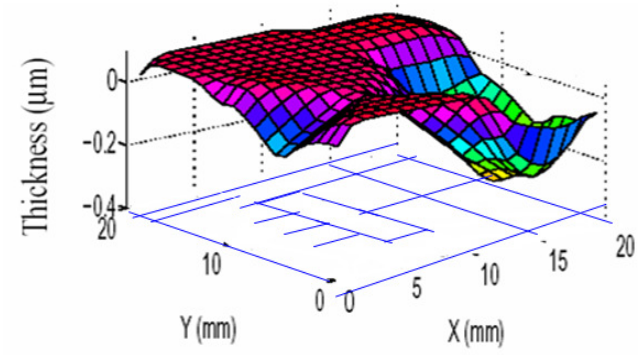


Figure 1. Dimension variation with thickness

These variations are further dived into two categories i.e. local or global depending upon the area it affects [7]. When all the transistors on die are affecting called global variation such as inter die process variation, temperature fluctuation where as the local variations affect the transistor which are influenced of one another such as IR drops. Under the robust design the noises are immune by the guard band provided to the supply voltage. This technique besides having many drawbacks as require a higher voltage, thicker interconnects wider devices and sometime having higher power consumption under the idle or low processor utilization period. The advance technology overcomes the limitations with a new technique called dynamic voltage scaling (DVS) technique. In traditional design, the canary circuit [8], [9] for DVS technique was widely used which has certain drawbacks and was then replaced by the new design called Razor as in figure- 2 where the safety margin is reduced corresponding to the error rate.

1.1 System Overview

Razor is flexible as it acquires dynamic voltage scaling (DVS) [10] technique where supply voltage varies according to the error rate this playing a very important role in low power design. It shaves the voltage margin where it is not required or under the low processor utilization and run below the critical voltage.

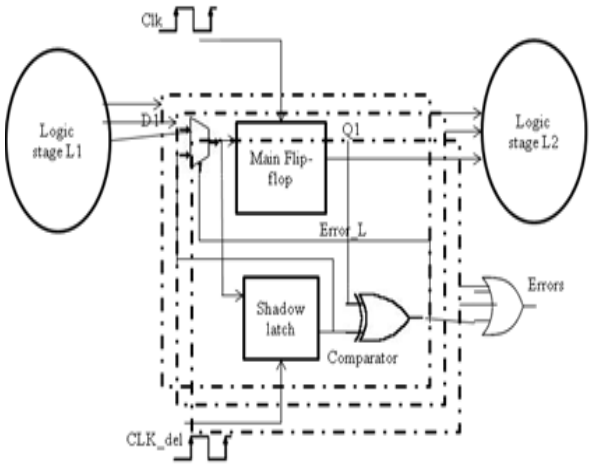


Figure 2. Razor architecture

The main concept follows by the razor is showing by the relation between frequency and voltage [11], where frequency is directly proportional to voltage and is given by the equation (1)

$$f \propto V_{dd} \tag{1}$$

Microprocessor is a pipeline process where razor use between input logic and output logic to detect the error which occurs due to delay. The razor circuit having the two flip-flop, main and shadow latch both are connected in such a way that if main flip-flop triggered by clock, shadow latch is triggered by delayed clock (skew). The shadow latch is the replica of main flip flop and is guarantee to store the correct data. There is a timing constraint for short path and long path [12]. The long path constraints states that the maximum state through a logic state must be less than the clock period (T) plus the skew between the clocks applied to main flip-flop and shadow latch and is shown by the equation (2). If the long path constraint is not satisfied, false negative error can occur causing the main flip-flop and shadow latch storing the incorrect value.

$$Delay_{max} < T + Skew \tag{2}$$

Similarly, for short path constraints, this states that there must not be a short path through a logic stage which can cause the output of the logic to change before the shadow latch latches the previous output. The condition for short path constraints is given by the equation (3). If condition does not satisfy that leads to false positive error, where the logic output changes in response to new circuit inputs before the shadow latch has sampled the previous output.

$$Delay_{min} > Skew + hold \tag{3}$$

Combination of the short and long path constraints demonstrates that Razor can only guarantee correctness when both condition in equation (2) and (3) satisfy and after combining is given by the conditions in equation (4) and (5):

$$Skew + hold < delay < T + Skew \tag{4}$$

$$Delay_{max} - Delay_{min} < T - hold \tag{5}$$

The timing violations are detected by supplementing critical (main) flip-flop, with a shadow latch as show in figure 2, where the output of a logic state strobes at a fixed delay (skew) after the main flip-flop. If timing violation occurs between main flip-flop and shadow latch that is if both having the different value then signal an error and stalls the whole pipeline. At the time of pipeline installation, the error signal instructs the main flip-flop to copy the correct value from the shadow latch. This whole process is more described in error recovery mechanism [13], [14]. During this time, the next logic stage has time to recalculate its values using the correct inputs.

1.2 Meta-stability detection

The digital system also goes through one more problem called meta-stability that can cause the system failure to detect the logic ZERO or ONE [15]. This occurs due to incorrect execution and wrong interpretation. In any D flip flop, the time requirement for meta-stability depends on two condition one the data input has to be stabilized before the clock event (Data setup time **Tsetup**) and second data input has to remain stable for some time after the clock event (data hold time **Thold**) as shown in figure 3. Similarly there is a propagation delay between clock-to-output which is denoted by **Tpd** in figurer 3.

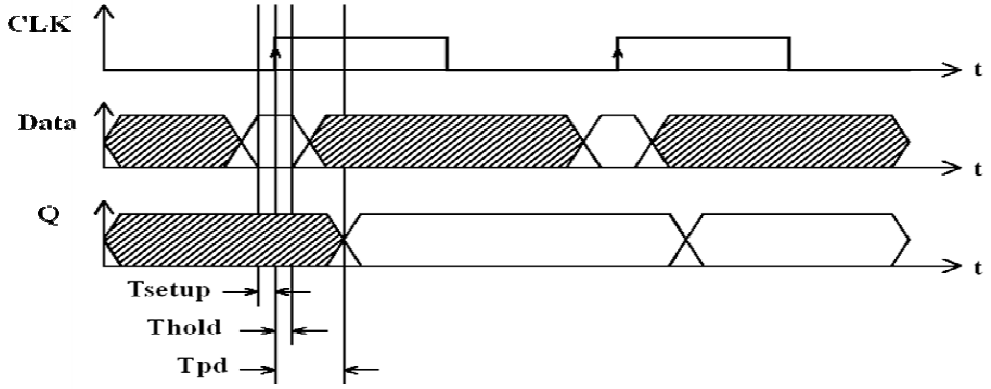


Figure 3. Timing requirement for meta-stability

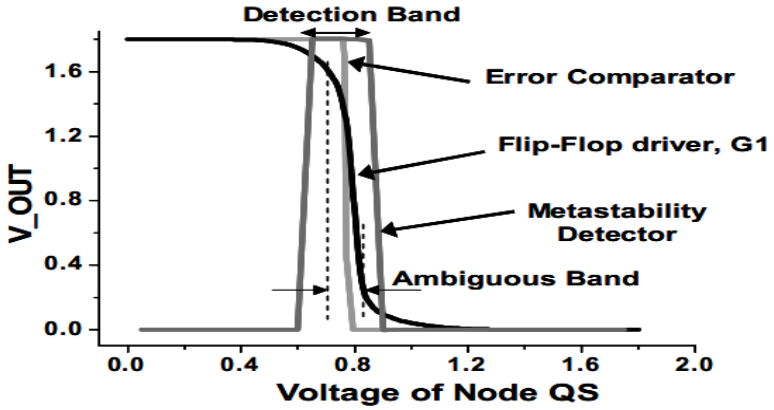


Figure 4. Principal of operation for meta-stability detector [18]

These failures come from the unusually long propagation delay for logic state that take the much decision time and lasts between the stable logic states for an indeterminate amount of time, and that result, need a circumstantially high resolving time. Initially this problem was detected and has been analyzed theoretically and measurement has taken with different aspect to completely understand its phenomena [16], [17].

2. METHODOLOGY

In this section we describe our implementation for new design of razor [17]. The new model is experimentally analyzed under the Cadence environment at 45 nm technology. First, the circuit schematic is designed where dynamic CMOS logic is replaced by the CMOS transmission logic. The circuit is also having meta-stability detector.

First the circuit for D flip-flop is design using CMOS transmission logic, which is then applied to the Razor architecture. The schematic is designed and then compile the design for the errors using Cadence virtuoso. The circuit simulation is done under ADL environment. The transient and DC analysis gives the D flip-flop characteristic, which shows that the data input is available at the rising age of the clock. The flip-flop consists of an extra latch called shadow latch to hold the correct data. The applied clock in shadow is guaranteed to store the correct data.

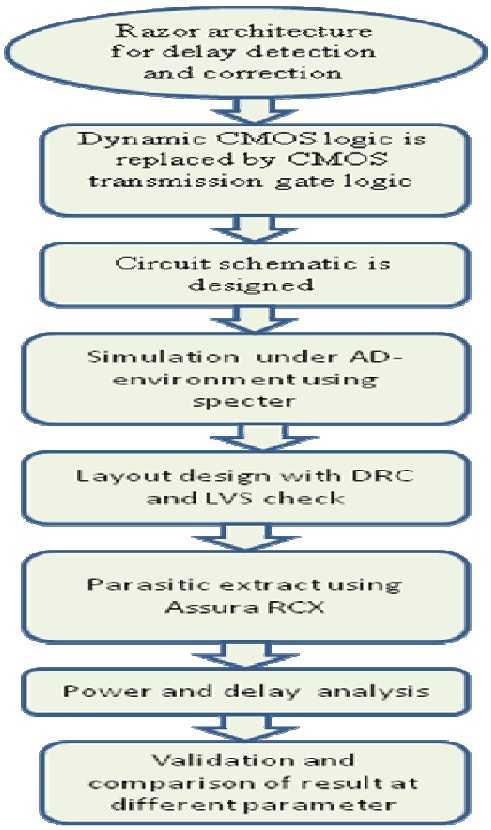


Figure 5. Methodology

The clock is half that of the clock applied to the main flip-flop and is simply generated using an inverter. At each clock cycle, the data in shadow latch match with the data in main flip-flop. Whenever the mismatch occurs, the circuit signals an error through error detector. The layouts extract and run the DRC check. Finally the circuit gives the parasitic value which then performs the power and delay analysis. The power analysis is done for the supply voltage range of 0.8V to 1.8V, at the temperature of 27C to 85C. Similarly the delay analysis is done for the W/L ratio of 2.22 to PMOS and NMOS transistor.

3. CIRCUIT LEVEL IMPLEMENTATION

The whole system is design at transistor level using cadence virtuoso. Traditionally, the system uses the dynamic CMOS approach. The circuit for Razor is normally behaved as the standard positive edge triggered D flip-flop where it shows the condition of no error. The master and slaves together with a shadow letch is designed by dynamic CMOS logic. The XOR gate is used for error detector or act as error comparator. It evaluates the error when the data latched by the slave differs from that of the shadow in the negative clock phase. There is a meta-stability detector designed which evaluate the meta-stable state of slaves output under the positive phase of the clock. The error comparator shares its dynamic node, Err_dyn, with the meta-stability-detector thus, the error signal is flagged by Razor design which either evaluate by the meta-stability-detector or the error comparator [18]. The Razor flip-flop is a pipeline process where the shadow latch (Razor flip-flop) is connected at each stage. This, in turn, evaluates the dynamic gate to generate the restore signal by “OR- ing” together the error signals of individual Razor flip-flop as shown in Figure 6, in the negative clock phase.

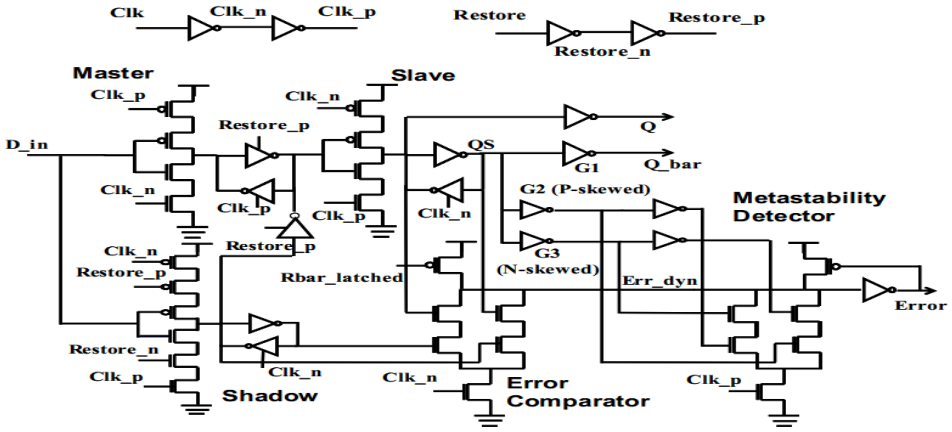


Figure 6. Circuit schematic for Razor [18]

3.1 Circuit redesign with CMOS transmission logic

In this paper, we review the model for Razor and give a new design where CMOS transmission logic is used. The circuit with dynamic logic is suitable for error detection and correction with DVS technique but somehow the power consumption is more [19] as there number of PMOS and NMOS transistor are used. The whole system is redesigned through CMOS transmission logic that also has the capability to detect the meta-stability state and best suited to the low power design. In dynamic voltage scaling, the processor run below the critical value thus there is more chances of threshold voltage attenuation [20]. The transmission gate logic has the advantage of minimum threshold voltage attenuation thus the transparency of the circuit is highly achieved. The D flip-flop is formed by using transmission gate as it is added at the master and slaves of the flip-flop. It is also added at the shadow latch. There is error detector for delay errors and one meta-stability detector to detect meta-stability state. The analysis and simulation of the circuit finally gives the better results.

3.1.1 CMOS Transmission Logic

The CMOS transmission gate can be constructed by the parallel combination of PMOS and NMOS with the complementary gate signal as in figure 7. The main advantage of CMOS transmission gate compared to NMOS transmission gate is to allow the input signal to be transmitted to the output without the threshold voltage attenuation. Besides this, certain other features affect the parameter of the transmission gate [21].

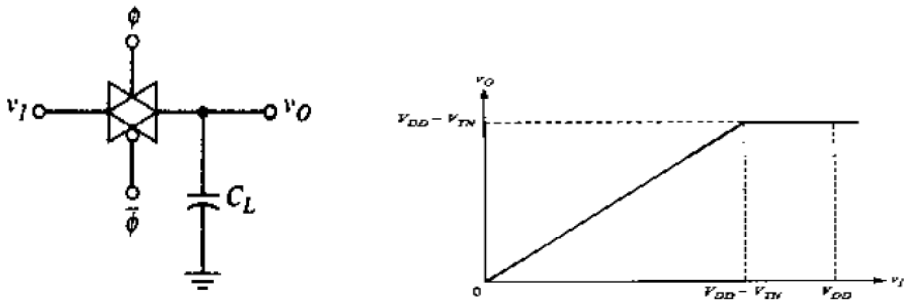


Figure 7. Circuit diagrame with output cherecterstic

3.1.2 D flip-flop with CMOS transmission logic

A D-type flip-flop is used to provide a delay. The logic bit on the D input is transferred to the output at the next clock pulse. When the CMOS transmission gate turn off (φ=0), the pn junction in the MN1 transmission gate transistor is reverse biased.

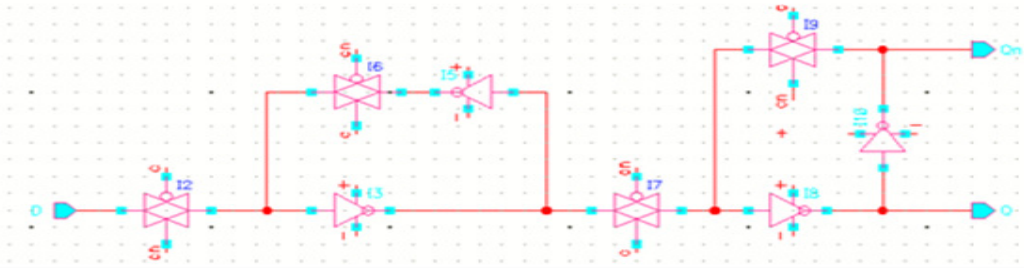


Figure 8. D-flip-flop with CMOS transmission logic

3.1.3 Circuit for clock generation and restore generation

The circuit for clock generation and restore generation is shown in figure 9 and 10. The shadow latch is driven by the delayed clock, and thus guaranteed to store the correct data in the shadow latch. This data is further compared to the data of main flip-flop. The delayed clock can be locally generated using an inverter. So that if main flip-flop is driven by CLK_P then shadow is driven by CLK_N. Similarly, the generation of restore signal restore_n and restore_p is shown in figure 10. The generation technique and there schematic for the clock and restore is show below in figure 9 and 10.

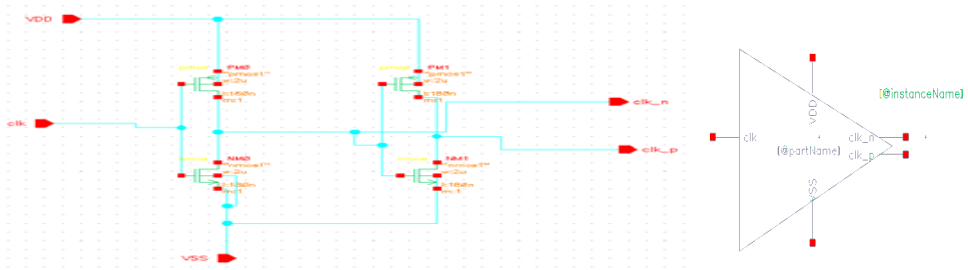


Figure 9. Clock generation buffer (a) Schematic (b) Symbol

Similarly the generation for the restore clock is given in figure 10

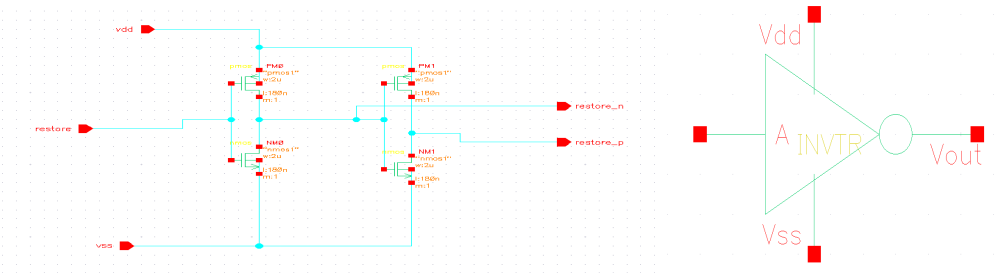


Figure 10. Restore generation (a) Schematic (b) Symbol

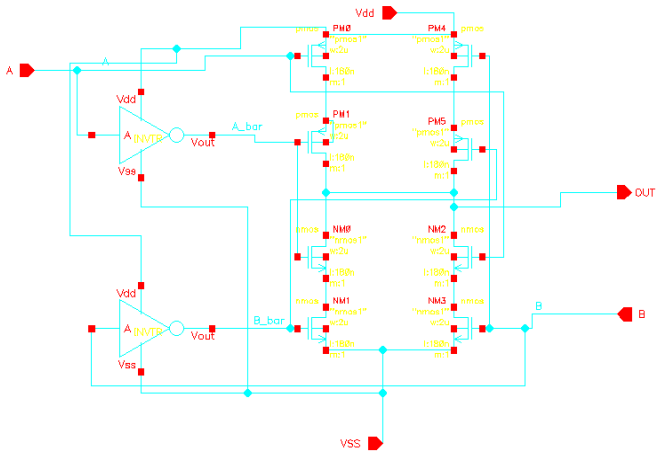


Figure 11. Circuit for error detection

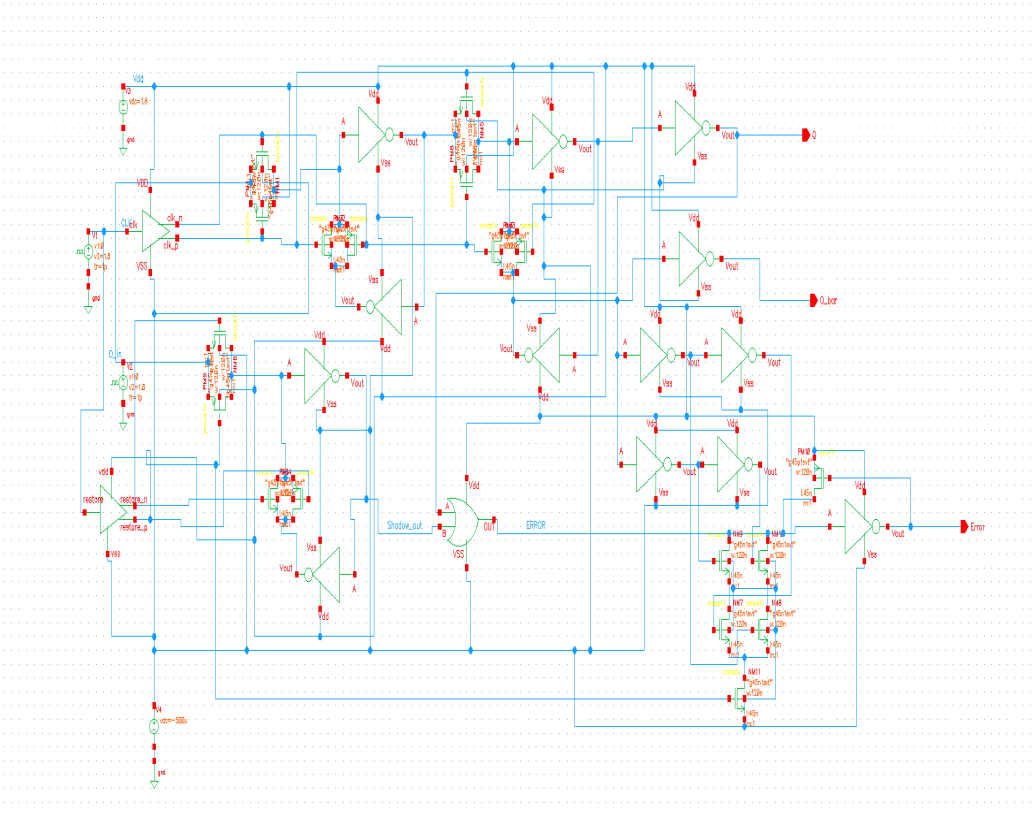


Figure 12. Razor with CMOS transmission logic

The transistor level schematic for Razor flip flop designed using Cadence Virtuoso at 45n technology, is shown in Figure 12 and layout design in Figure 13. The critical operating point for this circuit is 1.8V below the critical operating point the catastrophic failures occur.

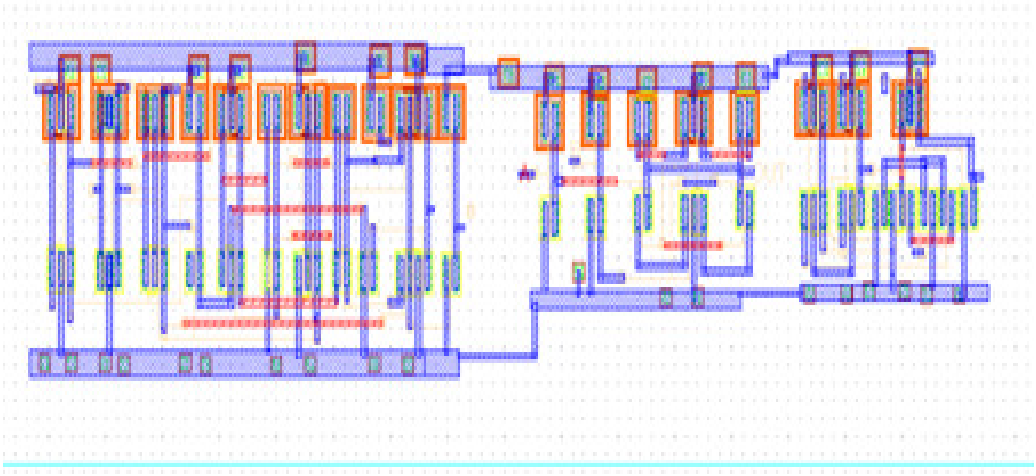


Figure 13. Layout for circuit design

4. PERFORMANCE AND EVALATION

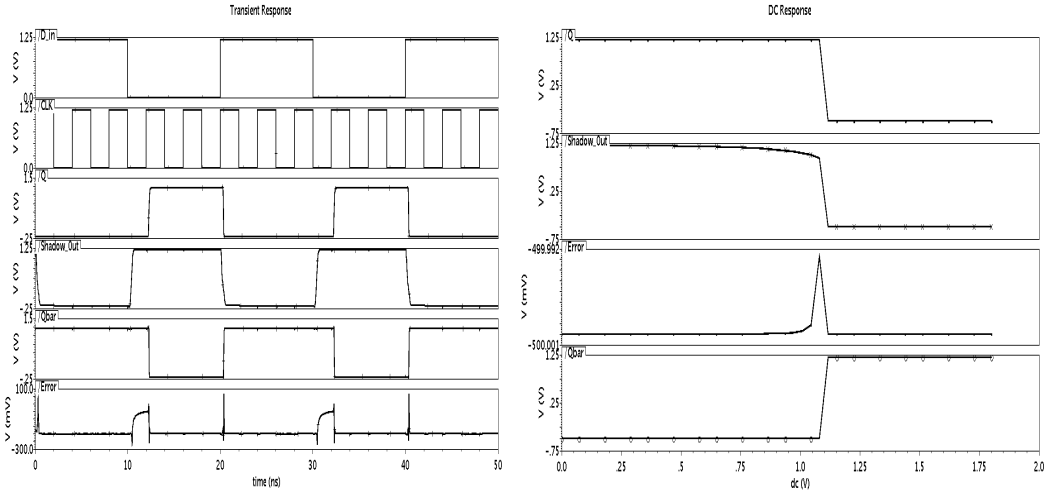
In this section the performance parameter for the designed circuit is evaluated using cadence tool. The circuit schematic is designed with CMOS transmission logic and run under analog and digital (ADL) environment. The extracted and designed layout run under DRC check and finally the circuit simulated with parasitic value.

4.1 Output, Power and Delay analysis

The circuit for new design is simulate and analyzed at 45nm node with the supply voltage range of 1.8V to 0.8V. The analysis gives the better result than that of traditional design. The total power overhead that is the power saving by DVS and the power consumption due to error recovery mechanism is reduced by 1.45mW. Similarly the delay analysis giving the better result for delay between clock to output and it is reduced by 12.11ns, which is very less than that of a traditional design. The comparative result between the traditional and new design is shown below in table 1.

S.No.	Parameters	Razor with dynamic logic	Razor with CMOS transmission logic
1.	Technology node	45 nm	45 nm
2.	Voltage range	1.8 V to 1.2 V	1.8 V to 0.8 V
3.	Total power overhead (mW)	2.9	1.45 mW
4.	Total Power	750 mW	0.6 mW
5.	Delay	0.18 µs	12.11 ns

Table 1. Comparison between Traditional and new design



(a) (b)

Figure 14. Output response

Similarly, the result for transient analysis which is done at range of 50ns is shown in figure 14(a). The flip-flop is operated at 1.2 V. The input is giving through D_in and result the same data at the output of Q terminal. At every rising edge of clock, the data is required to appear at the output which is the characteristic of D flip-flop. Similarly the other terminal of flip-flop Q_bar stores the inverted data. There is an error signal if both Q and shadow_ out has different value. It is required to have the same data in main flip-flop and shadow latch. Similarly the DC response of the circuit is shown in figure-14(b). This paper is mainly focused to reduce the power and delay of the circuit, by replacing the CMOS with transmission gate, thus through the transient characteristic the peak power for the new design is 1.45 mW, which is much lower than that of the earlier design.

The circuit operates initially at the voltage of 1.8V which is then scaled and results of reducing the average power as in figure-16(a). Similarly the delay analysis is done at different W/L ratio as in Figurer-16(b). The analysis of the propagation delay showing that it decreases with W/L ratio. The minimum range of width which can vary at 180n is 400n for the circuit.

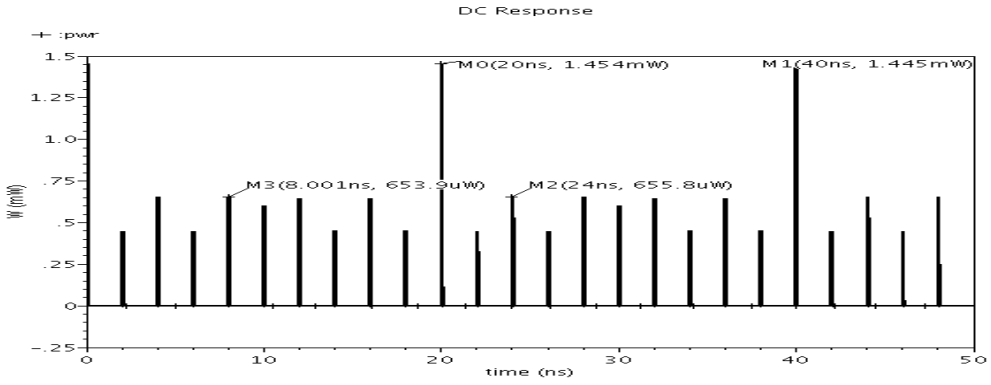
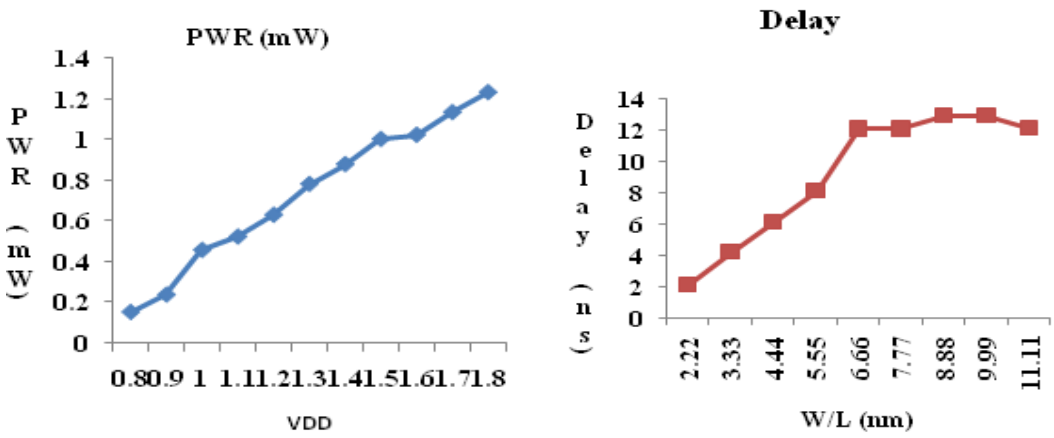


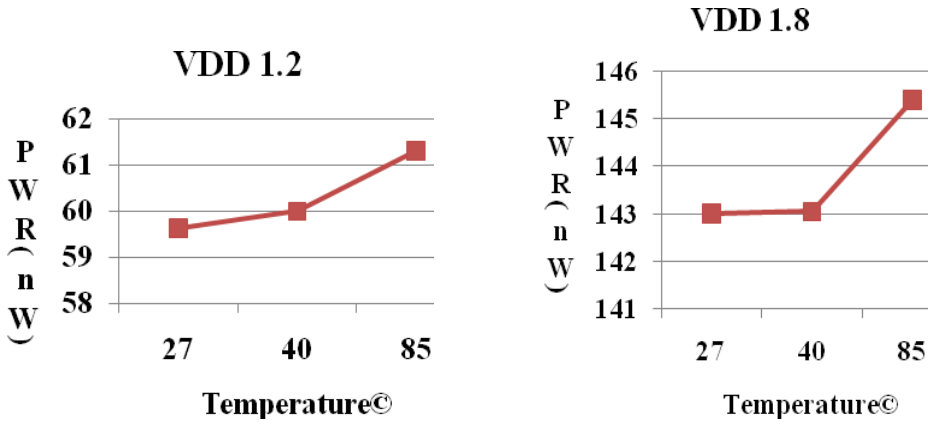
Figure 15. Power analysis for DC response



(a) (b)

Figure 16. Power and Delay analysis

The analysis is done at different temperature with different supply voltage resulting in the variation of the average power which is shown below in figure-17. The average power analysis for the circuit with respect to Vdd at 1.2V and 1.8V is shown in Figure-17. The average power for the modified design is reduced and is much lower than that of the conventional circuit [18] which is shown in Figure-17.



(a) (b)

Figure 17. Power analysis with temperature variation

5. CONCLUSIONS

In this paper we present a Razor flip-flop which is designed for error detection and correction of timing violation under the dynamic voltage scaling where CMOS logic is replaced by the transmission technology. The spice level analysis of razor using cadence virtuoso is done, where power analysis and delay analysis is done with respect to Vdd. The minimum range of scaling is 0.8 volts at temperature 27C. The new model for Razor is designed where dynamic logic is replaced by CMOS transmission logic and giving the better result thereby meeting the goal for the

low power design. We discussed how conventional circuit for Razor, fail to meet the low power requirement. Traditional techniques, robust circuit is designed holding wide margins to compensate for the PVT variations. We showed how CMOS transmission is better as giving the output without any threshold voltage attenuation. Razor supports the timing speculations using dynamic voltage scaling technique. The Razor voltage control system monitors the error-rate and tunes the supply voltage according to the observed error-rate to achieve a targeted rate, given as an input to the system. New design for Razor is more suited for low power design and allowing error-tolerant processor operation is still enables to determine the reduction of worst-case safety margins, thereby leading to significant improvements in energy efficiency. Error detection and correction is not more described here as we only work for the design. The new design is reducing the power and delay for the circuit. The whole circuit is analyzed in two mode one with meta-stability detector and other is the without meta-stability detector favorably trades-off the energy overhead of error-correction for additional efficiency benefits through margin elimination.

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