STAND-BY LEAKAGE POWER REDUCTION IN NANOSCALE STATIC CMOS VLSI MULTIPLIER CIRCUITS USING SELF ADJUSTABLE VOLTAGE LEVEL CIRCUIT

Deeprose Subedi[1] and Eugene John[2]

[1]Student, Department of Electrical and Computer Engineering, University of Texas at San Antonio, San Antonio, TX USA.
deeprose_76@hotmail.com

[2]Professor, Department of Electrical and Computer Engineering, University of Texas at San Antonio, San Antonio, TX USA.
Eugene.john@utsa.edu

ABSTRACT

In this paper, we performed the comparative analysis of stand-by leakage (when the circuit is idle), delay and dynamic power (when the circuit switches) of the three different parallel digital multiplier circuits implemented with two adder modules and Self Adjustable Voltage level circuit (SVL). The adder modules chosen were 28 transistor-conventional CMOS adder and 10 transistor- Static Energy Recovery CMOS adder (SERF) circuits. The multiplier modules chosen were 4Bits Array, 4bits Carry Save and 4Bits Baugh Wooley multipliers. At first, the circuits were simulated with adder modules without applying the SVL circuit. And secondly, SVL circuit was incorporated in the adder modules for simulation. In all the multiplier architectures chosen, less standby leakage power was observed being consumed by the SERF adder based multipliers applied with SVL circuit. The stand-by leakage power dissipation is 1.16µwatts in Bits array multiplier with SERF Adder applied with SVL vs. 1.39µwatts in the same multiplier with CMOS 28T Adder applied with SVL circuit. It is 1.16µwatts in Carry Save multiplier with SERF Adder applied with SVL vs. 1.4µwatts in the same multiplier with CMOS 28T Adder applied with SVL circuit. It is 1.67µwatts in Baugh Wooley multiplier with SERF Adder applied with SVl circuit vs. 2.74µwatts in the same multiplier with CMOS 28T Adder applied with SVL circuit.

KEYWORDS

10 Transistor SERF Adder, SVL Circuit, Stand-by Leakage Power, Dynamic Power, Delay, Low Power Design, Sub-micron Regimes.

1. INTRODUCTION

Today's Semiconductor device industries have been challenged with producing low power high performing portable electronic devices due to the increasing demand of their own consumer market. It is believed that the next generation portable electronic devices have to be developed with ultra-low power computational units such as multipliers [4]. In order to incorporate low power design into such computational units, Leakage power has to be minimized because leakage power accounts for the significant portion of the total power consumption in such circuits in deep sub-micron regimes. Research has shown that greater than 50% of the total power consumption is

due to leakage phenomenon within which stand-by leakage is another major component [6]. The stand-by leakage is the only source of power consumption in a static circuit [8]. This means that a fully charged device will be deficient of any charge even if it is not used for some long time. In such case the efficiency of the device is compromised.

The CMOS technology, supply voltage and threshold voltage have been scaled down to achieve faster performing devices [12]. However, leakage current has increased considerably and has become a major component of the total power consumption [1]. The leakage power component further is comprised of stand-by and active leakage currents. Most microelectronic circuits remain for considerable amount of time in static state. Therefore, low power design approach should also include stand-by leakage power reduction in static CMOS circuits. Stand-by leakage power dissipation dominates the dynamic power dissipation in deep sub-micron circuits and also in circuits that remain in idle mode for long time such as mobile phones [1]. The Stand- by leakage power dissipation is the power dissipated by the Static or the "idle" circuit. i.e. when the circuit is not turned ON. In the same lines, the dynamic power dissipation occurs when the circuit is switching. The equations (1) and (2) denote leakage and dynamic power dissipation respectively.

$$Pleak = Ileak \times Vdd \tag{1}$$

$$Pdynamic = \alpha f CVdd^2 \tag{2}$$

Where α is the switching activity, f is the operating frequency, C is the load capacitance, Vdd is the supply voltage and $I\,leak$ is the cumulative leakage current due to all leakage components [1], [14]. The total power dissipation is the sum of (1) and (2). The leakage current consists of various components, such as *Pn Junction Reverse-Bias current*, *subthreshold leakage, Gate leakage, Gate –induced drain leakage and punchthrough leakage* [1], [3], [7], [8], [9], [10]. Among them the *subthreshold leakage* is considered to be a major contributing component of the leakage power. These leakage mechanisms are well described by literature [1].

Literature [13] includes the ideas of bulk driven voltage which generates a channel inversion and sufficiently low gate to source voltage supply. The multi- Threshold Voltage CMOS (MTCMOS) and Variable threshold- voltage CMOS (VTCMOS) are the two regularly used techniques for reducing stand- by leakage power [2]. The MTCMOS technique requires additional fabrication process for higher threshold voltage and the storage circuits are not able to retain data [2]. The VTCMOS technique has major drawbacks as well, such as large area penalty, slow substrate-bias controlling operation and large power overhead [2]. Therefore, in order to skip the above mentioned drawbacks, a SVL circuit was chosen which minimizes stand-by leakage power whilst maintaining high- speed performance.

Figure 1 shows a self-adjustable voltage level circuit with *Vdd* as supply and *VL* as output voltages. The output voltage from this circuit is applied to the load circuit. The load circuits are the adder modules of conventional CMOS adder and SERF adder including their half adders which all are net-listed in the multiplier circuits. The SVL circuit hangs above these adder modules and drizzles only minimum voltages to them as such the subthreshold leakage current of idle MOSFETS decreases and the standby leakage power is minimized. For the stand-by mode that is when SL= 1 it supplies less voltage to the load circuit through "weakly on" NMOS transistors [6]. The voltage supplied to the load circuit is

$$Vl = Vdd - Vn \tag{3}$$

Where *Vn* is the voltage drop of all "weakly on" NMOS transistors. If Vdsn is the drain to source voltage of the NMOS transistors, then,

$$Vdsn = Vl - Vss \tag{4}$$

Now, from equations (3) and (4), we have,
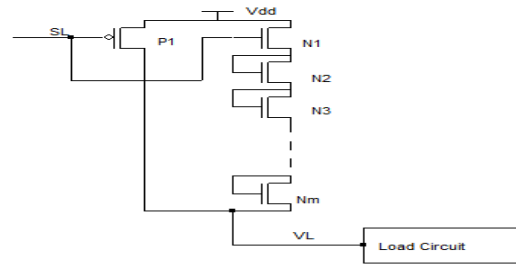
$$Vdsn = Vdd - Vn - Vss \tag{5}$$

Figure1. Self-Adjustable Voltage Level Circuit. Source: M. Rani etl., *Leakage Power reduction and analysis of CMOS sequential circuits (International Journal of VLSICS vol. 3 2012).*

Equation (5) shows that *Vdsn* can be decreased by increasing *Vn* [6]. In other words, by increasing the number of NMOS transistors. By decreasing Vdsn the Drain-Induced Barrier Lowering effect is decreased which increases the threshold voltage of NMOS transistors [6], [1]. The increased threshold voltage reduces the *subthreshold leakage* current of the NMOS transistors and thus, the Stand-by leakage power is reduced [6]. It will also decrease the dynamic power dissipation because of low supply voltage, *VL.*

Initially, each multiplier circuits were simulated using conventional 28 transistor adders and 10 transistor SERF adders one at a time. Their corresponding stand-by leakage power dissipation, delay and dynamic power were noted. And then, the two adder modules were constructed with SVL circuit and put into the multiplier architecture forming the complete circuit mesh one at a time. Again, their corresponding stand-by leakage power dissipation, delay and dynamic power were noted and a comparative analysis and evaluation was carried out. The SERF adder with SVL circuit based multipliers outperformed all other combinations which suggest that this combination (SERF adder with SVL circuit based multipliers) is suitable for ultra-low power design of multipliers. SVL circuits have been applied by literature [6] in CMOS sequential circuits, by Literature [2] in SRAM. This is the first time SVL circuits are being applied in CMOS multiplier circuits.

2. ADDER MODULES

2.1. Conventional CMOS 28 Transistor (28T) Adder

Employing fast and efficient adders in multiplier circuits will aid in design of low power high performance system [4]. Adders being the fundamental building block of the multiplier architecture play an essential role in design of such system. Figure 2 shows the conventional CMOS 28T adder which is constructed using same number of NMOS and PMOS transistors. The full adder logic is as follows [4], [14]:

$$Cout = AB + BCin + ACin \tag{6}$$

$$Sum = ABCin + (A + B + Cin)Cout' \tag{7}$$

These adder modules are constructed with functional pull up and pull down blocks of PMOS and NMOS transistors [14]. These adders form the basic building block in our multiplier architecture and often line in the critical signal path. Therefore, it determines the over performance of the system.
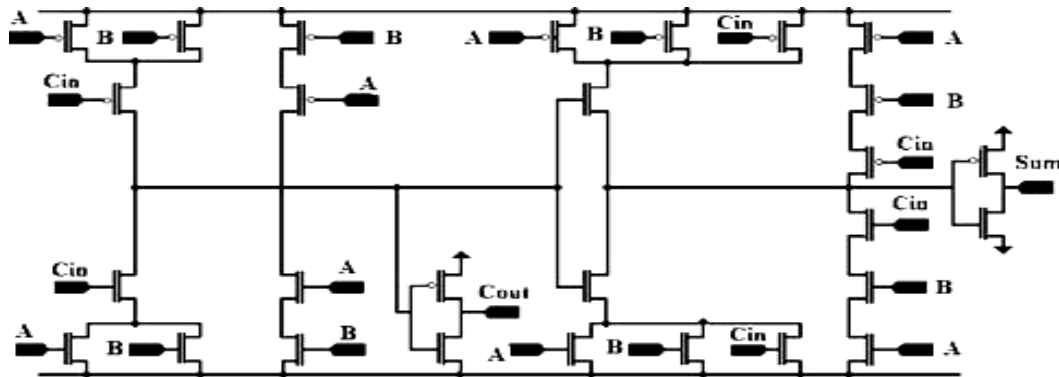
Figure 2. Conventional CMOS full adder with 28T Source: J.M Rabaey et al,. *Digital Integrated Circuits, Prentice Hall Publication (2003).*

The half adder logic can be realized setting Cin as zero [4]. During simulation Cin is set as ground (GND=Vss=0 volts) for CMOS 28 T half adder modules. The CMOS inverters are placed at the Carry out and Sum nodes in order to read the logic during actual verification.

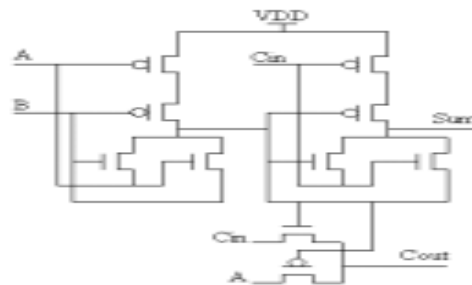## 2.2. 10 Transistor (10T) Adder

Figure 3. SERF full adder. Source: R Shalem et al., *A novel low power energy recovery full adder cell (Proceedings of the Great Lakes Symposium on VLSI (1999).*

The 10 transistor SERF adder is considered to be efficient in both low power consumption and less chip area [5]. In non- energy recovering circuits the charge from load capacitance during high is directly dumped to the ground (GND) during low logic level. In contrast, SERF adder reuses charge which the load capacitance during logic high to excite the gates rather than dumping the charge to the GND [5].

The circuit is shown in figure 3 which consists of two exclusive NORs realized by four transistors. The Carry Out is calculated by multiplexing inputs A and carry in (Cin). The sum is generated from the output of second stage exclusive NOR. If there is a capacitor charging at the output node of the first exclusive NOR and if initially, A=B=0, and A goes to high. When A and B both equal to low the capacitor is charged by VDD. In the next stage when B goes to high keeping A fixed at low, the capacitor discharges through A. Some charge is retained in A. Hence when A goes high it is not required to be charged fully. So the energy consumption is well managed and low here [5].

3. MULTIPLIER ARCHITECTURES

The multipliers are the well organised array of adder cells [4]. The performance and characteristics of the multipliers depend upon the algorithm in which they are based on [4]. Due to the emphasis of low power design, speed is not only the criterion for design objective. Therefore, designing multipliers with low power adder modules is essential keeping an eye on the

consumer market of portable electronic devices. In this paper, we have designed and characterized three well-known multipliers viz. The 4 Bits Array multiplier, the 4 bits Carry Save Multiplier and 4 bits Baugh Wooley Multipliers.

3.1. Bits Array Multiplier

Bit Array multiplier has a simple expandable structure which makes it easy to understand. In Bit Array Multiplier, the partial product is generated by multiplying multiplicand and multiplier bits [4]. The partial products are placed according to the correct shift in bit orders and then are added. If there are N partial products in the Bit – Array multiplier, (N-1) bit adders are required. Figure 4 shows the schematic of 4 bit- array multiplier. There is more than just one critical path in the Bit-Array multiplier.
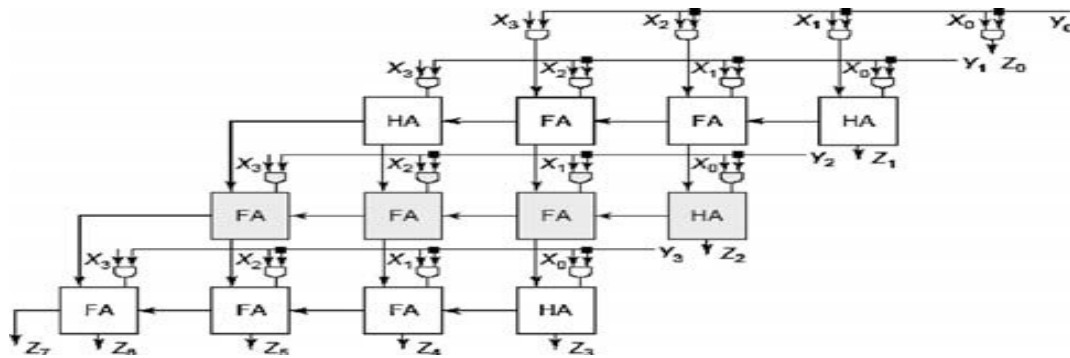

Figure4. 4bits Array Multiplier. Source: J.M Rabaey Y et al., *Digital Integrated Circuits, Prentice Hall Publications (2003).*

Theoretically, the approximate equation to calculate the propagation delay of these paths is shown below.

$$\Delta T = Tand + Tsum + [(Y-1) + (X-2)]Tcarry \qquad (8)$$

Where, *Tsum* is the delay between Carry in (Cin) and the sum bit of full adder, *Tand* is the delay of the AND gates, Y is the width of multiplicand, X is the width of multiplier and *Tcarry* is the propagation delay of the input and output carry [4].

3.2. Carry Save Multipliers

Carry-Save multiplier has the simple expandable structure like the Bits- Array multiplier. The only difference in algorithm is that in Carry Save multiplier the output carry bits are passed diagonally downwards instead of only to the right as the multiplication result does not change while doing so. The literature [4] has shown that in the final stage the sums and carries are fed in a fast carry adder usually by using fast- carry-look ahead adder. It is slightly bigger than the Bits array in the area. However, it only has one critical path.
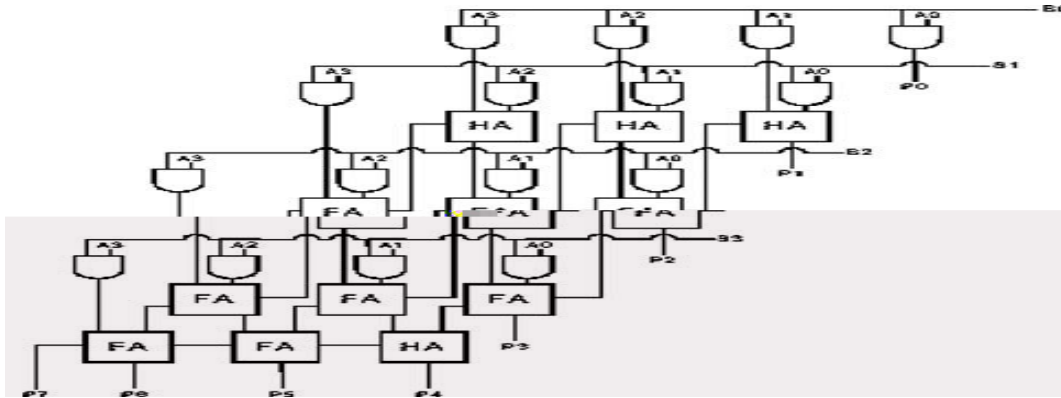
Figure5. 4 bits Carry-Save multiplier. Source: J.M Rabaey Y et al., *Digital Integrated Circuits, Prentice Hall Publications (2003).*

The schematic of 4 bits Carry-Save multiplier is shown in figure 5. Theoretically, the propagation delay of this multiplier is given by equation (9).

$$\Delta T = Tand + Tfinal + (X-1)Tcarry \tag{9}$$

Where *Tcarry* is the delay between input and output carry, X is the number of partial product stages, *Tfinal* is the delay of final stage carry look ahead adder and *Tand* is the delay of the AND gate [4].

3.3. Baugh Wooley Multiplier

Baugh Wooley multiplier has different algorithm than Bits- Array and Carry- Save multipliers. It is used to perform 2's complement multiplication and effectively handles the signed bits. The N x N Baugh Wooley multiplication algorithm is given by equation (10).

$$X \times Y = -2^{2N-1} + (\overline{X_{N-1}} + \overline{Y_{N-1}} + X_{N-1}Y_{N-1})2^{2N-2} + \sum_{0}^{N-2}\sum_{0}^{N-2} X_i Y_j \, 2^{i+j} + (X_{N-1}Y_{N-1})2^{2N-1} + \sum_{0}^{n-2} Y_{N-1}\overline{x_i} \cdot 2^{i+N-1} + \sum_{0}^{N-2} X_{N-1}\overline{Y_i}2^{i+N-1} \tag{10}$$

Where, X and Y are N-bits operand and their product is 2N bits number [4]. The Schematic of 4 bits Baugh Wooley Multiplier is shown in figure 6. The delay of Baugh Wooley Multiplier is similar to that of Bit-Array multiplier as it has also more than one critical path.
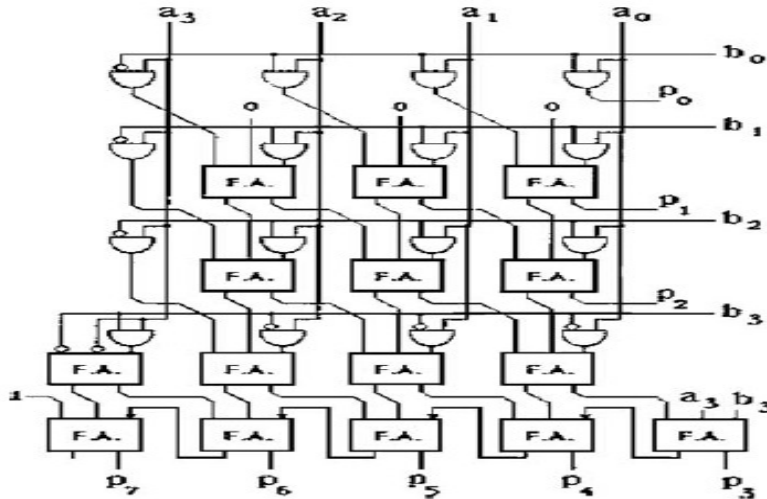
Fig6. 4 bits Baugh Wooley multiplier. Source: J.M Rabaey Y et al., *Digital Integrated Circuits, Prentice Hall Publications (2003).*

4. SIMULATION SET UP AND RESULTS

The CMOS sub-circuit of the CMOS AND gate, CMOS full adders and half adders and SVL circuits were created in HSPICE decks specifying the input and output nodes. The global variables such as supply voltage and ground were specified respectively as Vdd and Vss. These sub-circuit programs are called each time when they are required by the multiplier architecture. CMOS multiplier circuits' netlists are created with different combination of adders modules. The functionality of each circuit, CMOS AND, CMOS full adders and half adders were verified before creating the multiplier architecture net lists. The respective logic truth tables of half adder, full adder, CMOS AND gate and inverters were used during the verification. After extracting the multiplier architecture net lists, each multiplier circuits with different adder modules combination were simulated and verified to be functioning correctly before proceeding ahead for power and delay calculations. These analyses are called the transient analysis and read on the Cscope of the Hspice. Multipliers functionality verification can be done with number of different methods and approaches. In multiplier function verification, we chose a typical 4bits by 4 bits multiplying method where partial products generated are added to produce the final product in the form of [P7….to… P0] shown by equation (11) below.

$$a \ 3 \ a \ 2 \ a \ 1 \ a \ 0$$
$$Xb \quad 3 \ b \ 2 \ b \ 1 \ b \ 0$$
$$\text{--- --- --- --- --- --- --- --- --- --- --- --- ---}$$
$$p \ 7 \quad p \ 6 \quad p \ 5 \quad p \ 4 \quad p \ 3 \quad p \ 2 \quad p \ 1 \quad p \ 0$$

$$(11)$$

We take the random two 4 bits numbers and find the final result of the multiplication in 8 bit number. Subsequently, we supply the same multiplier and multiplicand two 4 bits number through the inputs *a3a2a1a0* and *b3b2b1b0* in the multiplier netlist in Hspice software and check the results in Hspice Cscope readout. The corresponding 1s and 0s of [P7…P0]are compared to highs and lows of the Cscope output. If they match, the multiplier circuit is functioning correctly.

A total of twenty four different multiplier circuits' netlists of different adder modules combinations were created for the combination shown in table 2 below in Hspice decks and all of them were tested to be functioning correctly.
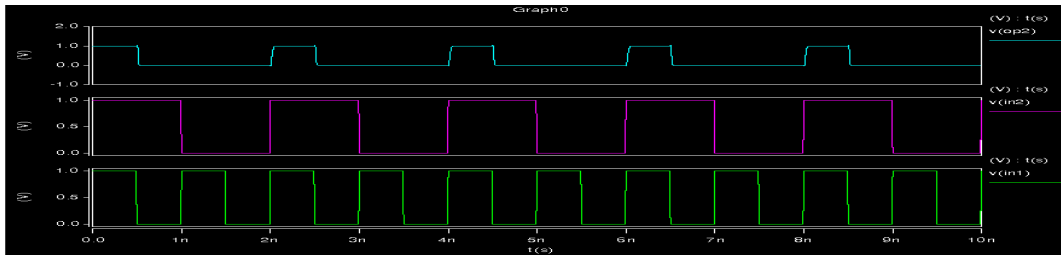

Fig7. Functionality verification of CMOS AND gate.

The net lists of the circuits were extracted and simulation was performed using UC Berkeley BSIM4 models available through Predictive Technology Model (PTM) which is a promising model file for accurate and predictive modeling of future transistors. All the CMOS circuits were implemented with *45nm* node technology in HSPICE.
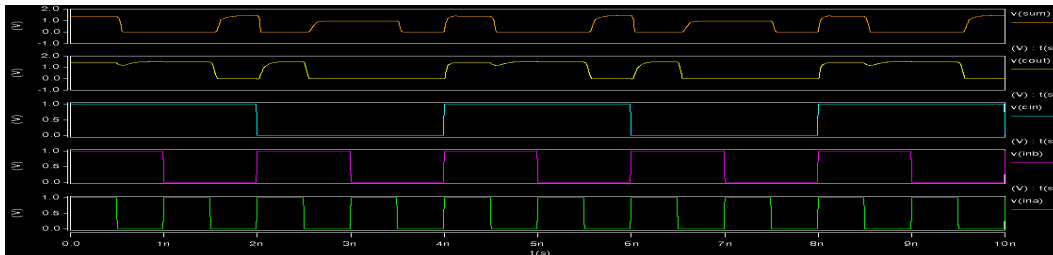

Fig8. Functionality verification of 28T CMOS full Adder with SVL circuit.

The simulations were run on a Red Hat Linux host machine. All the multipliers were compared and analyzed for stand-by leakage power, delay and dynamic power. The delays were measured for worst case scenarios i.e. always the worst case delay was considered for data pickup.
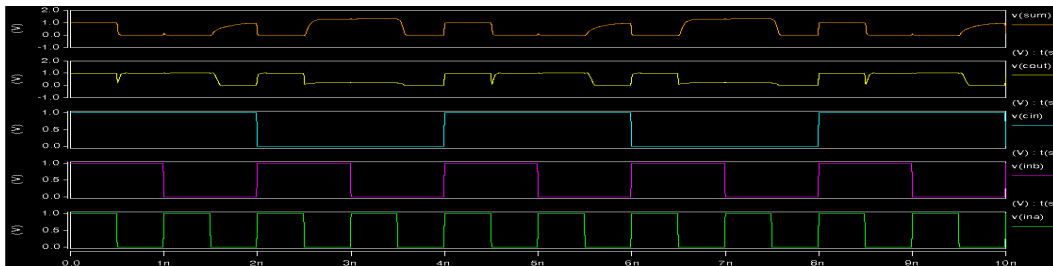

Fig 9. Functionality verification of 10 T SERF full adder with SVL circuit.

The delay measurements for the all combinations are tabulated for a convenient analysis. In the same fashion, the leakage and dynamic power is also presented in tabular form.

Table1. Delay Measurements

Delay Measurements	Bits Array	Carry Save	Baugh Wooley
Delay with SERF adder	1.46E-10 seconds	7.26E-09 seconds	2.02E-10 seconds
Delay with CMOS 28 T adder	1.46E-10 seconds	1.26E-08 seconds	3.66E-09 seconds
Delay with SERF applied with SVL circuit	6.60E-09 seconds	7.27E-09 seconds	3.05E-09 seconds
Delay with CMOS 28 T applied with SVL	9.12E-09 seconds	1.27E-08 seconds	2.74E-08 seconds

Table2. The stand-by Leakage and dynamic power dissipation of the 3 different multipliers with various combinations

multipliers power	Bits Array	Carry Save	Baugh Wooley
Leakage with 28 t	1.00E-04 watts	1.12E-04 watts	1.43E-04 watts
Dynamic with 28 t	1.10E-04 watts	1.05E-04 watts	1.36E-04 watts
Leakage with SERF	2.14E-05 watts	2.11E-05 watts	2.08E-05 watts
Dynamic with SERF	2.14E-05 watts	2.12E-05 watts	2.23E-05 watts
Leakage with 28 t applied with SVL	1.39E-06 watts	1.40E-06 watts	2.74E-06 watts
Dynamic with 28 t applied with SVL	5.80E-05 watts	2.25E-05 watts	1.93E-05 watts
Leakage with SERF applied with SVL	1.16E-06 watts	1.16E-06 watts	1.67E-06 watts
Dynamic with SERF applied with SVL	2.39E-05 watts	1.85E-05 watts	1.64E-05 watts

Table3. Area/transistor count

Adders multipliers	CMOS28T	SERF 10T	CMOS28Twith SVL	SERF10T With SVL
Bits Array	512	296	548	316
Baugh Wooley	624	354	669	399
Carry save	512	296	548	316

5. FUTURE WORK

Dual threshold CMOS technique can be applied into the multiplier circuits. There are certain critical and non- critical paths in the multiplier circuits. A higher threshold voltage can be assigned to the transistors in the non- critical paths and lower threshold voltage can be assigned to

the transistors in the critical paths as such the leakage current is minimized without compromising the performance [1]. Dual threshold CMOS can reduce leakage power in both stand-by and active mode of operation without a penalty on both area and delay [1].
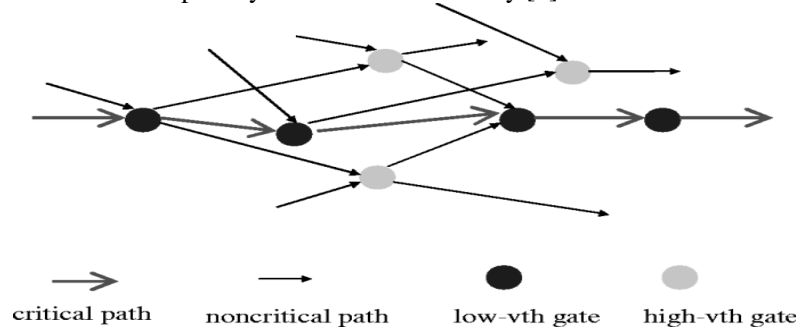

Figure12. Dual threshold Voltage circuitry

6. CONCLUSIONS

The table1 show the propagation delay of different multiplier circuits. The delay of multipliers with SERF adders applied with SVL circuit exhibit a huge difference compared to the rest two multiplier combinations applied with CMOS 28T Adder modules. The CMOS 28T Adder applied with SVL circuit has large penalty in area and have bad delays. The delay is *6.6nS* in Bits Array Multiplier with SERF Adder applied with SVL circuit vs. *9.12nS* in the same multiplier with CMOS 28 T Adder applied with SVL. It is *7.2nS* in Carry Save Multiplier with SERF Adder applied with SVL circuit vs. *12.7nS* in the same multiplier with CMOS 28T Adder applied with SVL circuit. It is *3.05nS* in Baugh Wooley multiplier with SERF Adder applied with SVL circuit vs. *27nS* in the same multiplier with CMOS 28T Adder applied with SVL circuit. The table2 show a comparison of stand-by leakage and dynamic power dissipation of different multiplier circuits applied with various combinations of adder modules and SVL circuit. Interestingly, the dynamic power dissipation has decreased for combinations that used SVL circuit because of low supply voltage, *VL* created by SVL circuit itself. Transistor count is proportional to area of the chip. Table 3 suggests that multipliers with SERF adder modules applied with SVL has less area compared to the multipliers with CMOS 28T adder modules applied with SVL circuit. The table2 shows that stand-by leakage power dissipation with SERF adder applied with SVL circuit in all three multipliers circuits is less compared to the same three multipliers with other combinations. The stand-by leakage power dissipation of multipliers with SERF adders applied with SVL circuit exhibit a significant difference compared to the rest two multiplier combinations applied with CMOS 28T Adder modules. The CMOS 28T Adder applied with SVL circuit has large penalty in area. The stand-by leakage power dissipation is *1.16µwatts* in Bits array multiplier with SERF Adder applied with SVL vs. *1.39µwatts* in the same multiplier with CMOS 28T Adder applied with SVL circuit. It is *1.16µwatts* in Carry Save multiplier with SERF Adder applied with SVL vs. *1.4µwatts* in the same multiplier with CMOS 28T Adder applied with SVL circuit. It is *1.67µwatts* in Baugh Wooley multiplier with SERF Adder applied with SVl circuit vs. *2.74µwatts* in the same multiplier with CMOS 28T Adder applied with SVL circuit. Therefore, the multiplier circuits with SERF Adder applied with SVL circuit outperform the multiplier circuits with CMOS 28T Adder applied with SVL circuit in terms of stand-by leakage power dissipation, area and delay. In other words, the SERF adders applied with SVL circuit are suited for ultra-low power design of CMOS multipliers circuits.

REFERENCES

[1] K. Roy, S. Mukhopadhyay and H. Mahmoodi-Meimand "Leakage Current Mechanisms and Leakage Reduction techniques in Deep-Submicrometer CMOS Circuits" Proceedings of the IEEE, Vol. 91, No.2, February, 2003.

[2] T. Enomoto, Y. Oka and H. Shikano, "A Slef-Controllable –Voltage –Level (SVL) Circuit for Low-Power, High-Speed CMOS Circuits", IEEE Journal of Solid –State Circuits, Vol. 38, No. 7, July 2003, Pages 1220-1226.

[3] A. Agarwal, S. Mukhopadhyay, A. Raychowdhury, K. Roy " Leakage Power Analyis And Reduction for Nanoscale Circuits" IEEE Computer Society, Vol. 26, April 2006, pages 68-80.

[4] D. Kudithipudi and E. John, "Implementation of Low Power Digital Multipliers using 10 Transistor Adder Blocks" Journal of Low Power Electronics, Vol. 1 2005, pages 1-11.

[5] R. Shalem, L.K John and E. John, "A Novel Low Power Energy Recovery Full Adder Cell", Proceedings of the Great Lakes Symposium on VLSI (1999), Pages 380-383.

[6] M. J. Rani and S. Malarkann, "Leakage Power Reduction and Analysis of CMOS sequential Circuits", International Journal of VLSI design and Communication Systems, Vol. 3, No. 1 February 2012.

[7] K. Kim, N. Park, Y. Kim and M. Choi, "Leakage Minimization Technique for Nanoscale CMOS VLSI based on Macro-Cell Modelling", IEEE Design & Test of Computers, Vol. 24 July 2007 pages 322-330.

[8] F. Fallah and Massoud Pedram " Standby and Active Leakage Current Control and minimization in CMOS VLSI Circuits", IEICE Leakage- Review-Journal.

[9] M. Singh, S. Akhase, S. Sharma " Leakage power reduction techniques of 45nm of Static Radom Access Memory (SRAM) cells", International Journal of Physical Sciences, vol. 6, December 2011, pages 7341-7353.

[10] J. Deshmukh, K. Khare "Standby leakage Reduction in nanoscale CMOS VLSI circuits", Proceedings of the International Conference and workshop on Emerging trends in Technology, 2010 pages 911-914.

[11] J.M Rabaey Y et al., Digital Integrated Circuits, Prentice Hall Publications 2003.

[12] Ratul kr. Baruah " Design of a low power low voltage CMOS opamp", International Journal of VLSI design and Communication system, Vol. 1, No. 1 March 2010.

[13] Neha Gupta etl., "Low power low voltage bulk driven balanced OTA", International Journal of VLSI design and Communication system, Vol. 2, No. 4 December2011.

[14] Y. Sunil Gavaskar Reddy and V.V.G.S Rajendra Prasad " Power comparision of CMOS and adiabiatic full adder circuits", International Journal of VLSI design and Communication system, Vol. 2, No. 3 September 2011

Authors

Deeprose Subedi received his Bachelor of Science in Physics from Tribhuvan University, Kathmandu, Nepal and is currently pursuing Bachelor of Science in Electrical Enginering from University of Texas at San Antonio. His research interests include, low power vlsi, Intregrated Circuit design, CMOS analog and mixed signal systems design and power electronics. This paper is the spin out result of a NSF funded research entitled "Experimental Study on Computer Architecture and Performance Evaluation" where he participated in summer 2012 at University of Texas at San Antonio. He is a Student member of IEEE.

Dr. Eugene John is the Professor of electrical and computer engineering at the University of Texas at San Antonio. His research interests include low power techniques, power efficient circuits and systems, multimedia and embedded systems and performance evaluation. He has a Ph.D. in electrical engineering from the Pennsylvania State University. He is a senior member of the IEEE.