QUATERNARY LOGIC AND APPLICATIONS USING MULTIPLE QUANTUM WELL BASED SWSFETS

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ABSTRACT

This paper presents Spatial Wavefunction-Switched Field-Effect Transistors (SWSFET) to implement efficient quaternary logic and arithmetic functions. Various quaternary logic gates and digital building blocks are presented using SWSFETs. In addition, arithmetic operation with full adder using novel logic algebra is also presented. The SWSFET based implementation of digital logic, cache and arithmetic block results in up to 75% reduction in transistor count and up to 50% reduction in data interconnect densities. Simulations of quaternary logic gates using the BSIM equivalent models for SWSFET channels are also described.

KEYWORDS

Quaternary Logic, Multi-Channel, Nanotechnology, SWSFETs

1. INTRODUCTION

The concept of SWSFET was introduced by Jain *et al.* [1]. SWSFETs offer multiple channels in a single transistor. In this paper we are discussing multichannel SWSFETs and presenting efficient quaternary logic gates and building blocks. The designs could potentially lower the device count by 75% for the same functionality and hence could significantly reduce the die size and data interconnect metal densities.

2. SPATIAL WAVE SWITCHED FIELD EFFECT TRANSISTOR (SWSFET)

In this section we will discuss different topologies of SWSFETs and related quantum mechanical simulations. Figure 1 shows the cross-sectional schematic of a two channel Si-SiGe SWSFET. Here the Si wells are grown on $Si_{0.75}Ge_{0.25}$ relaxed layer. It is a type-II structure with $Si_{0.5}Ge_{0.5}$ barrier layers.

Figure 2 illustrates two channels corresponding to each quantum well. Generally, the quantum wells are asymmetric having different thicknesses. As the gate voltage V_G is applied above threshold V_{TH1}, the electrons are confined in well W2, the lower of the two wells. As the gate voltage is further increased ($V_G > V_{TH2}$), the electrons from W2 starts transferring to the upper well W1. Eventually, all electrons would belong to the upper level. Since the gate voltage is higher when the electrons transfer to the upper well W1, it has a greater density of electrons, and hence higher drain current.

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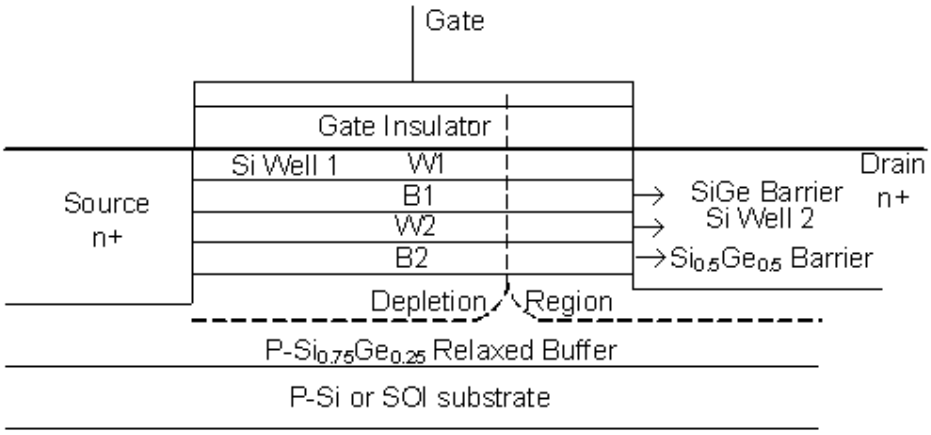


Figure 1. Layer topology of two quantum well SiGe-Si SWSFET.

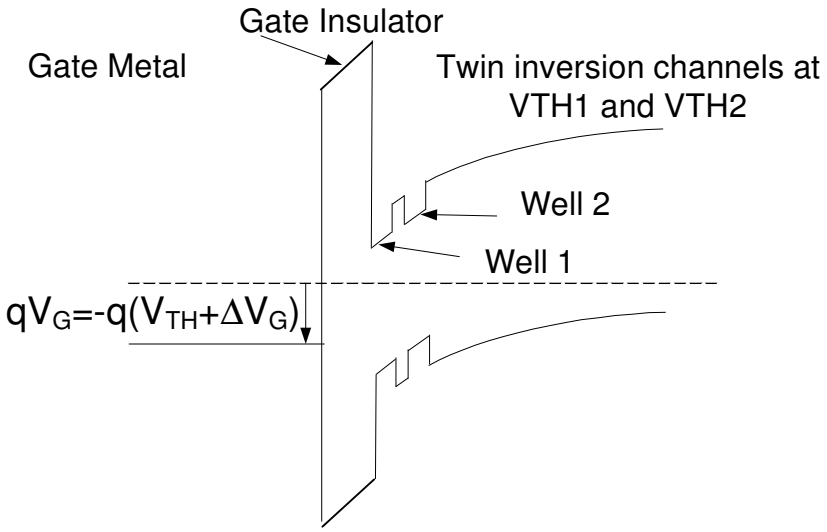


Figure 2. Schematic energy band diagram of two-well SWSFET structure.

2.1. Two-Well SWSFET

Figure 3(a)-(b) presents the quantum mechanical simulations for a two well SWSFET. At a gate voltage of -1.5V, the electron wavefunction is confined to W2. The wave function moves with changes in the gate voltage to 0.5V from lower well W2 to the upper well W1. Hence the carrier concentration also moves from lower to upper well, with this increased gate voltage.

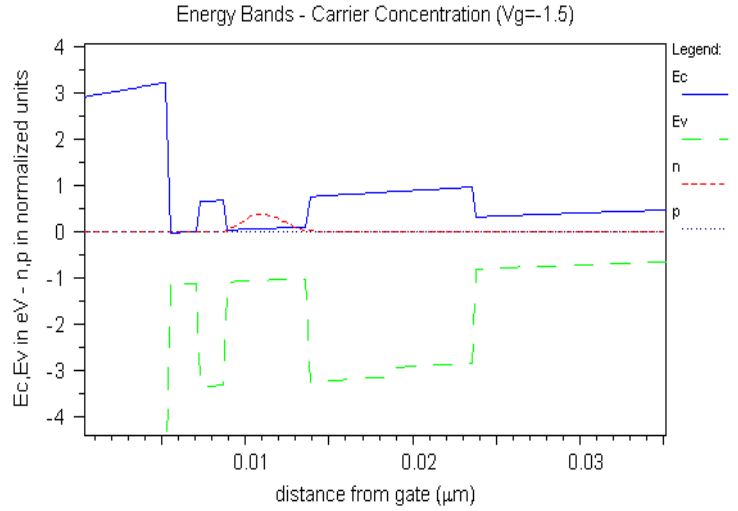


Figure 3 (a). Quantum mechanical simulations showing carriers available in lower well only.

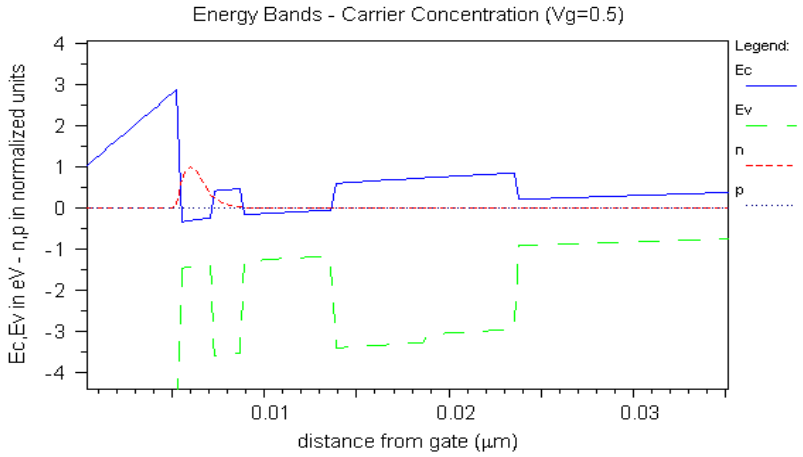


Figure 3 (b). Quantum mechanical simulations showing carriers available in upper well only

2.2. Three-Well SESFET

Three-well SWSFET was designed with Ge wells and ZnSSe barrier layers. Unlike Fig. 1, it is a type I structure. Figure 4 shows the topology of the three-well design. Figure 5(a) and (b) present the quantum mechanical simulations for this structure. The carriers move from lower most well W3 to the upper most well W1with the change in gate voltage as show in figure 5(a) and (b). It should be noted that the gate voltage at which the wavefunction transfers, will change depending on the work function, gate insulator thickness and other parameters.

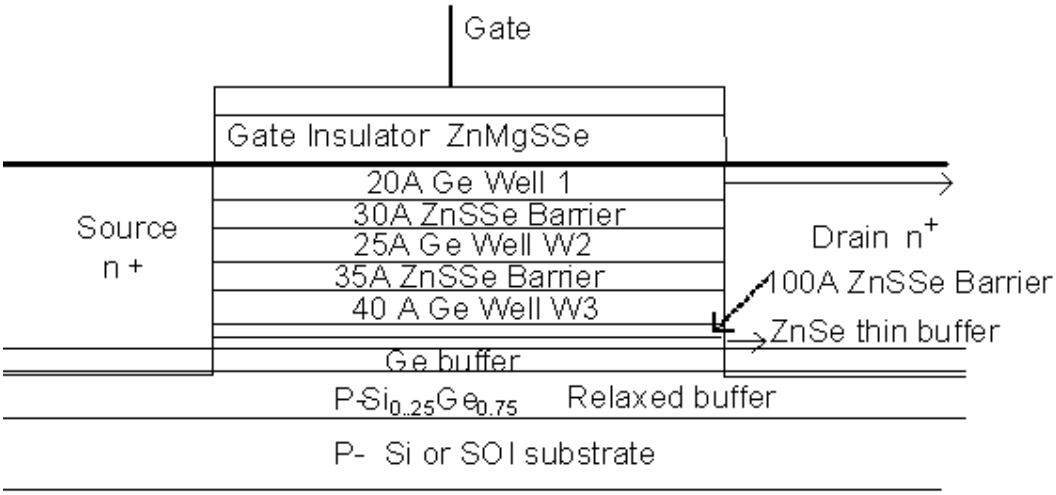


Figure 4. Layer structure for three well SWSFETs

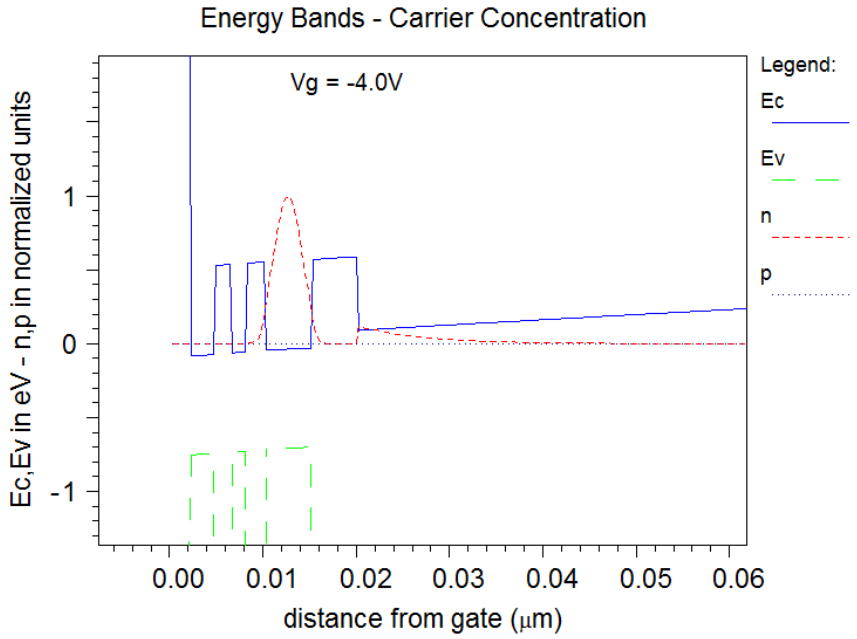


Figure 5 (a). Quantum mechanical simulations showing carriers available in lower most well of three well SWSFET.

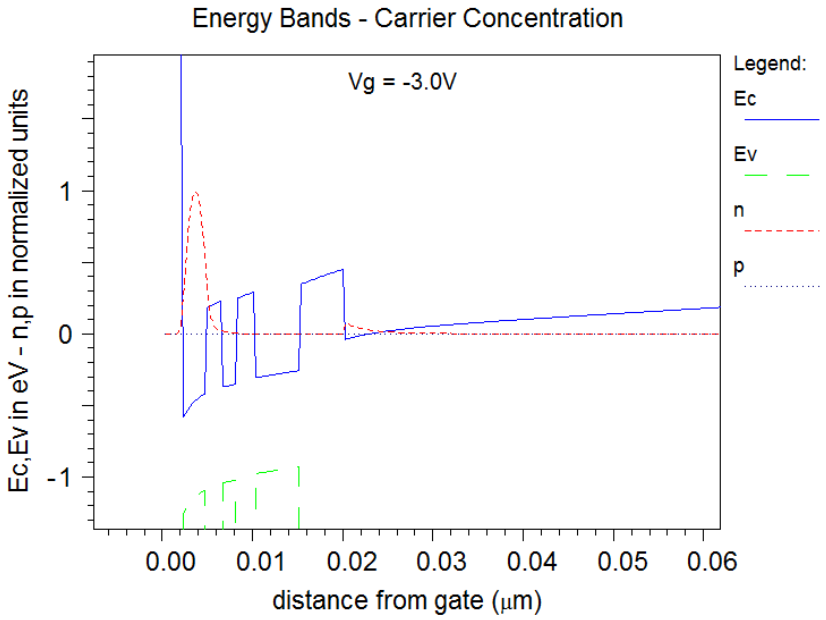


Figure 5 (b). Quantum mechanical simulations showing carriers available in upper most well of three well SWSFET.

2.3. Four-Well SWSFET:

Figure 6 presents the four well SWSFET structure with InGaAs wells and AlInAs as barriers. Figure 7 (a) and (b) shows the quantum mechanical simulations for this structure with movement of carriers from lower wells to the upper wells with the change in the gate voltage.

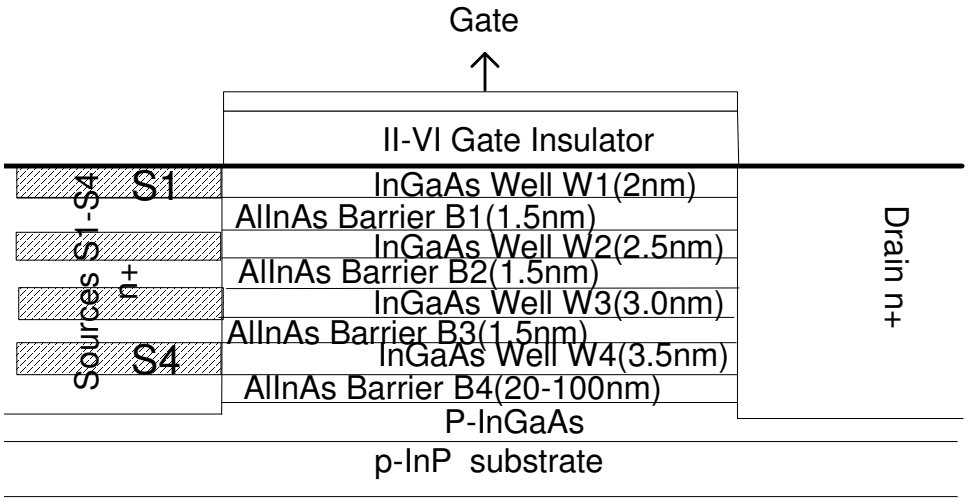


Figure 6. Design of four well SWSFET layer structure

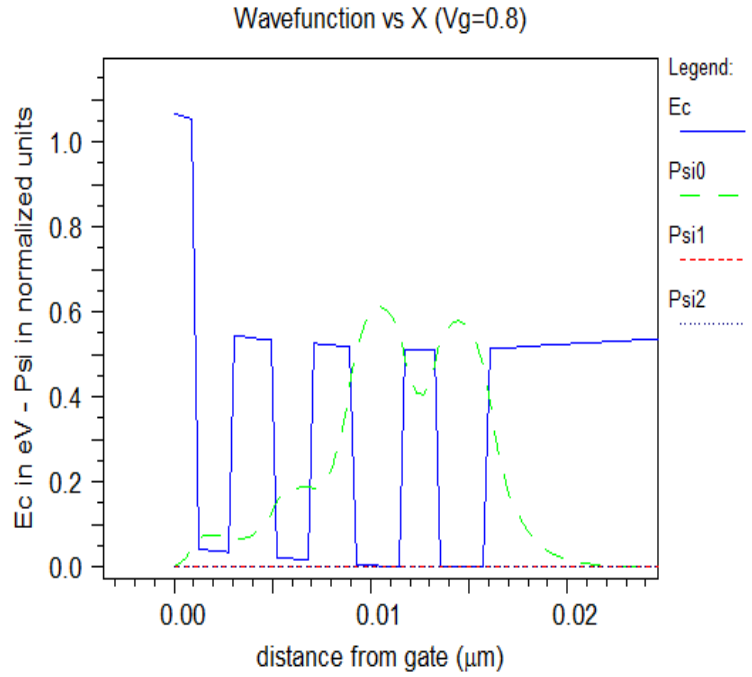


Figure 7 (a). Quantum mechanical simulations showing carriers available in lower wells of four well SWSFET

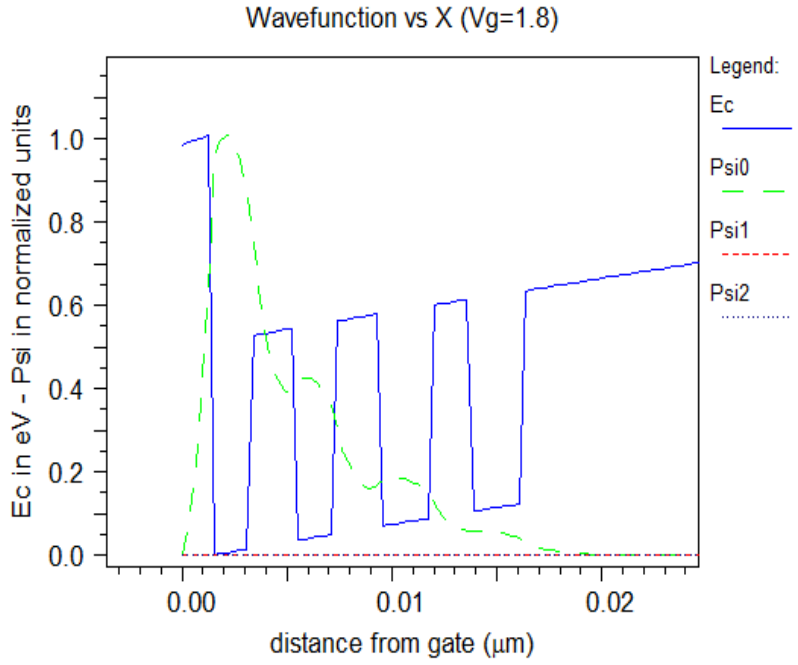


Figure 7 (b). Quantum mechanical simulations showing carriers available in upper wells of four well SWSFET

2.4. Fabricated SWS MOS Device

Figure 8 shows cross-sectional schematic of a fabricated SWS-MOS structure which is used to demonstrate carrier transfer as a funciton of the gate voltage. Figure 9 presents the measured C-V characteristics of this device. The existence of the peak in C-V is a proof of carrier transfer from one well to the other. The capacitance peak (gate voltage Vg=0 V) corresponds to charge (holes) in the lower well W2 as the device moves from threshold towards accumulation. The transfer of carriers to upper well W1 takes place at V_g=-2.0 V in this asymmetrically coupled quantum well InGaAs SWS-FET device. The inversion peak (~-3.8V) is not that pronounced. Simulation has verified the capacitance behaviour showing two peaks, one near the accumulation and the other near the inversion regime [1,4].

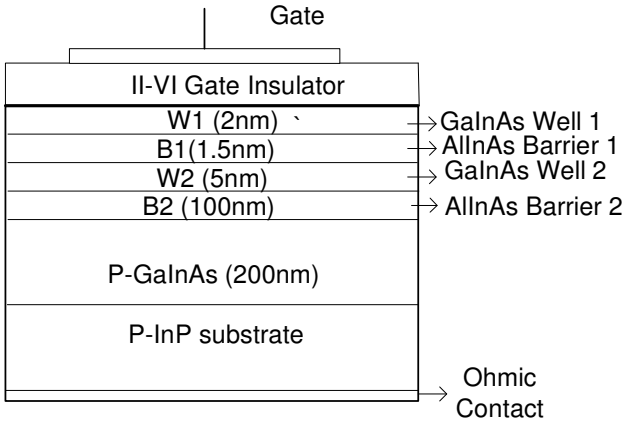


Figure 8. Structure of fabricated two-well SWSFET with layer topology.

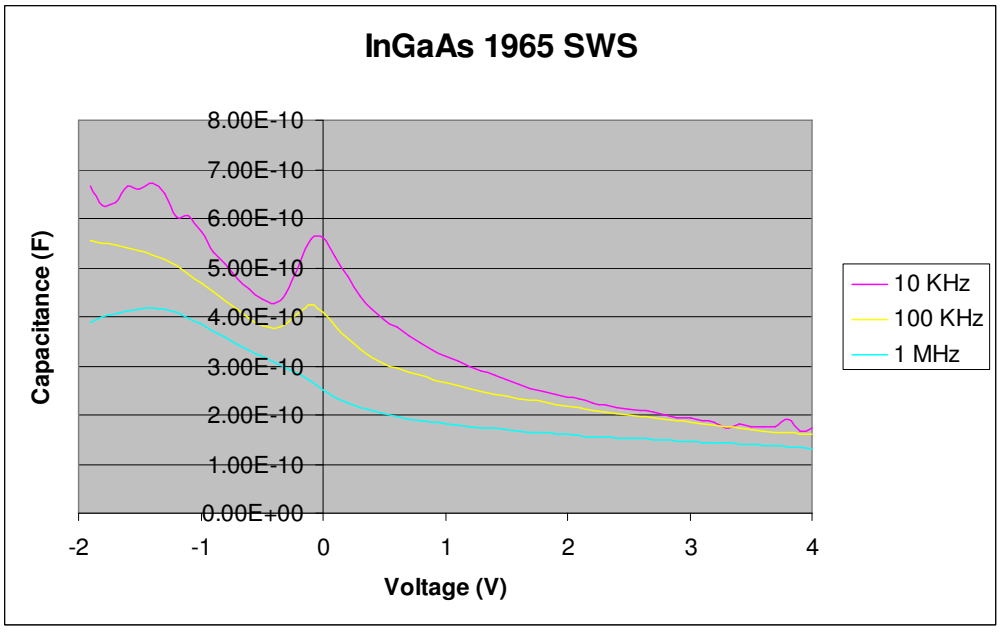


Figure 9. C-V characteristics for a fabricated two-well InGaAs SWSMOS structure

3. QUATERNARY LOGIC, LOGIC GATES AND OTHER DIGITAL BUILDING BLOCKS USING SWSFET.

3.1. Quaternary Logic

In the last section we discussed SWSFET with multiple channels and the control over channel carrier concentration with change in gate voltages. The multiple channels in SWSFET offers design possibilities that are not available using single channel CMOS transistors. To develop efficient logic gates we decided to use the quaternary logic. Figure 10 compares the binary logic used in CMOS based digital cells, with the quaternary logic, we decided to use for SWSFET based cells.

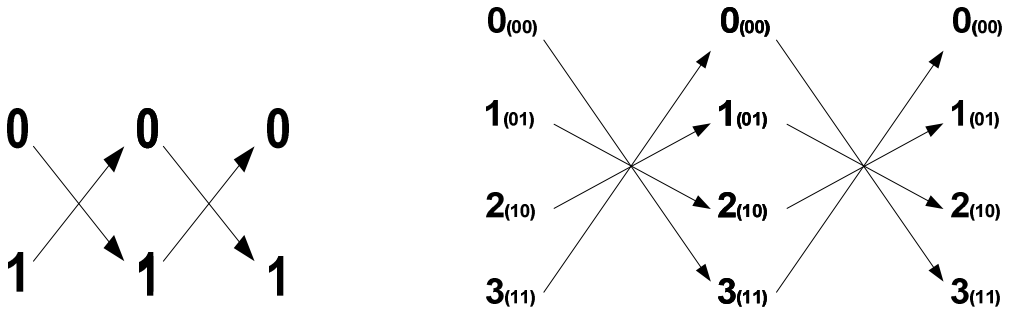


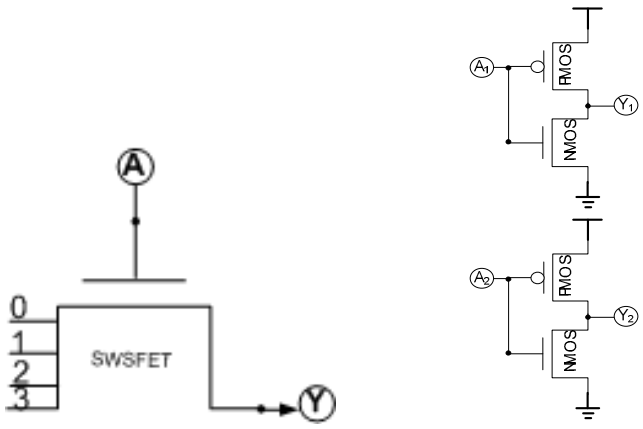
Figure 10: Binary logic verses Quaternary logic with two inversions.

3.2. Logic Cells

In this section we are presenting the Quaternary logic building blocks along with implemented truth tables for the logic levels presented in sec 3.1.

3.2.1 NOT Gate

The NOT gate implementation with SWSFET as well as CMOS is shown in figure 11. The related truth table is presented in table I. Two bit NOT gate implementation with CMOS binary logic requires four transistors as compared to one SWSFET using quaternary logic.



(a) (b)

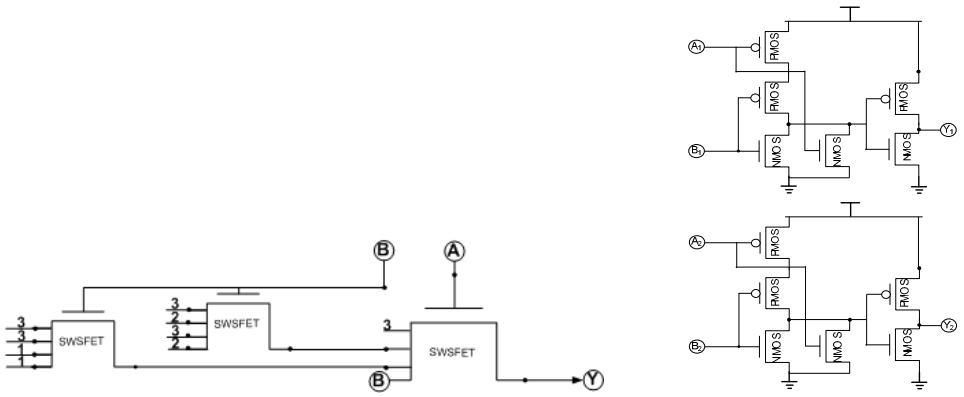
Figure 11: NOT Gates (a) Quaternary NOT gate implemented with SWSFET (b) Two binary NOT gates implemented with CMOS binary logic.

Table I: Truth table implementing NOT Gate.

#	A (A_1,A_2)	Y(Y_1,Y_2)
1	0 (00)	3 (11)
2	1 (01)	2 (10)
3	2 (10)	1 (01)
4	3 (11)	0 (00)

3.2.2 OR Gate

Two bit OR gate implementations using SWSFET with quaternary logic and CMOS with binary logic are presented in figure 12. The truth table for the implemented OR-gates is presented in table II. Two bit OR gate implementation in CMOS based binary logic requires twelve transistors as compared to three transistors required SWSFET based implementation with quaternary logic.



(a) (b)

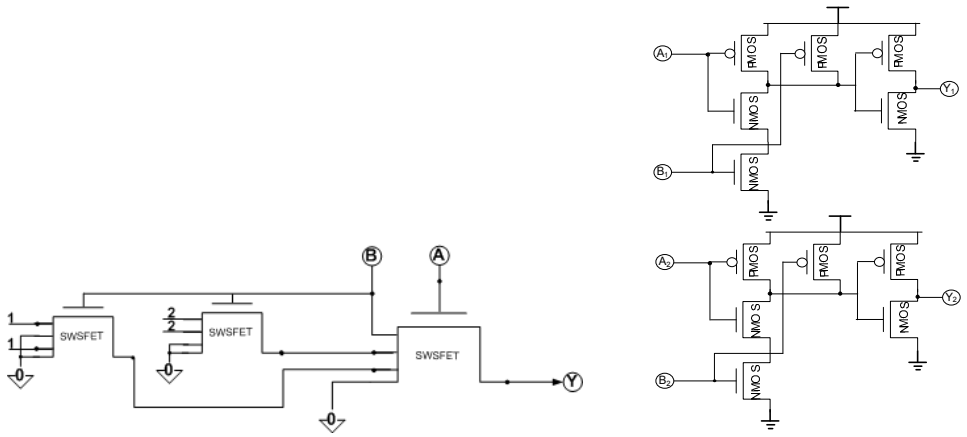
Figure 12: OR Gates (a) Quaternary OR gate implemented using SWSFET (b) Two binary OR gates using CMOS.

Table II: Truth table implementing OR Gate.

S/N	A(A_1,A_2)	B(B_1,B_2)	A OR B = Y(Y_1,Y_2)
1	00	00	00
2	00	01	01
3	00	10	10
4	00	11	11
5	01	00	01
6	01	01	01
7	01	10	11
8	01	11	11
9	10	00	10
10	10	01	11
11	10	10	10
12	10	11	11
13	11	00	11
14	11	01	11
15	11	10	11
16	11	11	11

3.2.3 AND Gate

The AND gate implementations using SWSFET with quaternary logic and CMOS with binary logic are shown in figure 13. The related truth table is presented in table III. Two bit AND gate implementation in CMOS based binary logic requires twelve transistors as compared to three transistors required SWSFET based implementation with quaternary logic.



(a) (b)

Figure 12: AND Gates (a) Quaternary AND gate implemented using SWSFET (b) Two binary AND gates using CMOS.

Table III: Truth table implementing AND gate

	$A(A_1,A_2)$	$B(B_1,B_2)$	A AND B = $Y(Y_1,Y_2)$
1	00	00	00
2	00	01	00
3	00	10	00
4	00	11	00
5	01	00	00
6	01	01	01
7	01	10	00
8	01	11	01
9	10	00	00
10	10	01	00
11	10	10	10
12	10	11	10
13	11	00	00
14	11	01	01
15	11	10	10
16	11	11	11

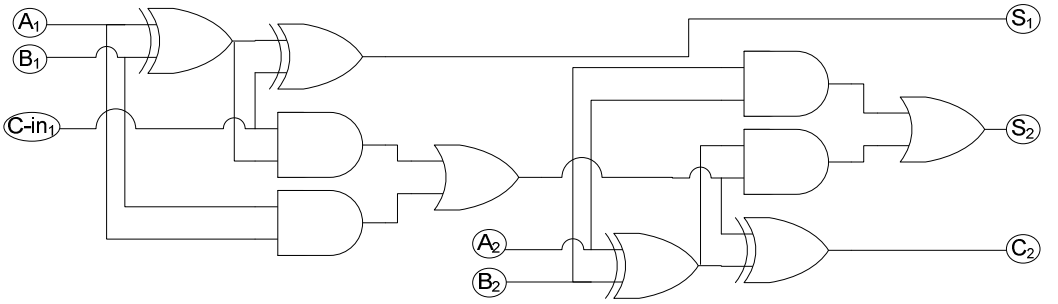
3.2.4 Full Adder

Arithmetic blocks are important and integral part of the processors. We are introducing quaternary full adder using SWSFET. Figure 14 shows full adder implemented using SWSFET with quaternary logic and using CMOS logic with binary logic. The truth table for the implemented full adder is presented in table IV. A simple full adder implementation in CMOS with binary logic for two bits requires eighty transistors as compared to eleven required for the

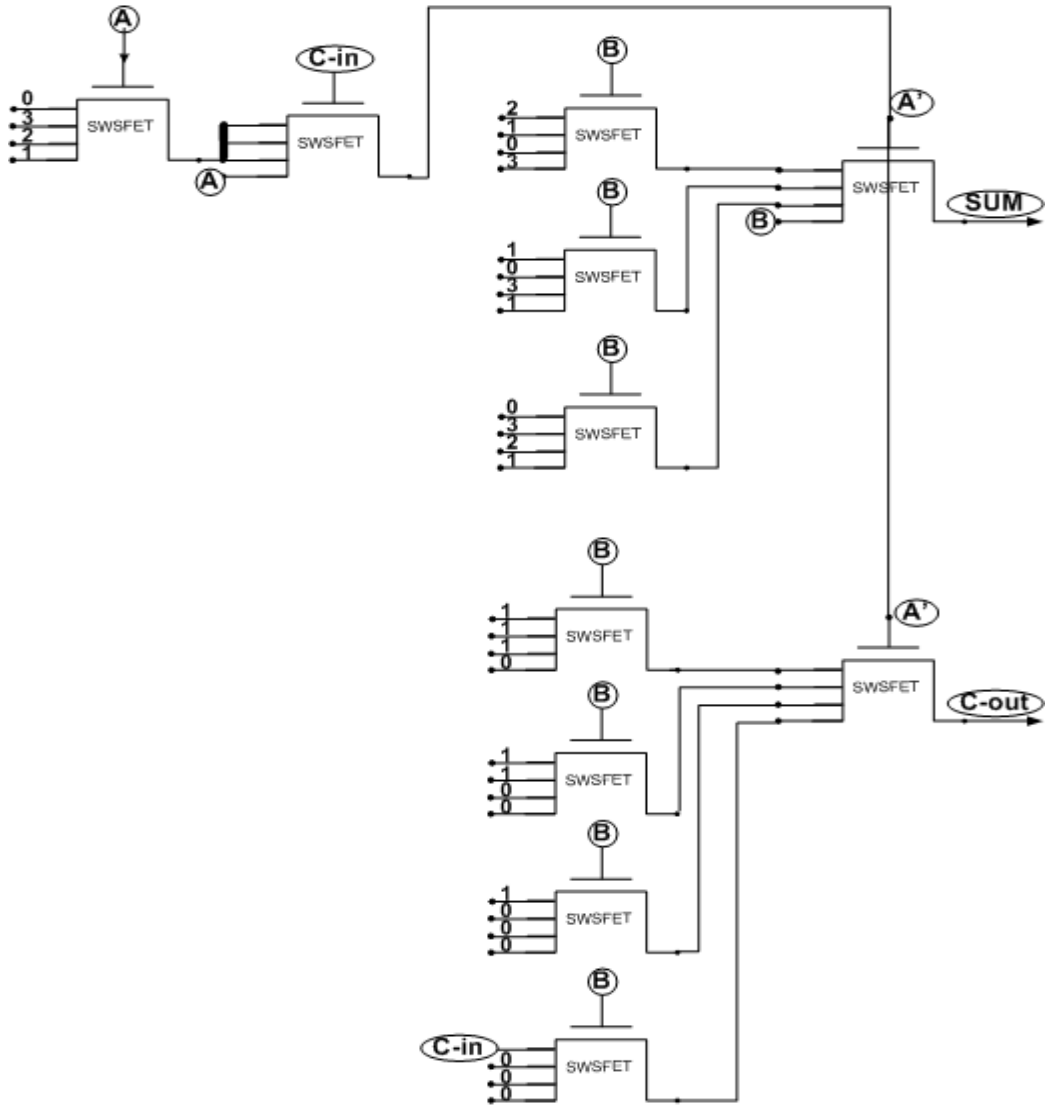
adder presented here using SWSFET with quaternary logic. Also the longest delay path in SWSFET implementation is three transistors as while in CMOS based implementation it is five gates as shown in figure 14.

Table IV: Truth table implementing two bit Full adder.

	Carry-in	**A**	**B**	**Sum**	**Carry-Out**
1	0	00	00	00	0
2	0	00	01	01	0
3	0	00	10	10	0
4	0	00	11	11	0
5	0	01	00	01	0
6	0	01	01	10	0
7	0	01	10	11	0
8	0	01	11	00	1
9	0	10	00	10	0
10	0	10	01	11	0
11	0	10	10	00	1
12	0	10	11	01	1
13	0	11	00	11	0
14	0	11	01	00	1
15	0	11	10	01	1
16	0	11	11	10	1
17	1	00	00	01	0
18	1	00	01	10	0
19	1	00	10	11	0
20	1	00	11	00	1
21	1	01	00	10	0
22	1	01	01	11	0
23	1	01	10	00	1
24	1	01	11	01	1
25	1	10	00	11	0
26	1	10	01	00	1
27	1	10	10	01	1
28	1	10	11	10	1
29	1	11	00	00	1
30	1	11	01	01	1
31	1	11	10	10	1
32	1	11	11	11	1



(a)



(b)

Figure 14: Full adders (a) Two binary full adders implemented using CMOS and (b) Quaternary full adder implemented using SWSFET

3.2.5 Quaternary Latch

All the digital logic could be implemented using NOT, AND & OR gates. An additional building block for digital processors is a latch or flop. A quaternary latch implementation using SWSFET is shown in figure 15. The related truth table is presented in table V. A similar two bit latch implementation for two bits using CMOS binary logic would require about twelve transistors as compared to four required using SWSFET with quaternary logic.

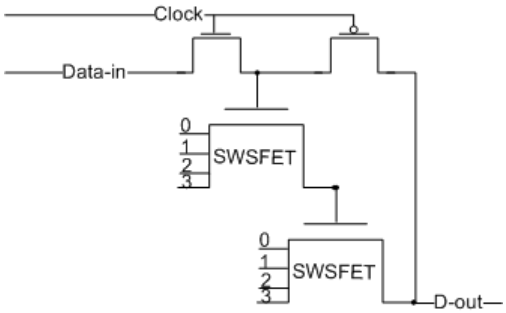


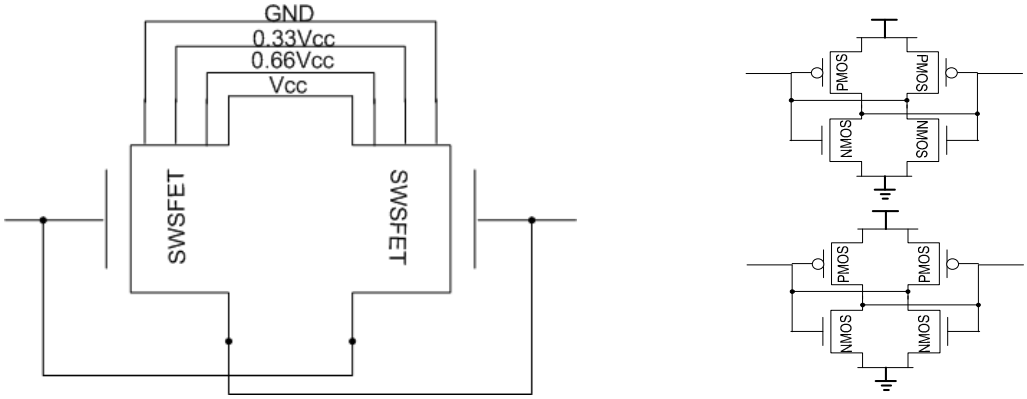
Figure 15: Quaternary Latch implanted using SWSFET.

Table V: Truth table for a latch

#	Clock	D-Out
1	0	D-Out
2	1	Data-In

3.2.6 SRAM Cell

Digital microprocessors today require massive amount of on die caches. Performance processors use over 50% of the die area for caches [5,6]. We are presenting the quaternary logic based cache implementation using SWSFET. Figure 16 shows the SRAM cell implementations using SWSFET with quaternary logic along with existing CMOS with binary logic. Two bit SRAM cell implementation in CMOS with binary logic requires eight transistors as compared to two transistors required using SWSFET with quaternary logic.



(a) (b)

Figure 16: SRAM cells (a) Quaternary SRAM cells implemented using SWSFET (b) Two binary SRAM cells implanted using CMOS.

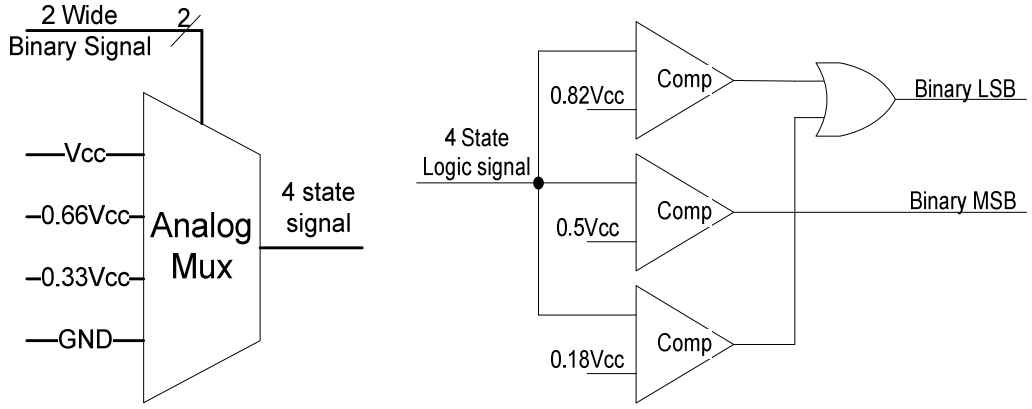
In this section we have discussed basic building blocks of a digital micro processor. Also we have seen some comparison between the quaternary and binary implementation. Table VI gives the summary of transistor count comparison for implementations using SWSFET vs. CMOS for digital building blocks.

Table VI: Transistor count per two bits for digital building blocks.

S/N	Cell	CMOS Count	SWSFET Count
1	NOT	4	1
2	AND	12	3
3	OR	12	3
4	Full Adder	80	11
5	SRAM	8	2
6	Latch	16	4

3.2.7 Integration with Binary logic

We also designed a simple set of circuits to convert binary logic signals to quaternary logic signals and vice versa. Figure 17 presents these simple designs. This helps integrate CMOS based binary logic along with SWSFET based quaternary logic designs on the same die.

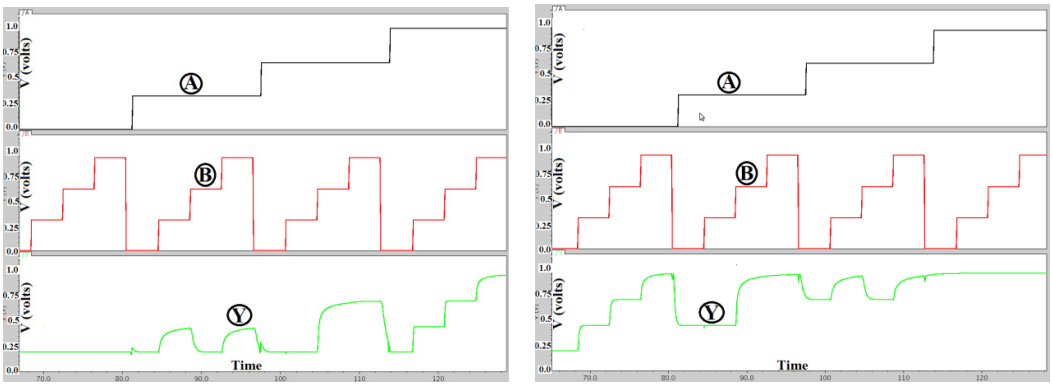


(a) (b)

Figure 17: (a) Binary logic to quaternary logic conversion circuit (b) Quaternary logic to binary logic conversion circuit.

4. SIMULATIONS

We simulated the basic gates using the BSIM equivalent channel models for the quaternary logic using SWSFETs. Figures 18 and 19 give the simulation results for quaternary AND gate, OR gate and NOT gate, in agreement with corresponding truth tables presented in the previous section.



(a) (b)

Figure 18: Simulation results for quaternary gates using BSIM equivalent channel models in agreement with tables II and III (a) SWSFET based two input quaternary AND gate (b) SWSFET based two input quaternary OR gate.

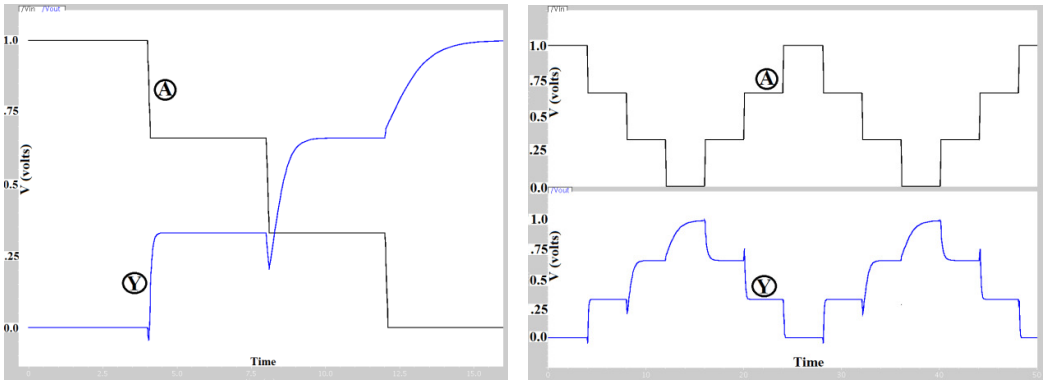


Figure 19: Simulation results for SWSFET based quaternary inverter using BSIM equivalent channel models.

5. CONCLUSIONS

Spatial wavefunction-switched field-effect transistors (SWSFETs) have multiple coupled channels allowing the location of the charge to be selected by the gate voltage, and providing a pathway for implementing quaternary logic functions. This novel approach provides a methodology for processing two binary bits simultaneously. Furthermore, the SWSFET-based building blocks may be easily integrated with current CMOS technology. In particular, the conversion circuits presented in the paper may be used for this purpose. Finally, simulations are presented for basic SWS quaternary gates with BSIM equivalent models using Cadence Spectre simulator. Though manufacturing of multi-channel SWSFETs have challenges, they have the potential to significantly reduce the device count in the implementation of logic and cache in digital processors. This would help reduce the die cost and extend Moore's law.

ACKNOWLEDGEMENTS

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