A XOR THRESHOLD LOGIC IMPLEMENTATION THROUGH RESONANT TUNNELING DIODE

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ABSTRACT

Resonant tunneling diodes (RTDs) have functional versatility and high speed switching capability. The integration of resonant tunneling diodes and MOS transistor makes threshold gates and logics. The design and fabrication of linear threshold gates will be presented based on a monostable bistable transition logic element. Each of its input terminals consist out of a resonant tunnelling diode merged with a transistor device. The circuit models of RTD and MOSFET are simulated in HSPICE. Two input XOR gate is designed and tested.

Keywords

MOSFET, RTD, SPICE, Threshold, TLG

1. INTRODUCTION

Energy quantization due to columbic repulsion of single charges and quantum confinement are their underlying physical phenomena to control the charge transport through this nanoscale structures. The use of quantum effects to reduce the logic depth of a circuit and a flexible and intuitive methodology to transfer give logic functionality into a circuit design [1]. The continuous scaling of CMOS has encouraged research into alternative structures for future logic devices. These devices are capable of high speed operation with reduced power consumption. RTDs operate on the principle of quantum mechanics. The tunneling of electrons through a potential barrier into quantized well states, and the result is resonances in the transmission characteristics. The RTD characteristic depends on quantum mechanics nature of the tunneling process [2].

The Resonant tunneling diode (RTD), have features of its low voltage operation, THz capabilities and negative differential resistance [2][3]. The Terahertz range is the RTD maximum operating frequency and offers a wide range of applications, in analog-digital converter (ADC), frequency divider or multiplier, oscillator [4]) as well as digital ("multi-value" logic [5] [6]) circuits. Its I-V characteristic presents an unusual negative differential resistance (NDR)[7]. Resonant Tunneling Diodes (RTDs) present very attractive characteristics, such as a high intrinsic cut-off frequency (theoretical value in the THz range) and current peaks associated with Negative Differential Resistance (NDR) regions.

1.1 THRESHOLD LOGIC

Threshold Logic (TL), as a powerful alternative to Boolean Logic (BL), was proposed in the late 1950's as a result of the development of neural network theory, and was proven in theory to be

more efficient than Boolean Logic [8]. Recently, TL gates have been proposed in CMOS technology, e.g., Capacitive Threshold Logic [9], Differential Current-Switch Threshold Logic [10], and emerging nano-technologies, e.g., Single Electron Tunneling (SET) [11], Resonant Tunneling Diodes (RTD) [12], etc. While important steps have been made towards the hardware implementation of TL computing units the TL utilization in Very Large Scale Integration (VLSI) also requires the existence of high-level TL synthesis tools. The research has been done is very little on Threshold logic [13]. Recently, a synthesis tool has been proposed in [14], but it mostly treats Threshold Logic Gates (TLG) as conventional BL gates and the particularities of TL gates are almost completely ignored during the synthesis process.

1.1.1 LINEAR THRESHOLD GATES

The basic function of a linear threshold gate (LTG) is to differentiate between labelled points (vectors) belonging to two different classes [15] [16] [17]. An LTG maps a vector of input data, x, into a single binary output Y. The transfer function of an LTG is given analytically by the Input Output relation of threshold element is defined as

$$V_0 = X_n W_n \pm - - - - \mp X_2 W_2 + X_1 W_1 + W_0$$

$$V_0 = X_n W_n \pm - - - - \mp X_2 W_2 + X_1 W_1 - T \qquad \text{.....(1)}$$

$$V_0 = \sum_{i=1}^{n} W_i X_i - T \Rightarrow \text{Weighted Sum of elements-Threshold}$$

Where

$V_0 = \sum_{i=1}^{n} W_i X_i$ is weighted sum

$Y = f(V_0)$ where f is function of Heaviside

Y=1 if V_0>0 or $\sum_{i=1}^{n} W_i X_i$ >T

Y=0 if V_0<0 or $\sum_{i=1}^{n} W_i X_i$ <T

Where

$X_i=[X_1\ X_2\text{-----}X_n]$

$W_i=[W_1\ W_2\text{ -----}W_n]$ are the inputs and weights respectively and

T is threshold constant.

The symbolic representation of an LTG with *n* inputs is shown in Figure 1. A graphical representation of Equation 1 is shown in Figure 2.

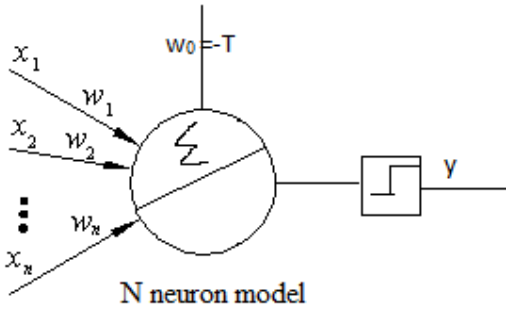

Figure 1 Symbolic representation of a linear threshold gate

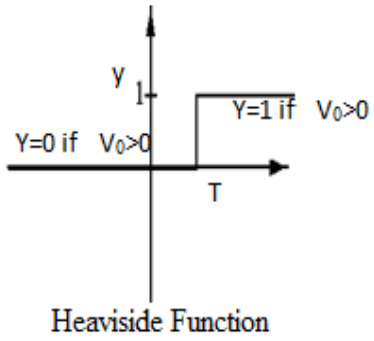

Figure 2 Transfer function.

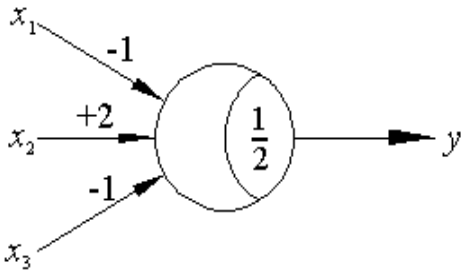

Figure 3 LTG realization of the Boolean function $y(x_1,x_2,x_3) = \overline{x_1}x_2 + x_2\overline{x_3}$

Exclusive-OR (XOR) $function(x_1,x_2) = \overline{x_1}x_2 + x_1\overline{x_2}$, cannot be realized using a single LTG and is termed a threshold function Shown in Figure 3.

1.1.2 GENERALIZED THRESHOLD GATES

After MTTG (Multiple Threshold Threshold Logic Gate), GTG is invented which reduce the complexity. GTG is Generalized Threshold Logic whose input implement according to positive and negative weight of threshold logic. We expect that the resulting Boolean function which is now only partially specified becomes a threshold function and hence realizable using a single

LTG. The realization of a Boolean function by the above process leads to a generalized threshold gate (GTG). The general transfer characteristics for an *n*-input GTG are given by

$$Y = 1 \; if \; \sum_{i=1}^{n} W_i X_i \; + \sum_{i=0}^{n} \sum_{j=0}^{m} X_i Y_j W_{ij} \; > \; T \; and \; otherwise \; Y = 0$$

1.2 RESONANT TUNNELING DIODE

Tunneling diodes (TDs) have been used in widely applications like in achieving very high speed in wide-band devices and circuits that are beyond conventional transistor technology. The Resonant Tunneling Diode (RTD) is a particularly useful form of a tunneling diode, is the RTDs have been shown to achieve a maximum frequency of up to 2.2 THz as opposed to 215 GHz in conventional Complementary Metal Oxide Semiconductor (CMOS) transistors [18]. The very high switching speeds have allowed for a range of applications in wide-band secure communications systems and high-resolution radar and imaging systems for low visibility environments[19]

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RTDs utilize a quantum well and with identically doped contacts to provide similar I-V characteristics. It consists of two heavily doped, narrow energy-gap materials encompassing an emitter region and a collector region. A quantum well in between two barriers of large band gap material, as shown in Figure 4 and the Energy Band Diagram of RTD shown in Figure 5. A Metal Organic Chemical Vapor Deposition using GaAs-AlGaAs is method of growth for this device. The barrier layers are around 1.5 to 5 nm thick and the quantum-well thickness is typically around 5nm [20].

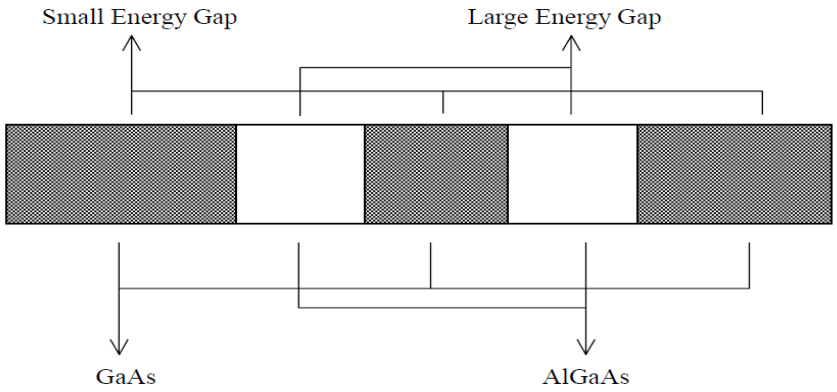

Figure 4. Structure of RTD (GaAs have small band gap and AlGaAs have large band gap).

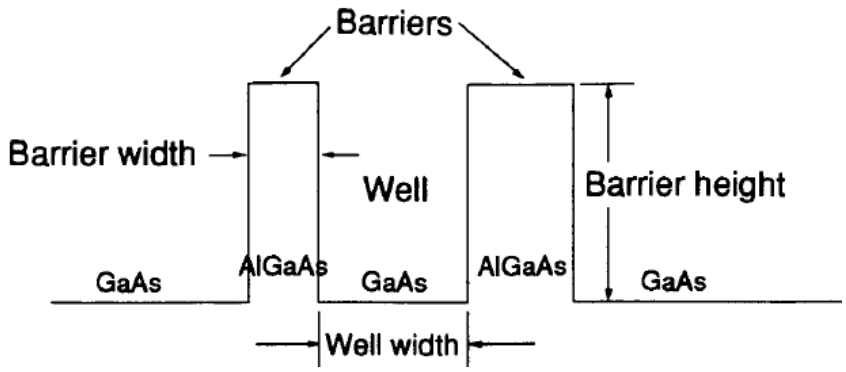

Figure 5. Energy Band Diagram of RTD

According to the graph on the emitter side, the current is at a maximum at the quasi-bound energy state indicated by the gray area in the quantum well shown in figure 4 and 5. RTD V-I characteristic shown in Figure 6.

1.3 PREVIOUS WORK

In threshold logic synthesis research was done mostly up to in the 1960s. In the determination of the input weights and threshold of a threshold function the approximation methods are used [21], [22]. Whether a function is threshold or not that is determine through admissible patterns on a Karnaugh map[23]. These methods are restricted to 10 or fewer variables due to computational complexity. Another methods like, the Linear programming and tabulation methods also have been used in [24] to determine if a function is threshold or not. The implementation of threshold gates using CMOS can be found in [25].

VLSI implementations survey report of threshold logic can be found in [26]. In [27], a branch-and-bound algorithm is used to synthesize two-level threshold networks. Multi-level threshold network synthesis did not receive much attention in the 1950s and 1960s because efficient algorithms to factorize a multi-level network were unknown at that time. The one-to-one mapping is used by mostly methods, by replacing each Boolean gate in the network with a threshold gate. However, various algorithms exist today to compute the kernels and co-kernels of a network, they also used to perform algebraic or Boolean factorization [28].

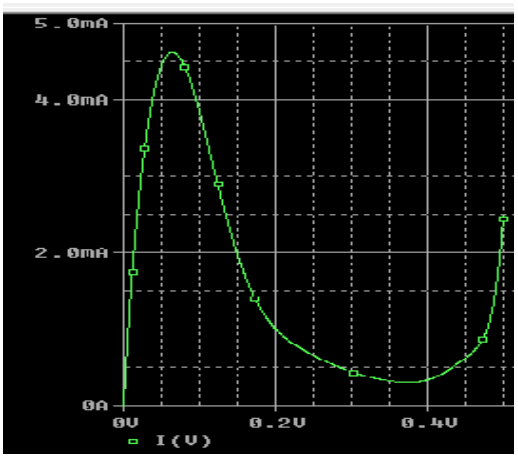

Figure 6. RTD V-I characteristic.

2. DESIGN AND IMPLEMENTATION

2.1 METHODOLOGY

In this section, we present our test generation framework for threshold logic gate. The input is a Boolean Inputs and the output is a test set which the operation of XOR logic. The Boolean input is synthesized into a threshold logic gate where TLG contains weights corresponding to input. We then perform threshold logic using RTD simulation using HSpice.

RTD works on concept of MOBILE where MOBILE is monostable bistable logic element. MOBILE is series connection of two RTDs which contain load RTD and driver RTD. Whenever MOBILE have load RTD than positive weighted inputs are connect to parallel with load RTD and negative weighted inputs are connect parallel with driver RTD, the driver RTD and load RTD is works according to bias voltage (Vbias) and gives output as Vout. Equivalent circuit of XOR make using RTD and threshold logic and simulate it using HSpice. The RTD areas should be adjusted to appropriate values for correct operation, moreover, the transistors width may be tuned for better performance in the MOBILE-based circuits.

The New structure of XOR gate are designed. The new design input, and output values and margins, maximum operating frequency, delay of each transition, static and dynamic power dissipations of the new structure are calculated. The performance of new designed XOR gate is compared with other XOR gates. The results confirm that has a high performance of New designed structure. Designing new XORs is of much attention because they are the main part of an ALU and other digital devices.

The design of XOR gates of different structures were presented in literature over the years. Most of XOR gate circuits are based on FET transistors and also some XOR gates based on other logics. At some point, the voltage drop across the RTD will increase such that it is operating in the NDR region (i.e., the dynamic resistance will increase), and the input current will drop sharply, turning off the transistor, thus switching At some point, the voltage drop across the RTD will increase such that it is operating in the NDR region (i.e., the dynamic resistance will increase), and the input current will drop sharply, turning off the transistor, thus switching V_{out} back to V_{bias}. Whenever we apply the bias voltage, current is increases at certain point, after that current is decreases at certain point and then current is increases, so that have two stable point and minimize the power dissipation than CMOS.

2.2 XOR FUNCTION REPRESENTATION

Here different implementation of XOR gate using the Threshold Logic and RTD/MOSFET. There is two threshold value so that XOR using MTTG is worked between

$$T_1 \prec \sum_{i=1}^{n} X_i W_i \prec T_2$$

Here $W_1 = W_2 = 1$, $T_1 = 1$, $T_2 = 2$ for XOR function.

Generalized Threshold Logic gate 1(GTG1), that is realized extended set of input variable as $(x_1, x_2, x_1 \& x_2)$, $W_1 = W_2 = 1$, $W_3 = -2$, $T = 1$.

The XOR gate designed by the authors is illustrated in figure 7(a). It is an adaption of the MOBILE configuration with the use of both positive and negative weighted input sections. The XOR function is realized by placing a series connected MOSFET pair in parallel with the driver RTD. Using this configuration both inputs must be high to direct current away from the summing node ensuring that the circuit output is logic low when both inputs are high. In the XOR gate depletion type MOSFETs (0.25μm gate length) are used above the summing node with

enhancement mode devices (0.25µm gate length) used in the series connected pair below the summing node. W:L ratios for all devices in both circuits are given in figure 4.

RTD areas given in figure 5 for both circuits are given in 2 µm and the peak current density of the devices is 21kA/cm2. Performance data for both circuits is given in table 1. The threshold logic gate shown in Figure 7 (b) uses both positive and negative weighted inputs.

The gate is designed to output a logic high when X1 is high and X2 is low ($X1.X2'$), and output logic low for all other input combinations. As with the XOR gate depletion mode MOSFETs (0.25µm gate length) are used in the positive weighted section with enhancement mode MOSFETs (0.25µm gate length) in the negative section.

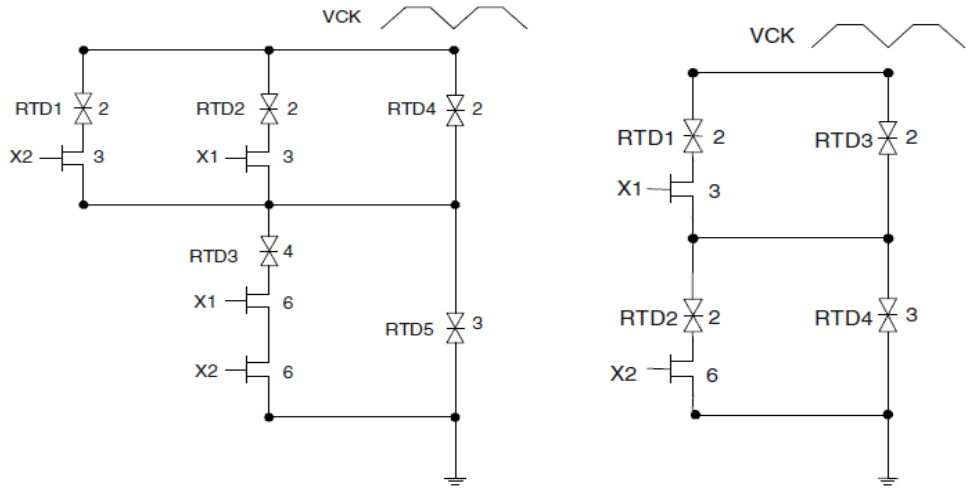

Figure 7. (a) Threshold logic XOR gate (b) Threshold logic gate for function $X1.X2'$

3. RESULT

The clock signal and V_{bias} is applied to the circuits and depict different sets of two inputs that are applied to the XOR gate and the HSPICE simulation results for these gates are depicted in Figure 8 and Figure 9.

Performance data for both circuits is given in table 1. The gate is designed to output a logic low when X1 and X2 is high ($X1.X2$), and output logic high for all other input combinations. As with the XOR gate depletion mode MOSFETs (0.25µm gate length) are used in the positive weighted section with enhancement mode MOSFETs (0.25µm gate length) in the negative section.

Our proposed circuits are the first MOBILE based designs that implement two-input XOR circuits in a single structure, i.e. a single gate in transistor level. Implementing XOR function in single structure (single block) enables designers to design more efficient full adders in comparison with the previous full adders that are based on cascading of two two-input XOR gates [29][30][31] to achieve a three-input XOR gate.

Table 1. Performance Data For the XOR gate and the f= X1.X2'gate.

Circuit	Clock	Logic High	Logic Low	Rise Time	Delay	Average	Max Power
AND	0.75 V	0.701V	0.074V	150pS	90pS	167µW	559 µW
Buffer	0.75 V	0.707V	0.0711V	160pS	90pS	95µW	338 µW
XOR	0.75 V	0.707V	0.101V	160pS	90pS	114µW	665 µW
X1.X2`	0.75 V	0.707V	0.071V	150pS	90pS	103µW	343 µW

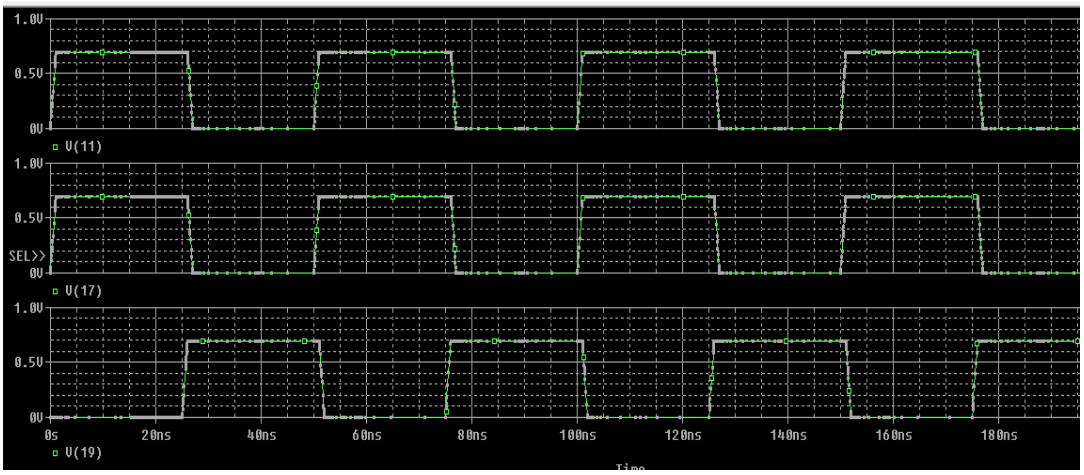

Figure 8. Voltage –Time Response of $X_1\overline{X_2}$ function (v(17),v(19) are input & v(11) is output)

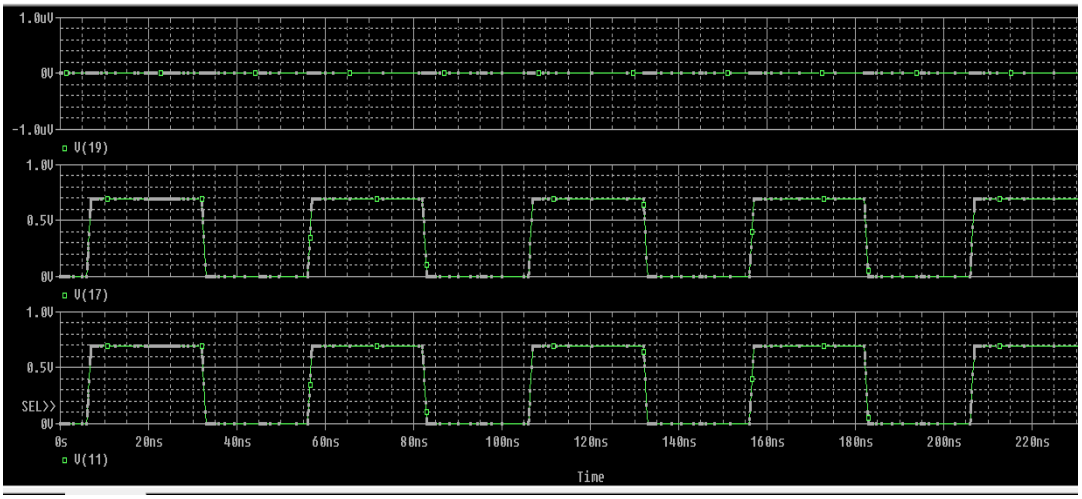

Figure 9.Voltage –Time Response of XOR function (v(17),v(19) are input & v(11) is output)

4. CONCLUSION

In this paper, to the best of authors' knowledge, a new two-input XOR gate circuit and a new two-input XOR gate circuit based on generalized threshold gate (GTG) are introduced for the first time. A simulation for all combination of inputs is done and the results are drawn. RTD designs can offer a reduction in component count by up to 40% when compared with the equivalent

CMOS logic family. Due to the threshold logic design style, which enables an increased low-level parallelism of computing multiple input signals, the advantage of the RTD circuits increases when equivalent circuit areas are compared. The main reason is that the threshold logic design eliminates the series connections of transistors in XOR-like gate configurations. Due to long series connections of p-MOSFETs in CMOS devices result in a large area consumption increases.

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