DESIGN LOW POWER ENCODER FOR THRESHOLD INVERTER QUANTIZATION BASED FLASH ADC CONVERTER

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ABSTRACT

Analog-to-Digital converters are the useful component in signal processing and communication system. In the digital signal processing low power and low voltage becomes a considerable component in that are challenging for designing high speed devices and converters. This paper describes the ultra high speed ADC design with a fat tree encoder that became highly suitable and accurate. Speed becomes the important part that enhanced by component of 2 guidelines of fat tree encoder. This paper also describes the implementation of TIQ based comparator that exhibits low power consumption as compared to other comparator based design. A 3 bit ADC has been designed and simulated in CMOS 45 nm technology with input voltage range of 0 V to 0.7 V. The simulated and analysed results shows low power and a high speed performance for optimised ADC.

KEYWORDS

Fat-Tree encoder, TIQ comparator, Average power, Delay.

1. INTRODUCTION

ADC standing for Analog-to-Digital converter. Analog Digital converter is a more useful component which helps to make up blocks in today's electronic system. ADC is a system which has a high speed operation it is designed as a faster component. ADC is the required $2^n - 1$ comparator for a n-bit A/D converter [1]. There are three types of technologies present in ADC converter: the CMOS technology, the bipolar technology, and the Gallium Arsenide (GaAs) technology. CMOS stands for Complementary-symmetry Metal-oxide semiconductor. The word "Complementary-symmetry" refers to the fact that the typical digital design make with CMOS uses complimentary and symmetrical pairs of P-type and N-type metal oxide semiconductor field affect transistors for logic functions. Typical CMOS technologies in manufacturing today add additional steps to implement the multiple device. CMOS technology is also used in Microprocessors, Microcontrollers, static RAM, and other digital circuits and it is also used for several Analog circuits such as image sensors (The CMOS sensor) data converters, and highly integrated transceivers for many types of communication. CMOS device provide a high comfortable immunity and low power consumption. With these important technologies ADC designed as a faster technology of inverter also used in ADC this unique technology is a called threshold inverter quantization (TIQ). TIQ technology makes ADC very faster and it provides

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high conversion speed. Along with these technologies ADC is faster and have a high speed flash [2]. CMOS logic circuit preferred for SOC and the fat tree TC-to-BC encoder provides a suitable and high speed to ADCs. Currently we can see that the main advantage of Fat tree encoder is that it provides high encoding speed than the other encoder. It also consumes less power consumption is a comparison of other encoder. For a high-speed application, resolution and power consumption these components are three key parameters. It acts a main role for an analog-to-digital converter (ADC). These parameters cannot be changed once a ADC. When ADC can operate at speed higher and will consume less power, it can operate easily. In designing the high speed ADCs, the code converter plays an important role in speed of and order of GSPS. ROM encoder [3-4] and fat tree encoders [5] are usually employed as code converters but these converters convert thermometer code into the 1-out-of-n code and at last it converts into binary code. Due to two step conversion process these converters introduce a large propagation delay of the order of ns [6]. The main feature of this concept of comparator technique is TIQ. Which is a high technique along with 6-bit and 8-bit flash ADCs were designed. This is a powerful technology of CMOS technology, but it requires a less means 0.7V power supply voltage [7]. The usual implementation of encoder has been read-only memory (ROM), programmable logic array (PLA) circuits, and ROM are implementation to tree encoder easily [8]. There are many following features of modern electronic system. 1) Should provide the high speed operation, 2) Should require less power consumption, 3) Should convert TC into 1-out of n-code then into binary code easily, 4) Read-only memory (ROM) and TIQ technology make it great feature, 5) There are different type of solid state technologies available for high speed in ADC converter. ADC is designed as essential as possible for high speed work we can define it as digital converter so digitalisation is also available in this technology.

2. THEORY OF ADC

In modern time there are many different types of ADCs available, which depend on the types of applications. ADC's are mostly defined include three main categories. It divided into three categories depending on their high speed of operation. The three types of ADCs are a low speed /serial ADC, medium speed ADC and high speed ADC. That means these ADCs have each high operating speed. The serial ADC has a very high resolution they support the high speed operation that means very high frequencies but these ADCs have a relatively low resolution. There are different types of ADC's, 1) Flash ADC, 2) Sigma delta ADC, 3) Ramp counter ADC and 4) Successive approximation ADC. Flash ADC is the fastest ADC it works faster just because of its parallel diagram. Flash ADC design has been widely defined, this type of ADC is a part of ADCs which have different diagrams, resolutions, sampling rates, power consumptions, and a range operating temperature. These are important features available in a flash ADC. Because of parallel design of flash ADC, it converts one cycle easily with many comparators. This flash ADC converts analog to digital are so fast as for analog signal and to a digital signal conversion. A most features flash ADC it has a power of consumption and large chip area by which flash ADC converters easily to signal and it practicable limits at higher resolution. The flash ADC is designed to save power consumption easily that means it provides proper output of signal but require a less amount of power. Now a day's CMOS flash ADC is also available. A Flash ADC using a CMOS inverter based comparator. It also has the threshold Inverter technique (TIQ) for high operating speed and low power consumption CMOS technology [9]. Signal processing in digital domain provides us with high level of accuracy and low power consumption it works fast possible. Some ADC's bandwidths are smaller than the Nyquist bandwidth [19-20].

2.1. Related Work

This section says about the related work did in designing low power TIQ based Flash ADC. Design and implementation of an ultrafast 3-bit 45nm CMOS Flash ADC based on TIQ comparator is presented. This paper [2] presents an ultrafast CMOS Flash A/D converter design and performance. To achieve high speed in CMOS, the featured A/D converter utilises the threshold inverter quantization (TIQ) technique.

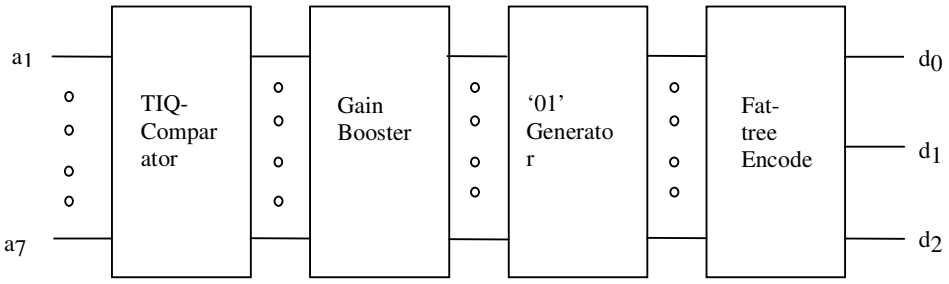

Fig1-: Block diagram of 3-bit ADC

2.2.TIQ Comparator

Comparator is used as a design component of ADC. This works here as 2^n-1 differential amplifiers. This improves gain or power savings. Comparator would have the advantage to our ADC but some disadvantage also. When the input signal voltage is less than the reference voltage, than the comparator output is at logic '0', when the input signal is higher than the reference voltage, the comparator output is at logic '1'. Comparator gives 2^n-1 levels of output for reference voltage. The Flash ADC performance of depends on comparator input signal without jitter [21].Therefore this comparator consisting of differential amplifiers.

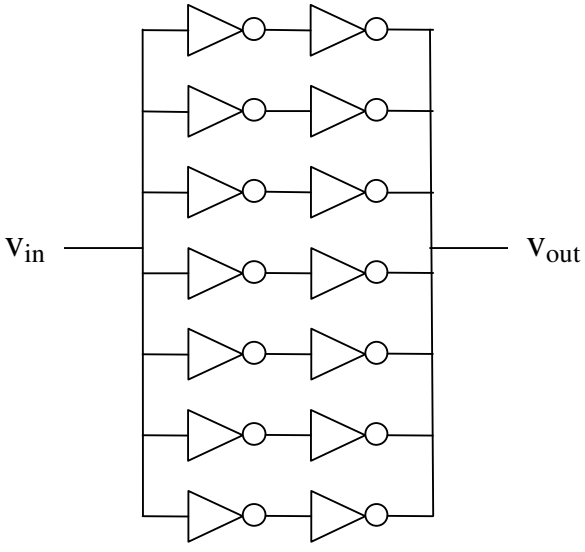

Fig2: TIQ Comparator

$$V_t = \frac{r(V_{dd} - |V_{tp}|) + V_{tn}}{1 + r}$$

Where :V_t =Threshold voltage of TIQ comparator,V_{dd} = supply voltage of ADC,V_{tp} and V_{tn} are threshold voltage of PMOS and NMOS devices,

$$r = \sqrt{\frac{K_p}{K_n}}$$

2.3. Fat-tree Encoder

By help of these equations we have design Fat-tree encoder.

$$d_0 = (a_1 + a_3) + (a_5 + a_7)$$
$$d_1 = (a_2 + a_3) + (a_6 + a_7)$$
$$d_2 = (a_4 + a_5) + (a_6 + a_7)$$

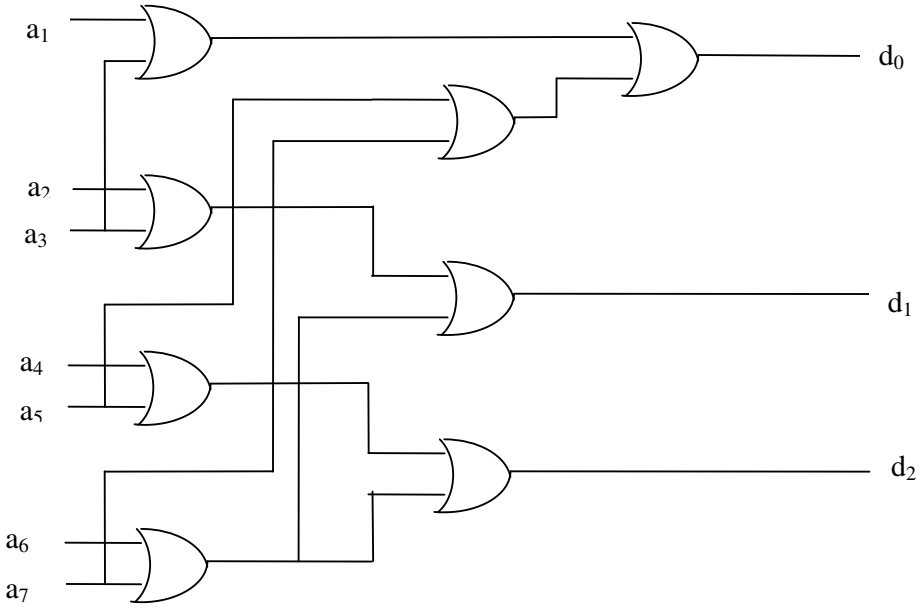

Fig 3:- Schematic of Fat-tree encoder

A fat-tree encoder has been designed to convert the encoded signal into n bit data this data is digital which is in binary code [11][12]. The output of converters is given in the encoded form but it is functioning of fat tree encoder that it converts the giving encoded signal into digital data. With this function the TC-to-BC encoding is carried out into two stages in the fat tree encoder. Fat tree encoder converts the data in many stages: the firsts on stage convert into the thermometer code to one-out-of-N code then encodes is the same address's decoder output. This code converts N bit parallel. The second stage converts the one-out-of-N code to binary code using the multiple trees or fat tree circuit signal delay is O(log2 N)after it ROM circuit signal delay is O(N)[13]. In this way the signal encoding delay is O(log1:5 N). A fat tree encoder performs better as has signal delay of "0" this is the speed is improved by a factor of 2 when we

use a fat tree encoder. The fat tree encoder is a very good solution for the little problem in high speed ADCs.

3. LEAKAGE POWER

Static CMOS gates are very power efficient because they dissipate nearly zero power when idle. Earlier, the power consumption of CMOS devices was not the major concern whiles designing chips. Factors like speed and area dominated the design parameters. As the CMOS, technology moved below sub-micron levels the power consumption per unit area of the chip has raised tremendously. Leakage power is a significant portion of the total power consumed by such designs. The leakage power dissipated by a circuit in the standby mode is dependent on the input vector to the circuit [14,15,16,17]. The total number of input vectors for a circuit with N inputs is 2N. Fig4 shows the transient response of Fat-tree encoder at 0.7v

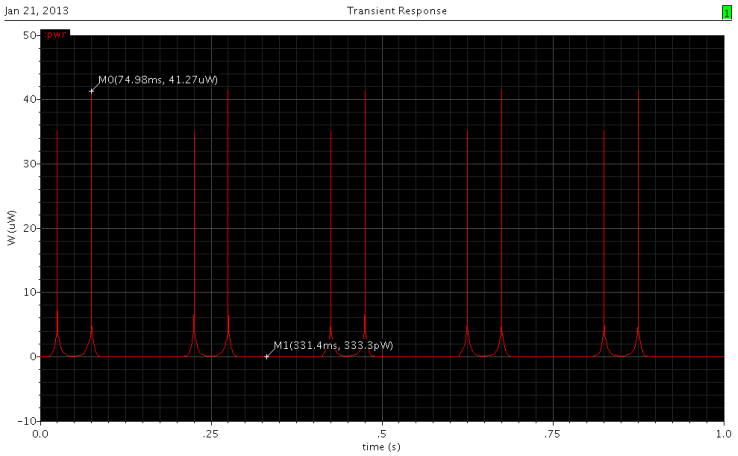

Fig 4:- Leakage power of Fat-tree encoder

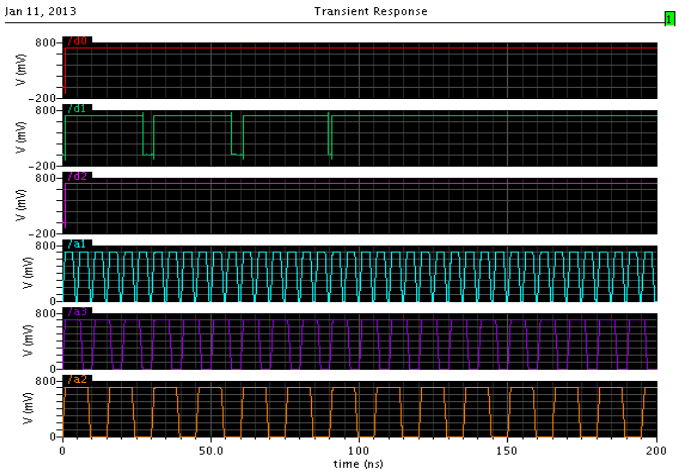

Fig5:- Output of Fat-tree encoder

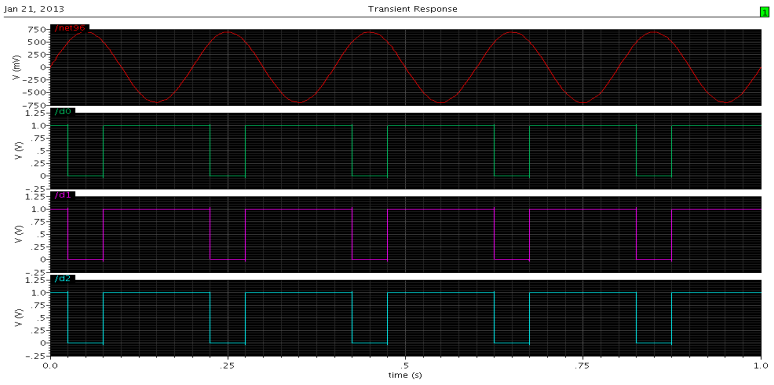

Fig6:- Output of 3-bit ADC using TIQ

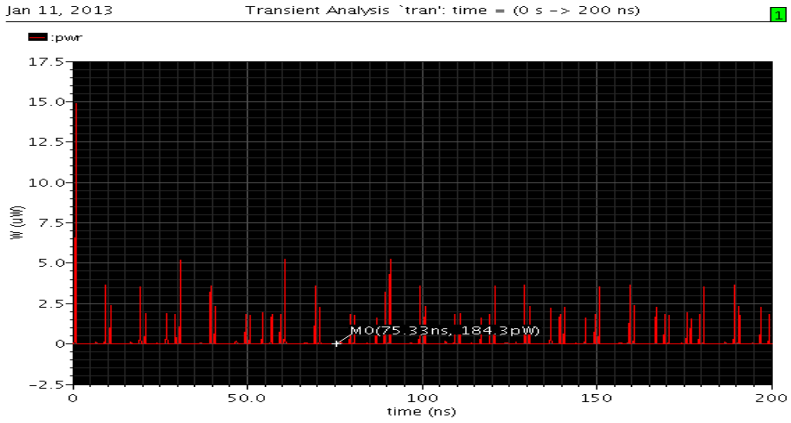

Fig 7:- Leakage of power 3-bit ADC

Fig.7 shows the transient response of 3-bit ADC in frequency 5Hz at 0.7v and Average power consumes in 185nw.

3. SIMULATION RESULTS

Voltage (V)	Performance Parameter							
	Delay	Average Power	Average Leakage Power (5Hz)	Average Leakage Power (2Hz)	SNHR	ENOB	SFDR	Bandwidth
0.7	6.5ps	4.34nw	4.344nw	45.52nw	8.512db	-1.03bit	1.57db	16.65mHz
1.0	8.296 ps	185.6nw	416.8nw	402.6nw	11.57db	-443.5bit	2.79db	25.02mHz
1.5	8.9ps	187.2nw	17.40uw	17.33uw	11.83db	-421.3bit	2.91db	25.52mHz
2.5	9.2ps	189.0nw	35.80uw	36.0uw	12.5db	-401.1bit	3.14db	28.03mHz

4. CONCLUSION

Flash ADC employs parallel voltage comparison that becomes the main factor for larger power consumption as an increase resolution of ADC therefore TIQ based ADC used here for lower power consumption converter design. Thermometer based encoder design becomes overhead in flash ADC design a so fat tree encoder is used for resolve the overhead problem of ADC. Leakage power is achieved to 4.344 nW at 5 Hz frequency however signal to noise ratio (SNR) 56.3db is reported as compared with other encoder based design. A Speed of 15.3 Gs/s is observed for 3 bit ADC that has been simulated by cadence tool at 45 nm technology. This paper evaluates a fat tree encoder performance and show it has been a better performance as compared with other encoder in design of ADC. TIQ based ADC provides the lower bandwidth of 16.65 MHz and low SFDR 1.57dB therefore a performance of ADC enhance.

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