PERFORMANCE ANALYSIS OF MODIFIED QSERL CIRCUIT

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ABSTRACT

This work is based on a new approach for minimizing energy consumption in quasi static energy recovery logic (QSERL) circuit which involves optimization by removing the non adiabatic losses completely. Energy recovering circuitry based on adiabatic principles is a promising technique leading towards low-power high performance circuit design. The efficiency of such circuits may be increased by reducing the adiabatic and non-adiabatic losses drawn by them during the charging and recovery operations. In this paper, performance of the proposed logic style is analyzed and compared with CMOS in their representative inverters, gates, flip flops and adder circuits. All the circuits were simulated by VIRTUOSO SPECTRE simulator of Cadence in 0.18μm technology. In our proposed inverter the energy efficiency has been improved to almost 30% & 20% upto 20MHz and 20fF external load capacitance in comparison to CMOS & QSERL circuits respectively. Our proposed circuit provides energy efficient performance up to 100 MHz and thus it has proven to be used in high-performance VLSI circuitry.

KEYWORDS

Adiabatic logic circuits, Energy, Diode, Power clock.

1. INTRODUCTION

With the growing requirement of portable communication many research have been done to reduce energy dissipation [1]-[4], among them adiabatic logic technique [5] is very promising. In adiabatic circuits energy dissipation occurs due to adiabatic and non adiabatic losses. If we lower the rate of charging, then lesser amount of power is drawn from the source and lesser will be adiabatic losses. Non adiabatic losses occur due to the voltage drop of terminals of a transistor (as a switch)/diode when it is on. Most of the adiabatic circuits have these non adiabatic losses due to the voltage drop across the diodes or incomplete energy recovery. The basic idea for reducing adiabatic losses is that; clock transient time T is kept much larger than intrinsic time constant RC_L of the device [6]. Non adiabatic losses are minimized by recovering the energy stored in load capacitances [7]. The energy in charging the load capacitances is recovered during discharging and stored for reuse. In adiabatic logic circuits time varying voltage supply is used so that the nodal capacitance are charged or discharged at a constant current which makes voltage drop

DOI : 10.5121/vlsic.2013.4403

almost negligible, whereas in CMOS logic circuits we use constant DC voltage source. The word 'adiabatic' is used in a reversible thermodynamic process [8] where a transformation is done so that no gain or loss of heat or energy occurs. By making the transformation process very slow the heat or energy loss can be made almost zero ideally.

In recent years many adiabatic logic structures have been proposed which work on the same theory but have different circuit structures and complexity. The quasi-static energy recovery logic (QSERL) circuit [9] attempts to reduce the drawbacks of the previous energy recovery logic (ERL) families due to its static logic resemblance circuit structure, reduced switching activity and number of power clocks but it have drawback of in-robustness and output floating due to the alternate hold phases. Complementary energy path adiabatic logic (CEPAL) provides improvement to the QSERL circuit because it does not need feedback keeper to remove floating output which in turn improves area and power overhead [10]. Also its throughput is better (twice) than QSERL. But due to the extra MOSFET diodes in charging and discharging path a bit larger power dissipation than QSERL circuits occurs.

Due to these challenges with reported adiabatic logic circuits [11-19] we propose modified quasi static energy recovery logic (MQSERL) circuit. MQSERL inherits all the advantages of recently reported QSERL circuits with additional improvement in power saving by reducing the non adiabatic losses as well as adiabatic losses. We have designed and simulated various MQSERL based logic circuits and their performances have been evaluated and compared with some reported adiabatic circuits and conventional CMOS circuits.

This paper contains four sections. Section 1 deals the introduction part. Section 2 describes the proposed energy recovery logic (MQSERL) circuit and it's working. In section 3 we have simulation results and discussion. The section 4 summarizes the conclusion.

2. PROPOSED ENERGY RECOVERY LOGIC CIRCUIT

2.1. Circuit description

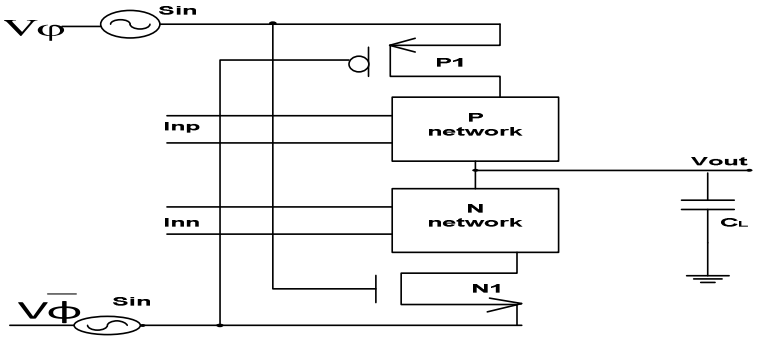
The circuit of modified quasi static energy recovery logic (MQSERL) is shown in Fig. 1(a). It is composed of with two complementary sinusoidal power clocks (V_Φ and $V_{\bar{\Phi}}$), a charging pMOS transistor (P1) whose gate is connected by the power clock $V_{\bar{\Phi}}$, and a P-network in charging path, and a discharging nMOS transistor (N1) whose gate is connected by the power clock V_Φ , and a N-network in discharging path. The power clock (V_Φ) is in phase whereas the other clock ($V_{\bar{\Phi}}$) is 180 degree out of phase. The sinusoidal clock charges/discharges the load capacitance comparatively slowly than the triangular or trapezoidal power clocks. We have discussed in previous section that we can enhance power efficiency of adiabatic logic circuits by ensuring that how slowly the nodal capacitances are charged or discharged thus power dissipation is minimized by using these sinusoidal clocks. The peak to peak voltage of power clocks V_Φ and $V_{\bar{\Phi}}$ is 1.8 V.

The transistor (P1) in the pull up network and transistors (N1) in the pull down network are used instead of the diode (which was used in QSERL circuit) for reducing the non adiabatic losses. Power clock (V_Φ) controls the ON and OFF time of transistor (N1) and ($V_{\bar{\Phi}}$) controls the ON and OFF time of transistors (P1). The noticeable source of power dissipation in QSERL circuits was due to the MOSFET diode's threshold voltage drop (which is non adiabatic loss) whereas in the proposed MQSERL circuit, the main source of power loss is due to the ON resistance of channels of MOSFET transistors P1 & N1 [12].

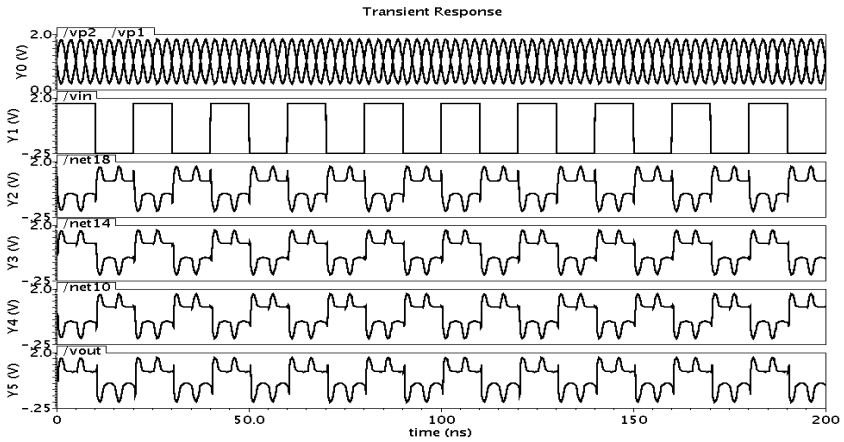
The losses due to the ON resistance of P1 & N1 are significantly lower than the losses due to the threshold voltage drop through diodes and overall losses can further be lowered by lowering the charging speed. Thus by using transistors (P1 & N1), power dissipation is much reduced in comparison to the diode based circuits. However we can not remove the power dissipation completely because of the non reversible nature of the proposed circuit.

2.2. Circuit operation

The operation of the circuit is divided into two stages based on the supply clock phases, evaluation and hold. In evaluation phase V_Φ gradually increases from low to high voltage while $V_{\bar{\Phi}}$ gradually decreases from high to low voltage, whereas in hold phase V_Φ gradually decreases from high to low and $V_{\bar{\Phi}}$ increases from low to high voltage as shown in Fig. 1(b).



(a)



(b)

Figure 1. Proposed MQSERL topology (a) circuit diagram, (b) simulation waveforms of 4 inverter chain

In evaluation phase, if output node (V_{out}) is at LOW logic and the P tree is turned ON, load capacitance (C_L) is charged through pMOS transistor (P1) producing HIGH logic at the output. Whereas if output node (V_{out}) is at HIGH logic and N tree turns ON, discharging and recycling to the power clock ($V_{\bar{\Phi}}$) via nMOS transistor (N1) occurs, producing LOW output logic. In hold phase, V_Φ decreases from high to low and $V_{\bar{\Phi}}$ increases from low to high and when they reaches below the threshold voltage of P1 & N1 both turns OFF thus no transitions shown at the output.

Dynamic switching is reduced because of the hold phase, which will again reduce the energy dissipation.

The simulated waveforms of proposed MQSERL 4 inverter chain in Fig 1(b) shows that the output signals of cascaded logics not affecting the performance in MQSERL inverter circuit.

3. SIMULATION RESULTS AND DISCUSSION

Adiabatic circuits cannot be designed by using conventional method [20] therefore the accurate design of proposed MQSERL gates will assist the better performance of the larger circuits [21, 22]. In the remaining paper several MQSERL based circuits have been presented.

We have simulated all the circuits with width to length ratio of the nMOS transistor as 240 nm/180 nm, pMOS as 540 nm /180nm respectively. The supply waveform is sinusoidal; and the supply frequency is 200 MHz. Input is a square voltage pulse with a frequency of 50 MHz. The peak supply voltage is fixed at 1.8 V, which is enough to drive the transistors with reasonable logic values.

3.1. Proposed energy recovery logic inverter

The inverter circuit (obtained by replacing P-network and N-network with pMOS and nMOS respectively in Fig. 1(a)) is simulated using VIRTUOSO SPECTRE simulator of cadence. The energy dissipation is calculated by subtracting the energy pumped back from the energy drawn.

3.1.1. Energy efficiency with frequency

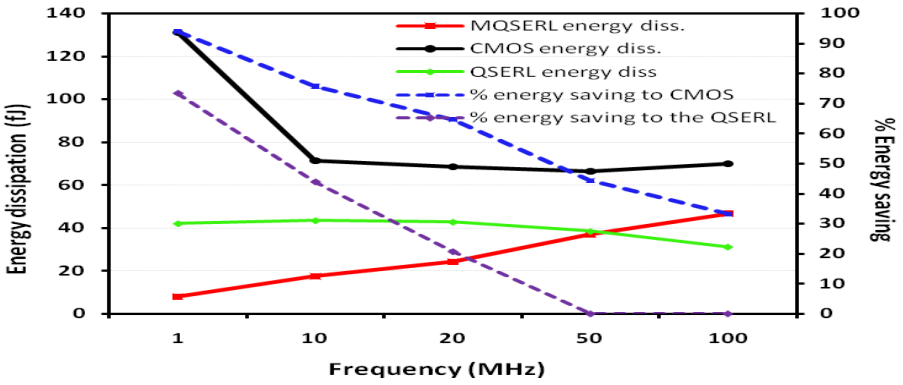


Figure 2. Simulation results of the performance comparison of inverters with frequency

To check the performance of proposed inverter with frequency, input and supply frequencies are varied simultaneously (keeping supply frequency four times the input frequency for better performance) from 1 MHz to 100 MHz and load capacitance is set to 20fF as shown in Fig. 2.

With the frequency, energy dissipation of QSERL & CMOS inverters decreases whereas proposed MQSERL inverter has lesser energy dissipation in comparison to these two inverters. After 50 MHz QSERL inverter fails to give correct output logics so it has lesser energy dissipation than proposed inverter after this frequency. The drawback is that a continuous decrease in percentage energy saving of proposed over other two inverters with frequency is observed.

3.1.2. Effect of variation of load capacitance

To check the performance with load capacitance variation we added extra capacitive load at the output node one by one from 10fF to 100fF as shown in Fig. 3. Clock & data rate kept fixed at 160 MHz & 40 MHz respectively.

When we increase the load capacitance, energy dissipation of all three inverters increases however the proposed inverter has good energy efficiency than CMOS at each point whereas QSERL output logic becomes incorrect after 10fF and thus have lower energy dissipation than proposed circuit.

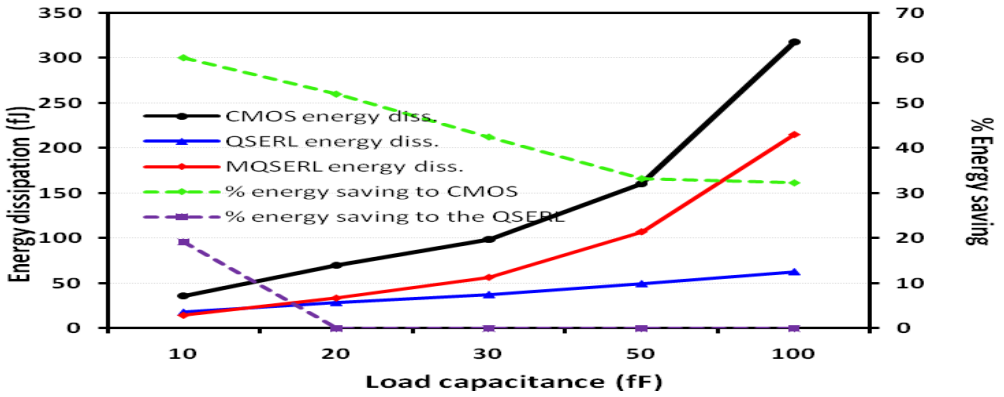
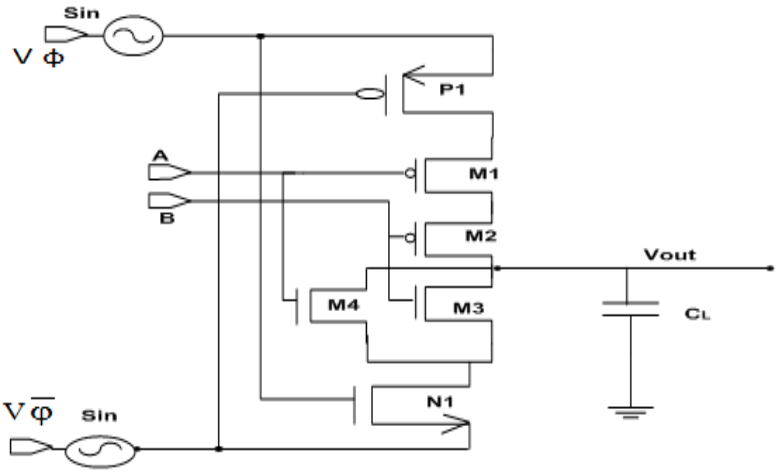
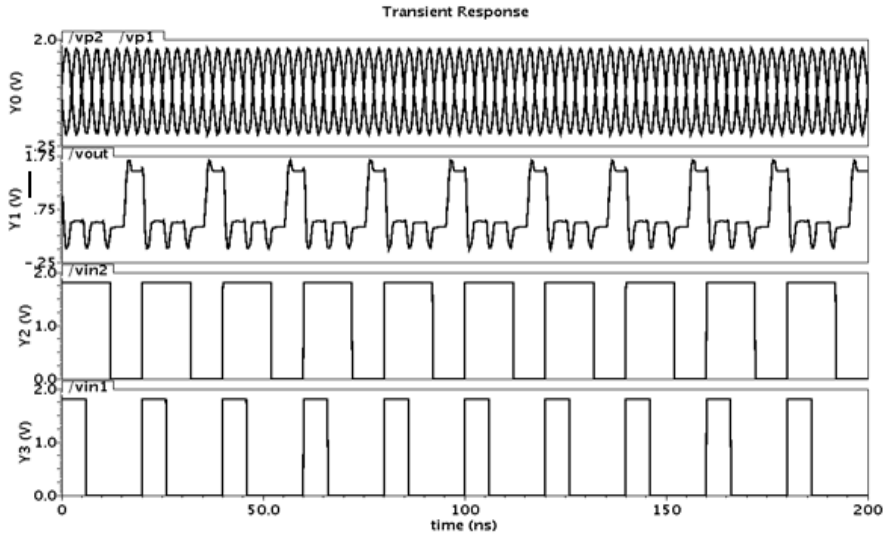


Figure 3. Simulation results of the performance comparison of inverters with load capacitance

3.2. Proposed energy recovery logic NOR Gate



(a)

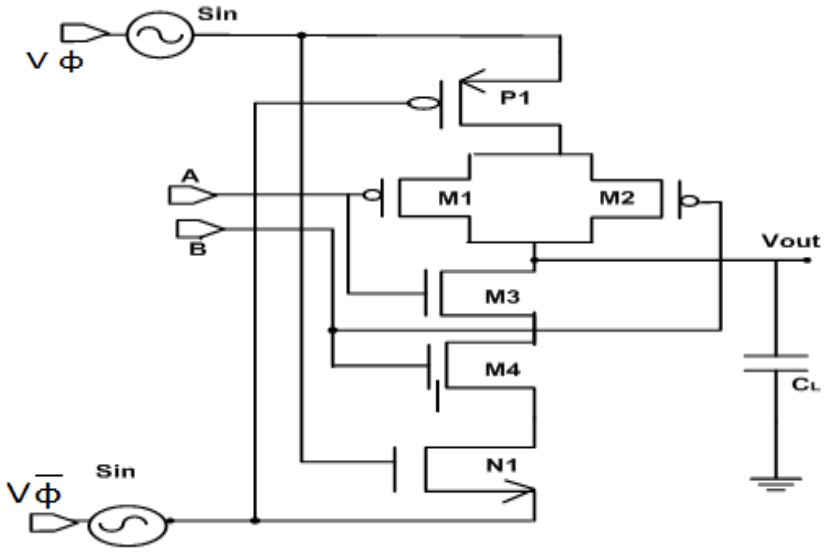


(b)

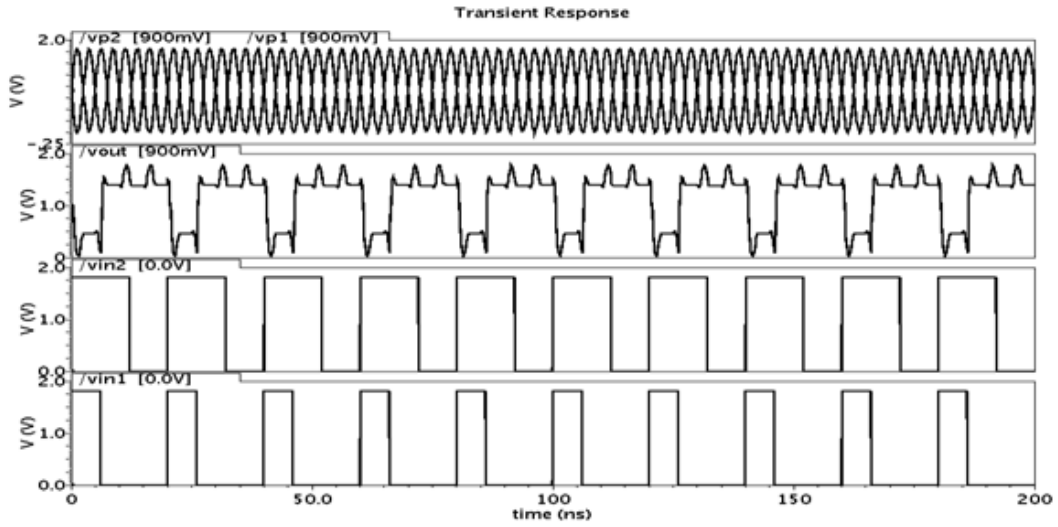
Figure 4. Proposed MQSERL NOR gate (a) circuit diagram, (b) simulation waveforms

The proposed MQSERL NOR gate is shown in Fig. 4(a). This circuit is made from two pMOS transistors (M1 and M2) and two nMOS transistors (M3 and M4). A charging pMOS transistor P1 & discharging nMOS transistor N1 is also present whose gate is tied with sinusoidal power clocks ($V_{\bar{\phi}}$ and V_{Φ} respectively). Input A is connected with the gates of M1 and M4 and gates of M2 and M3 are connected with another input B. The simulated timing waveforms having bottom two graph as input strings A= '10010010010010010010010010010100', B= '11011011011011011011011011011110'and the top two graphs as power clocks & output= '00100100100100100100100100100100' respectively are shown in Fig 4(b).

3.3. Proposed energy recovery logic NAND Gate



(a)



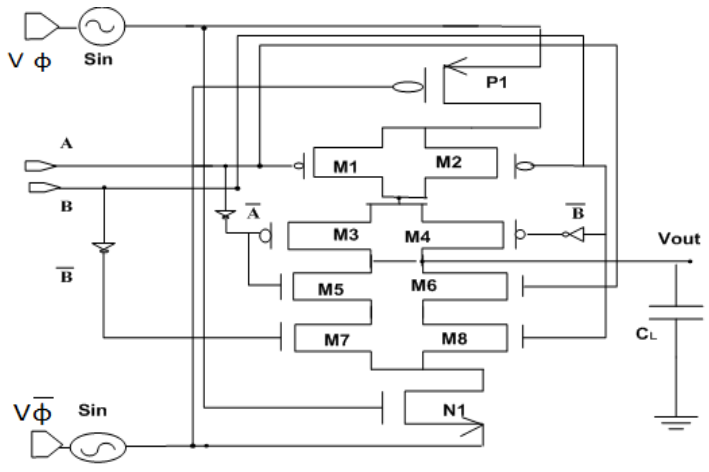
(b)

Figure 5. Proposed MQSERL NAND gate (a) circuit diagram, (b) simulation waveforms

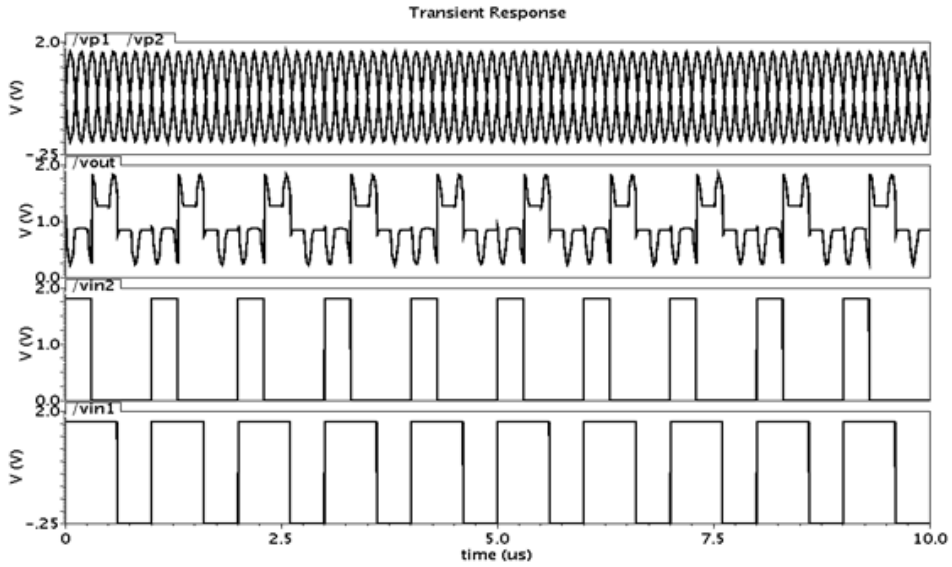
The proposed MQSERL NAND gate is shown in Fig. 5(a). The circuit is made from two pMOS transistors (M1 and M2) tied in parallel and two nMOS transistors (M3and M4) which are connected in series. Output load capacitance is charged/discharged through charging/discharging pMOS/nMOS transistors P1 & N1 whose gate is directly connected with sinusoidal power clock ($V_{\bar{\phi}}$ and V_{Φ} respectively). M1 and M3 gates are connected together with an input A and M2 and M4 gates are connected with another input B.

The simulated timing waveforms having bottom two graph as input strings A= '1001001001001001001001001001001001', B= '1101101101101101101101101101101101' and the top two graphs as power clocks & output= '0110110110110110110110110110110110' respectively are shown in Fig 5(b).

3.4. Proposed energy recovery logic XOR Gate



(a)



(b)

Figure 6. Proposed MQSERL XOR gate (a) circuit diagram, (b) simulation waveforms

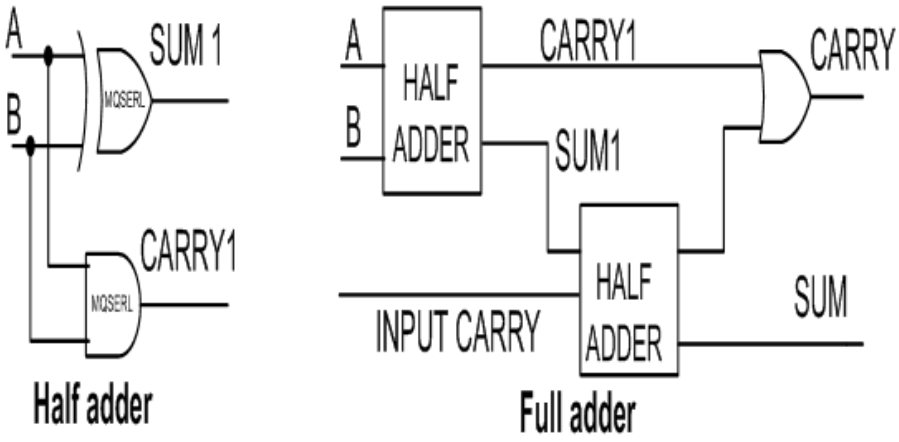
The proposed MQSERL XOR gate is shown in Fig. 6(a). Its' circuit is made from a P network with four pMOS transistors (M1, M2 tied in parallel and M3, M4 connected in parallel) and a N network with four nMOS transistors (M5 and M7 connected in parallel with M6 and M8). A charging pMOS transistor P1 and a discharging nMOS transistor N1 is also used which are controlled by sinusoidal power clocks ($V_{\overline{\phi}}$ and V_{Φ} respectively). M1 & M6 gates are connected with input A, and M3 & M5 with $\overline{A}$. However M2 & M8 gates are connected with input B and M4 & M7 with $\overline{B}$.

Simulated timing waveforms having bottom two graph as input strings A= '1101101101101101101101101101101101101', B= '1001001001001001001001001001001001001'and the top two graphs as power clocks and output= '0100100100100100100100100100100100100' respectively are shown in Fig 6(b).

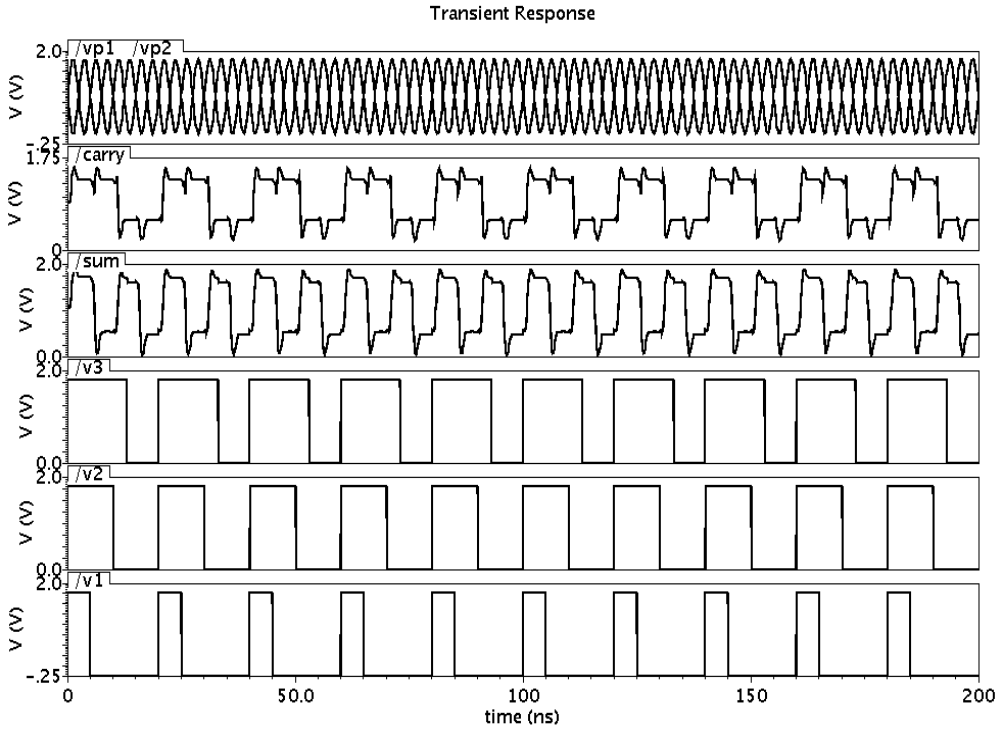
3.5. Proposed energy recovery logic 1 bit Full adder

The MQSERL full adder consists of two MQSERL half adders and an OR gate. The block level diagram of our MQSERL half adder is given in Fig. 7(a). It is made from a XOR gate and one AND gate.

Simulated timing waveforms having bottom three graphs as input strings A='1000100010001000100010001000100010001000',B='1100110011001100110011001100110011001100'and Cin= '1110111011101110111011101110111011101110' the top three graphs as power clocks & outputs, Carry= '1100110011001100110011001100110011001100' and Sum = '1010101010101010101010101010101010101010' respectively are shown in Fig 7(b).



(a)



(b)

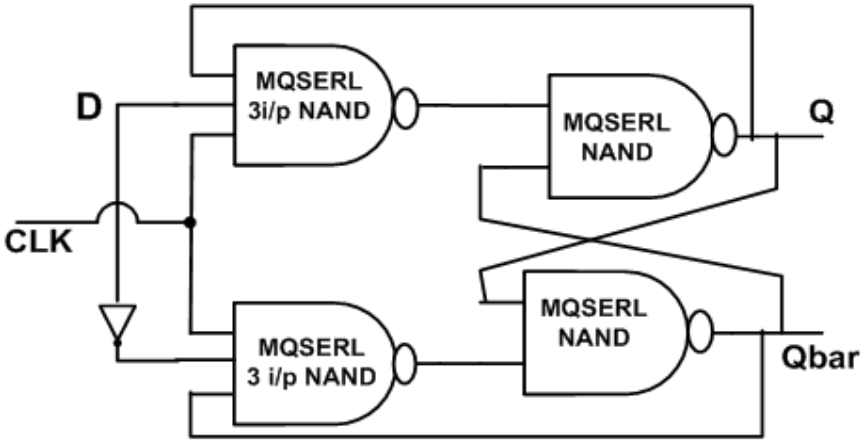
Figure 7. Proposed MQSERL Full adder (a) circuit diagram, (b) simulation waveforms

3.6. Proposed energy recovery logic D flip flop

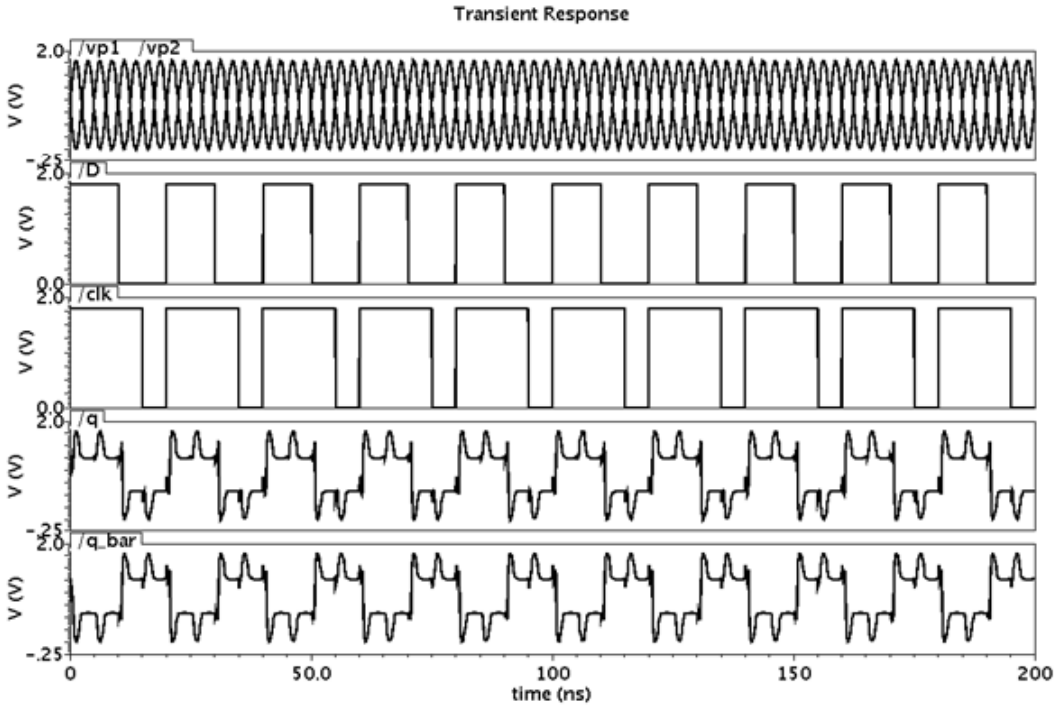
The proposed MQSERL D flip flop is shown in Fig. 8(a), it is made from two MQSERL 3 input NAND gates and two MQSERL 2 input NAND gates and a MQSERL inverter circuit.

Simulated timing waveforms from the top for power clocks, inputs D= '1001001001001001001001001001001' & CLK= '1101101101101101101101101101101' outputs

Q= '1001001001001001001001001001001' & Qbar= '0010010010010010010010010010010' respectively are shown in Fig. 8(b).



(a)



(b)

Figure 8. Proposed MQSERL D flip flop (a) circuit diagram, (b) simulation waveforms

The simulated timing waveforms of proposed MQSERL based all the circuits verifies the functionality of proposed logic style. These circuits are compared with CMOS circuits using equal switching probability of inputs whereas W/L ratio in proposed MQSERL circuits is same as given in the starting of this section i.e. for pMOS it is 540nm/180nm and for nMOS it is 240nm/180nm however in CMOS circuits it is same for pMOS and nMOS i.e. 240nm/180nm. It

is observed from the Table 1 that the proposed MQSERL circuits have almost 36% or greater energy saving to the conventional CMOS circuits except half adder (25.7% energy saving).

Table 1 Comparison of proposed MQSERL and CMOS circuits at (f_{Φ}, $f_{\overline{\Phi}}$) =200MHz, f_{in} =50MHz

Energy dissipation (fJ)/per cycle							
Circuits	4,inv chain	NAND	NOR	XOR	Half Adder	Full Adder	D flip flop
CMOS	28.8	11.26	7.34	31.6	48.2	159.4	100.4
Proposed	17.4	7.2	3.24	19.52	35.8	90.4	52
% Energy saving							
	39.58	36.05	55.85	38.23	25.7	43.8	48.2

4. CONCLUSIONS

In this paper we have presented modified quasi static energy recovery logic (MQSERL) family. Specifically we presented the performance analysis of MQSERL inverter to validate the operating capability and energy efficiency of proposed circuit with variation in frequency and load capacitance. The simulation results and comparative performance evaluation revealed that energy dissipation in the MQSERL logic are considerably lower than the CMOS and QSERL logic. The proposed MQSERL family outperforms and provides almost 36% of energy saving at 50MHz for almost all the MQSERL based logic circuits.

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