A NEW LOW VOLTAGE P-MOS BULK DRIVEN CURRENT MIRROR CIRCUIT

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ABSTRACT

This work proposes a new low voltage current mirror circuit using bulk driven technique. Bulk driven technique is used to reduce the threshold of PMOS used in low voltage current mirror circuits (LVCM). The proposed circuit consist of 4 PMOS and 5 NMOS. The proposed circuit operated at +0.85 V supply voltage. The bandwidth of this circuit has also been enhanced using resistive compensation technique. The proposed circuit has been simulated in Cadence Design Environment in UMC 180nm CMOS technology. A transfer characteristic of the proposed circuit has been discussed. The proposed circuit find application in low voltage and low power analog integrated circuits.

KEYWORDS

Low voltage, Current Mirror, Bulk driven.

1. INTRODUCTION

Advances in CMOS technology have made it feasible to design chips with high packaging density, better performance and lower power consumption. To attain these goals, the size of the CMOS devices has been scaled down to very small features and dimensions. However, the power supply voltage has not been scaled down proportionally to ultra-deep sub-micron technology. The limitation of low voltage circuit design using the existing technology is that the power supply must be at least equal to the sum of the magnitude of the threshold voltages of cascaded P-MOS and N-MOS transistors. There are several techniques, such as bulk-driven, sub-threshold, self cascode, and floating-gate has been evolved to construct high performance analog circuits under low power supply voltages. Figure 1 shows the symbols of current mirror circuits in which arrow is used to show the direction of the current flow on the input side. The ratio 1: K shows the current gain of the Current mirror circuit.

Figure 1 Current Mirror symbols (a) NMOS current mirror (b) PMOS current mirror.
The bulk-driven technique is used to scale down the threshold voltage of PMOS transistor used in circuit. The body terminal of PMOS is connected to input to provide weak positive bias so that threshold voltage of PMOS is reduced and supply voltage is effectively scale down. This technique is completely compatible with standard CMOS process.

Current mirror (CM) circuits are widely used in analog integrated circuit. It is clear from its name that it copies the current. Current mirror are circuits whose output current is independent of output terminal voltage and depends on input current only. They are used for current amplification, biasing, active loading and level shifting. Efficient design of current mirror circuit improves the overall performance of analog integrated circuit and reduces the supply voltage requirement of the circuit.

2. PREVIOUSLY REPORTED CURRENT MIRROR CIRCUITS

2.1 Very Low Input impedance Low Power Current Mirror

In order to get low input impedance, the main idea is to introduce transistor $M_3$ in series with the input terminal of the basic circuit of the current mirror and use a gain amplifier of ‘$-A$’ gain to control the gate voltage of $M_3$. In Figure 2 (a) a simple current mirror is shown and in Figure 2 (b) conceptual schematic of the current mirror. Any increase in source voltage of $M_3$ (i.e. due to injected input current) causes its gate voltage to decrease ‘$-A$’ times, hence causing stronger sink of input current which results in decrease of input impedance by ‘$A$’ times.

![Figure 2](image)

2.2 Self Cascode Current Mirror

As the device sizes are reducing the output impedance of the MOSFET is also reducing due to the channel length modulation. For having high gains we need high output impedance of the devices and short channel MOSFETs cannot provide high gain structures for which cascoding of MOSFETs is the obvious technique. Cascade MOSFETs increase the gains but it decreases the output signal swing as well. The technique is to use the self cascode structure which requires low compliance voltages at output nodes as compare to regular cascode and provides high output
impedance to give high output gains. This approach has potential applications in low voltage design.

A self-cascode is a 2-transistor structure which can easily be treated as a single composite transistor. The composite structure has higher effective channel length and the effective output conductance is much low. The lower transistor M₁ is equivalent to a resistor, where value is input dependant. For optimal operation, the W/L ratio of M₂ must be greater than that of M₁, i.e., m>l. For the composite transistor, the effective trans-conductance is given as

\[
g_{\text{m(\text{effective})}} = \frac{g_{m2}}{m} = g_{m1}
\]

Figure 4 Self Cascode Current mirror [6].

2.3 Multi Input Floating Gate Low Voltage Current Mirror

The Current Mirrors are basic elements for the design of low voltage circuits and many low voltage current mirror circuits have been developed. Most of these circuits have low compliance voltage at output node but many of them have high compliance voltage at the input node. There are few circuits only which have low input and output compliance voltages. However they have high offset current, thus limiting operating range. To increase their operating range, a technique named as multiple inputs floating gate (MIFG) need to be examined.

In multi input floating gate current mirror circuit the threshold voltage of MOSFET is made programmable with input current I_in. This can done by providing feedback of I_in which produce a voltage proportional to the I_in. This is done by passing I_in through a resistor. The voltage drop is high for high I_in while it will be low at low I_in. Hence the threshold voltage of the circuit is varied in accordance with the requirement of the circuit.
In Figure 5, the threshold voltage of $M_1$ is varied as per requirement of the circuit. For low value of $I_{in}$ threshold value is reduced and when $I_{in}$ is high threshold voltage increases as per requirement of the circuit.

### 2.4 Adaptive Biasing Low voltage current mirror

In Figure 6, the adaptive biasing Current mirror structure is shown.

Figure 5 Multi input floating gate Current mirror [7].

Figure 6 Adaptive biasing Current mirror structure [8].
In low voltage current mirror circuit, if $I_{in}$ increases then $V_{in}$ also increases. But this increase in $V_{in}$ can be compensated by increasing the value of $I_{bias}$. In adaptive biasing low voltage current mirror circuit the supply voltage is reduced by increasing the biasing current so that circuit should work at low voltage. Disadvantage of adaptive biasing is that there is always an offset current flow through circuit even in absence of input current. Figure 6 shows adaptive biasing low voltage structure.

3. PROPOSED LOW VOLTAGE CURRENT MIRROR CIRCUIT

3.1 Circuit Description

Figure 7 shows the proposed low-voltage current mirror circuit. In this proposed circuit the transistors $M_4$ and $M_5$ are generating the bias current. At node 1, two currents i.e. input current ($I_{in}$) and bias current ($I_{bias}$) are injecting in which the input current is transferred to the output terminal (node 4). In accordance with KCL, the value of W/L of transistor $M_0$ is chosen in such a manner that the current ($I_{in} + I_{b}$) will flow through it. The gate-to-source voltages of transistors $M_0$ and $M_1$ are equal hence; the same current ($I_{in} + I_{b}$) will flow through these transistors. Rest of the transistors are used to copy the currents and transfer to the relevant nodes. Finally, the output current ($I_{out}$) through transistor $M_8$ is same as the input current ($I_{in}$).

The bulk terminal of P-MOS $M_4$, $M_5$, $M_6$ and $M_7$ are connected to input current circuit for reducing the threshold voltage of P-MOS instead of connecting it supply $V_{dd}$. As a result of above connection the supply voltage is effectively reduced to $+0.85$ V.

![Figure 7 Proposed Low Voltage Current Mirror Circuit.](image)

In Figure 7 KCL at node 4, we get

$$I_{out} + I_{b} = I_{in} + I_{b} \quad (1)$$
Now (1) reduces

\[ I_{\text{out}} = I_{\text{in}} \]  

From (2), it is clear that the proposed circuit behaves as current mirror circuit. The Bulk terminal of PMOS used in the circuit is connected to input current source so as to provide biasing of PMOS. The current into bulk terminal is very small i.e. current necessary for biasing the PMOS. The transconductance parameters and parasitic capacitances of the transistors are selected as

\[ g_{m0} = g_{m1}; g_{m2} = g_{m3}; g_{m4} = g_{m5}; g_{mb} = g_{m7} \]

\[ C_{gs0} = C_{gs1}; C_{gs2} = C_{gs3}; C_{gs4} = C_{gs5}; C_{gs6} = C_{gs7} \]  

(3)

3.2 AC analysis of the proposed circuit.

In this section the AC analysis of the proposed current mirror circuit is discussed. The AC equivalent model of the proposed circuit is shown in Figure 8.

![AC equivalent model of proposed current mirror circuit](image)

Figure 8 AC equivalent model of proposed current mirror

In this model, it is assumed that

\[ C_1 = C_{gs0} + C_{gs1}; C_2 = C_{gs2} + C_{gs3}; C_3 = C_{gs4} + C_{gs5}; \]

\[ C_4 = C_{gs6} + C_{gs7}; C_5 = C_{gs8} \]  

(4)

From Figure 8, The output current \( I_{\text{out}} \) is

\[ I_{\text{out}} = g_{m8} V_{\text{out}} \]  

(5)

where \( g_{m8} \) is the transconductance of the transistor \( M_8 \) and \( V_0 \) is the output voltage.

Applying KCL at nodes 1, 2, 3 and 4 different expressions can be written as follows

\[ I_{\text{in}} - g_{m4} V_1 = g_{m0} V_1 + sC_3 V_1 + sC_1 V_1 \]  

(6)

\[ -g_{m5} V_1 = g_{m2} V_2 + sC_2 V_2 \]  

(7)
After simplification (6), (7), (8) and (9) reduces to (10), (11), (12) and (13) respectively as:

\[ I_{in} = V_1 \left[ g_{m0} + s c_1 + s c_3 + g_{m4} \right] \]  
\[ V_2 = \frac{-s g_{m5} V_1}{s c_2 + g_{m2}} \]  
\[ V_3 = \frac{-s g_{m6} V_1}{s c_4 + g_{m6}} \]  
\[ V_{out} (s c_5 + g_{m8}) = -(g_{m3} V_2 + g_{m7} V_3) \]

Substituting (11) and (12) in (13), the output voltage \( V_{out} \) is

\[ V_{out} = \frac{1}{(s c_5 + g_{m8}) (s c_2 + g_{m2}) (s c_4 + g_{m6})} \left[ g_{m5} g_{m6} V_1 + g_{m1} g_{m5} V_1 \right] \]

Using (14) in (5), the output current \( I_{out} \) is

\[ I_{out} = \frac{g_{m8} [g_{m1} g_{m5} (s c_2 + g_{m2}) + g_{m3} g_{m5} (s c_4 + g_{m6})]}{(s c_5 + g_{m8}) (s c_1 + s c_3 + g_{m0} + g_{m4}) (s c_2 + g_{m2}) (s c_4 + g_{m6})} \]

Dividing (15) by (10), the current gain is

\[ \frac{I_{out}}{I_{in}} = \frac{g_{m8} [g_{m1} g_{m5} (s c_2 + g_{m2}) + g_{m3} g_{m5} (s c_4 + g_{m6})]}{g_{m5} (s c_1 + s c_3 + g_{m0} + g_{m4}) (s c_2 + g_{m2}) (s c_4 + g_{m6})} \]

The above relation can be written as:

\[ \frac{I_{out}}{I_{in}} = \frac{g_{m8} \left[ g_{m1} g_{m5} \frac{s + g_{m2}}{c_2} + g_{m3} g_{m5} \frac{s + g_{m6}}{c_4} \right]}{g_{m5} \left( \frac{s + g_{m0}}{c_1} + \frac{s + g_{m4}}{c_4} \right) (\frac{s + g_{m2}}{c_2} + \frac{s + g_{m6}}{c_4})} \]

The transconductance parameters and parasitic capacitances of the transistors are selected as

\[ g_{m0} = g_{m1}; \quad g_{m2} = g_{m3}; \quad g_{m4} = g_{m5}; \quad g_{m6} = g_{m7} \]
\[ C_{g_{s0}} = C_{g_{s1}}; \quad C_{g_{s2}} = C_{g_{s3}}; \quad C_{g_{s4}} = C_{g_{s5}}; \quad C_{g_{s6}} = C_{g_{s7}} \]

Using (17) in (16), (16) becomes

\[ \frac{I_{out}}{I_{in}} = \frac{g_{m8} \left[ g_{m1} g_{m5} \frac{s + g_{m2}}{c_2} + g_{m3} g_{m5} \frac{s + g_{m6}}{c_4} \right]}{c_5 \left( \frac{s + g_{m0}}{c_1} + \frac{s + g_{m4}}{c_4} \right) (\frac{s + g_{m2}}{c_2} + \frac{s + g_{m6}}{c_4})} \]

From (18), it is clear that the transfer function exhibits a dominant pole \( s = -\frac{g_{m8}}{c_4} \) which decide the bandwidth of the proposed circuit.
3.3 Proposed current mirror circuit with enhanced bandwidth.

The bandwidth of the proposed circuit has been enhanced by customizing the circuit as shown in Figure 9. In this circuit, a resistance \( R \) is connected between drain and gate terminals of the transistor \( M_0 \). The working of circuit is similar to first circuit. In this figure, the resistance \( (R) \) connected between drain and gate terminals of the transistors \( M_0 \) which create the potential difference between two terminals.

![Figure 9 Proposed current mirror circuit with enhanced bandwidth.](image)

3.4 AC analysis of the proposed current mirror circuit with enhanced bandwidth.

In this section the AC analysis of the proposed circuit with enhanced bandwidth has been performed and the AC equivalent model of this circuit is shown in Figure 10.

![Figure 10 AC equivalent model of enhanced bandwidth current mirror circuit](image)

In this model, it is assumed that

\[
C_0 = C_{gs0}; \quad C_1 = C_{gs1}; \quad C_2 = C_{gs2} + C_{gs3}; \quad C_3 = C_{gs4} + C_{gs5};
\]

\[
C_4 = C_{gs6} + C_{gs7}; \quad C_5 = C_{gs0}
\]  

(19)
From Figure 10, the output current $I_{out}$ is

$$I_{out} = g_{m8}V_{out}$$  \hspace{1cm} (20)

where $g_{m8}$ is the transconductance of the transistor $M_8$ and $V_0$ is the output voltage.

Applying KCL at nodes 1, 2, 3 and 4 different expressions can be written as follows

$$I_{in} - g_{m4}V_1 = g_{m0}V_1 + sC_3V_1 + sC_1V_1 + \frac{V_2 - V_0}{R}$$  \hspace{1cm} (21)

$$-g_{m3}V_1 = g_{m2}V_2 + sC_2V_2$$  \hspace{1cm} (22)

$$-g_{m6}V_3 = g_{m1}V_1 + sC_4V_3$$  \hspace{1cm} (23)

$$-g_{m7}V_3 = g_{m8}V_{out} + g_{m3}V_2 + sC_5V_{out}$$  \hspace{1cm} (24)

$$\frac{V_3 - V_2}{R} + sC_0V_0 = 0$$  \hspace{1cm} (25)

where $g_{mi}$ ($i = 0$ to 8) is the transconductance of the $i^{th}$ transistor. Voltages $V_0$, $V_1$, $V_2$ and $V_3$ are the voltages at nodes 0, 1, 2 and 3 respectively.

After simplification (21), (22), (23), (24) and (25) reduces to (26), (27), (28), (29) and (30) respectively as:

$$I_{in} = V_1 \left[g_{m4} + \frac{1}{R} + C_1 + C_3\right] + V_0 \left[g_{m0} - \frac{1}{R}\right]$$  \hspace{1cm} (26)

$$V_2 = \frac{-g_{m3}V_1}{(sC_2 + g_{m2})}$$  \hspace{1cm} (27)

$$V_3 = \frac{-g_{m1}V_1}{(sC_4 + g_{m6})}$$  \hspace{1cm} (28)

$$V_0 = \frac{V_3}{1 + RsC_0}$$  \hspace{1cm} (29)

Substituting (29) in (26), the input current $I_{in}$ is

$$I_{in} = V_1 \left[g_{m4} + \frac{1}{R} + sC_1 + sC_3\right] + \frac{V_1}{1 + RsC_0} \left[g_{m0} - \frac{1}{R}\right]$$  \hspace{1cm} (30)

With further calculation (30), may be written as

$$I_{in} = \frac{V_3 \left[2RsC_0(C_1 + C_3) + s(Rg_{m4}C_0 + C_1 + C_2) + sC_0 + sC_4\right]}{(1 + RsC_0)}$$  \hspace{1cm} (31)

Using (27) and (28) in (24), the output voltage $V_{out}$ is

$$V_{out} = \frac{1}{(sC_2 + g_{m2})} \left[\frac{g_{m2}g_{m3}V_2}{(sC_2 + g_{m2})} + \frac{g_{m1}g_{m2}V_3}{(sC_4 + g_{m6})}\right]$$  \hspace{1cm} (32)

Substituting (32) in (20), the output current $I_{out}$ is

$$I_{out} = \frac{g_{m0}}{(sC_2 + g_{m2})} \left[\frac{g_{m2}g_{m3}V_2}{(sC_2 + g_{m2})} + \frac{g_{m1}g_{m2}V_3}{(sC_4 + g_{m6})}\right]$$  \hspace{1cm} (33)

Dividing (33) by (31), the current gain is
The above relation can be written as:

\[
\frac{I_{\text{out}}}{I_{\text{in}}} = \frac{g_{m0}\left[g_{m1}g_{m7}(sc_2 + g_{m2}) + g_{m3}g_{m5}(sc_4 + g_{m6})\right]}{(sc_6 + g_{m6})(sc_2 + g_{m2})(sc_4 + g_{m4})}
\times \frac{(s + \frac{g_{m2}}{c_2})(s + \frac{g_{m4}}{c_4})(s + \frac{g_{m6}}{c_6})}{(s + \frac{g_{m0} + g_{m4}}{c_1 + c_3})}
\times \frac{1}{\left(c_4 + c_2\right)^2 + \left(g_{m0}R_c + g_{m4}\right)c_2 + g_{m4}c_2}
\]

(34)

From (37), it is clear that the transfer function has two zeros and five poles. In (18), the transfer function consists of one zero and four poles. Therefore, it is visible that the resistance R connected between drain and gate of the transistor M0 proposes a zero and a pole in the transfer function of Figure 9. This proposed zero cancels the dominant pole and therefore, the bandwidth of the proposed circuit (Figure 7) is now improved.

The MOSFET sizes in case of channel width to length ratio are listed in Table 1

<table>
<thead>
<tr>
<th>MOSFET</th>
<th>W/L Ratio (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M0</td>
<td>44.8/2.0</td>
</tr>
<tr>
<td>M1</td>
<td>44.8/2.0</td>
</tr>
<tr>
<td>M2</td>
<td>1.8/0.9</td>
</tr>
<tr>
<td>M3</td>
<td>1.8/0.9</td>
</tr>
<tr>
<td>M4</td>
<td>5.3/0.9</td>
</tr>
<tr>
<td>M5</td>
<td>5.3/0.9</td>
</tr>
<tr>
<td>M6</td>
<td>93.6/1.44</td>
</tr>
<tr>
<td>M7</td>
<td>93.6/1.44</td>
</tr>
<tr>
<td>M8</td>
<td>16.38/0.9</td>
</tr>
</tbody>
</table>
4. SIMULATION RESULTS

4.1 Current Transfer characteristics.

The proposed current mirror is simulated using Cadence Design Environment in the UMC 180 nm CMOS Technology. This proposed current mirror circuit is operated with supply voltage of +0.85 V. Figure 11 shows the current transfer characteristics of the proposed circuit and plots the graph between output current and input current. The input current changes from 0 to 100 uA. From the plot, it is seen that output current follow the input current with ±10% error in copying current.

![Figure 11 DC characteristics of the proposed current mirror circuit.](image)

4.2 AC characteristics.

Figure 12 shows the frequency response of the proposed circuit. In this figure current gain versus frequency graph is plotted. In the same figure, frequency response of the proposed current mirror circuit with bandwidth enhancement resistor (R1=3.7KΩ) is also plotted. The bandwidths of the proposed circuits without and with compensation resistor are 38 MHz and 92 MHz, respectively.

![Figure 12 Frequency response of the proposed circuit.](image)
TABLE 2 Comparison of proposed current mirror with other reported current mirror.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply</td>
<td>+1.5 V</td>
<td>+1.3 V</td>
<td>+0.85 V</td>
</tr>
<tr>
<td>CMOS Technology</td>
<td>180 nm</td>
<td>180 nm</td>
<td>180 nm</td>
</tr>
<tr>
<td>Input Current Range</td>
<td>0 to 100uA</td>
<td>0 to 100uA</td>
<td>0 to 100uA</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>577MHz</td>
<td>163MHz</td>
<td>92MHz</td>
</tr>
</tbody>
</table>

5. CONCLUSION

This work presents a new low voltage current mirror circuit operating with a supply voltage of +0.85 V. The proposed circuit can be used for a wide variety of low voltage and low power applications. The bandwidth of the circuit has been enhanced using resistive compensation technique. The mathematical analysis of the proposed low voltage current mirror has also been presented. The simulation results have been presented to validate the usefulness of the proposed current mirror circuit.

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