A NEW LOW VOLTAGE P-MOS BULK DRIVEN CURRENT MIRROR CIRCUIT

Anuj Dugaya[1] and Laxmi Kumre[2]

[1]Department of Electronics and Communication Engineering, Maulana Azad National Institute of Technology, Bhopal, India
akdugaya@gmail.com
[2]Department of Electronics and Communication Engineering, Maulana Azad National Institute of Technology, Bhopal, India
laxmikumre99@rediffmail.com

ABSTRACT

This work proposes a new low voltage current mirror circuit using bulk driven technique. Bulk driven technique is used to reduce the threshold of PMOS used in low voltage current mirror circuits (LVCM).The Proposed circuit consist of 4 PMOS and 5 NMOS. The proposed circuit operated at +0.85 V supply voltage.The bandwidth of this circuit has also been enhanced using resistive compensation technique. The proposed circuit has been simulated in Cadence Design Environment in UMC 180nm CMOS technology. A transfer characteristic of the proposed circuit has been discussed. The proposed circuit find application in low voltage and low power analog integrated circuits.

KEYWORDS

Low voltage, Current Mirror, Bulk driven.

1. INTRODUCTION

Advances in CMOS technology have made it feasible to design chips with high packaging density, better performance and lower power consumption. To attain these goals, the size of the CMOS devices has been scaled down to very small features and dimensions. However, the power supply voltage has not been scaled down proportionally to ultra-deep sub-micron technology. The limitation of low voltage circuit design using the existing technology is that the power supply must be at least equal to the sum of the magnitude of the threshold voltages of cascaded P-MOS and N-MOS transistors. There are several techniques, such as bulk-driven, sub-threshold, self cascode, and floating-gate has been evolved to construct high performance analog circuits under low power supply voltages. Figure 1 shows the symbols of current mirror circuits in which arrow is used to show the direction of the current flow on the input side. The ratio 1: K shows the current gain of the Current mirror circuit.

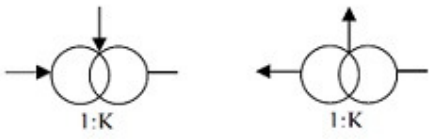

Figure 1 Current Mirror symbols (a) NMOS current mirror (b) PMOS current mirror.

DOI : 10.5121/vlsic.2013.4405

The bulk-driven technique is used to scale down the threshold voltage of PMOS transistor used in circuit. The body terminal of PMOS is connected to input to provide weak positive bias so that threshold voltage of PMOS is reduced and supply voltage is effectively scale down. This technique is completely compatible with standard CMOS process.

Current mirror (CM) circuits are widely used in analog integrated circuit. It is clear from its name that it copies the current. Current mirror are circuits whose output current is independent of output terminal voltage and depends on input current only. They are used for current amplification, biasing, active loading and level shifting. Efficient design of current mirror circuit improves the overall performance of analog integrated circuit and reduces the supply voltage requirement of the circuit.

2. PREVIOUSLY REPORTED CURRENT MIRROR CIRCUITS

2.1 Very Low Input impedance Low Power Current Mirror

In order to get low input impedance, the main idea is to introduce transistor M_3 in series with the input terminal of the basic circuit of the current mirror and use a gain amplifier of '−A' gain to control the gate voltage of M_3. In Figure 2 (a) a simple current mirror is shown and in Figure 2 (b) conceptual schematic of the current mirror. Any increase in source voltage of M_3 (i.e. due to injected input current) causes its gate voltage to decrease '−A' times, hence causing stronger sink of input current which results in decrease of input impedance by 'A' times.

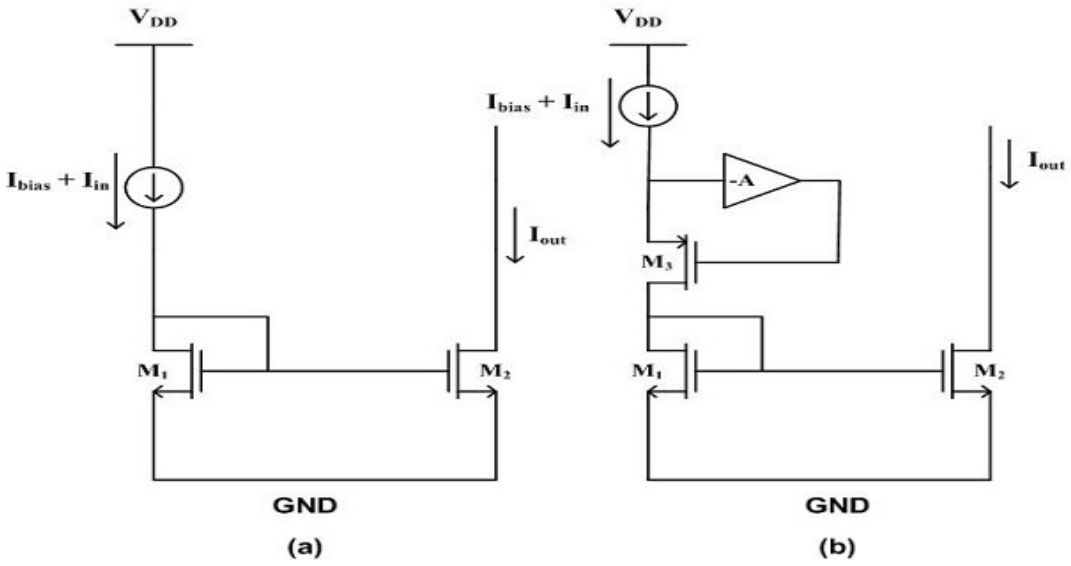

Figure 2 (a) Simple current mirror (b) Conceptual schematic of the current mirror [4].

2.2 Self Cascode Current Mirror

As the device sizes are reducing the output impedance of the MOSFET is also reducing due to the channel length modulation. For having high gains we need high output impedance of the devices and short channel MOSFETs cannot provide high gain structures for which cascoding of MOSFETs is the obvious technique. Cascode MOSFETs increase the gains but it decreases the output signal swing as well. The technique is to use the self cascode structure which requires low compliance voltages at output nodes as compare to regular cascode and provides high output

impedance to give high output gains. This approach has potential applications in low voltage design.

A self-cascode is a 2-transistor structure which can easily be treated as a single composite transistor. The composite structure has higher effective channel length and the effective output conductance is much low. The lower transistor M_1 is equivalent to a resistor, where value is input dependant. For optimal operation, the *W/L* ratio of M_2 must be greater than that of M_1, i.e., m>l. For the composite transistor, the effective trans-conductance is given as

$$g_{m(effective)} = \frac{g_{m2}}{m} = g_{m1}$$

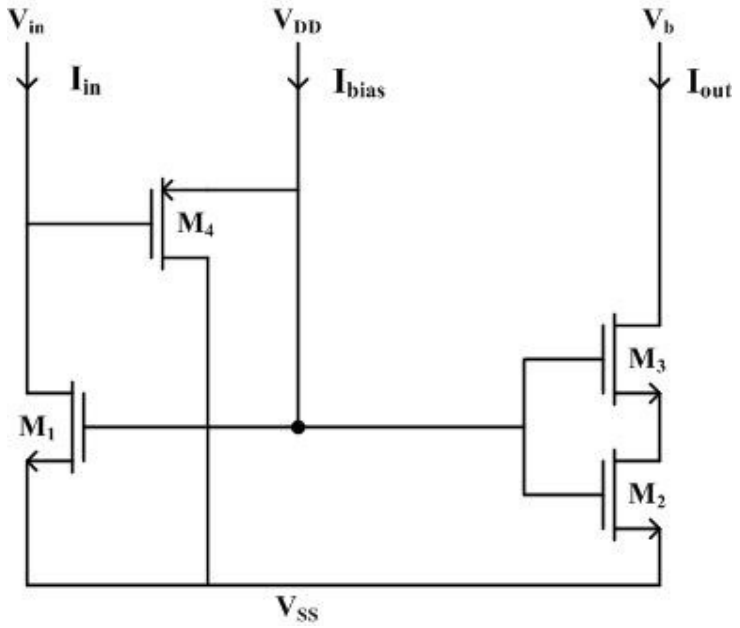

Figure 4 Self Cascode Current mirror [6].

2.3 Multi Input Floating Gate Low Voltage Current Mirror

The Current Mirrors are basic elements for the design of low voltage circuits and many low voltage current mirror circuits have been developed. Most of these circuits have low compliance voltage at output node but many of them have high compliance voltage at the input node. There are few circuits only which have low input and output compliance voltages. However they have high offset current, thus limiting operating range. To increase their operating range, a technique named as multiple inputs floating gate (MIFG) need to be examined.

In multi input floating gate current mirror circuit the threshold voltage of MOSFET is made programmable with input current I_{in} .This can done by providing feedback of I_{in} which produce a voltage proportional to the I_{in}. This is done by passing I_{in} through a resistor. The voltage drop is high for high I_{in} while it will be low at low I_{in}. Hence the threshold voltage of the circuit is varied in accordance with the requirement of the circuit.

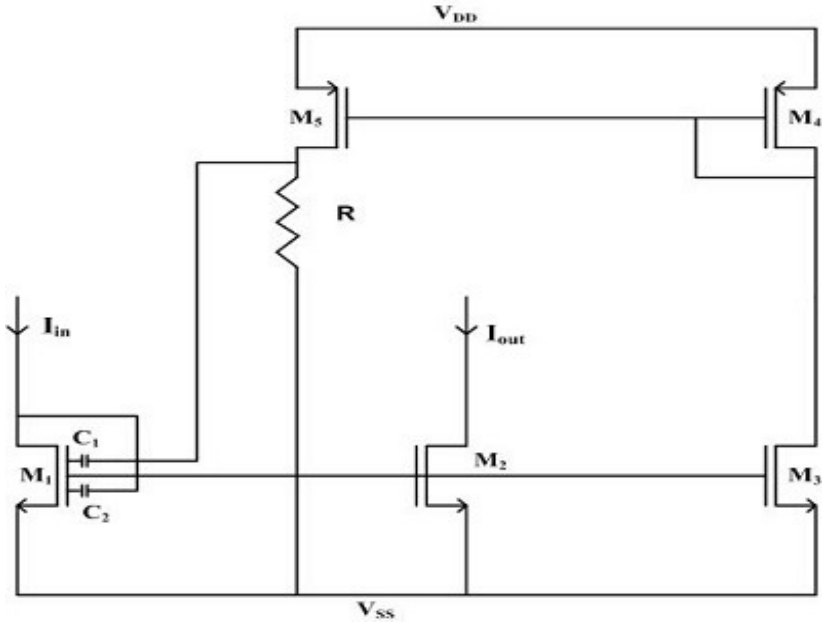

Figure 5 Multi input floating gate Current mirror [7].

In Figure 5, the threshold voltage of M_1 is varied as per requirement of the circuit. For low value of I_{in} threshold value is reduced and when I_{in} is high threshold voltage increases as per requirement of the circuit.

2.4 Adaptive Biasing Low voltage current mirror

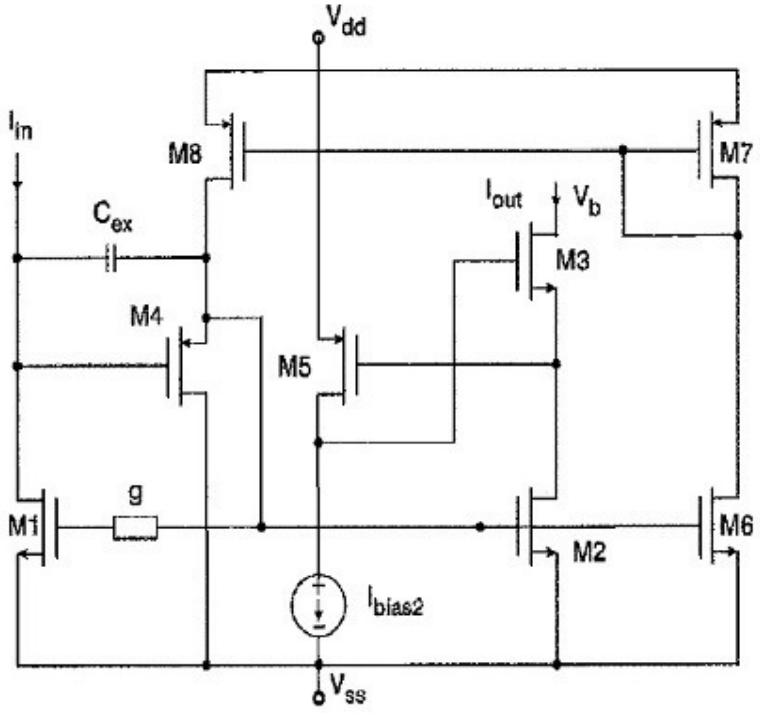

Figure 6 Adaptive biasing Current mirror structure [8].

In low voltage current mirror circuit, if I_{in} increases then V_{in} also increases. But this increase in V_{in} can be compensated by increasing the value of I_{bias}. In adaptive biasing low voltage current mirror circuit the supply voltage is reduced by increasing the biasing current so that circuit should work at low voltage. Disadvantage of adaptive biasing is that there is always an offset current flow through circuit even in absence of input current. Figure 6 shows adaptive biasing low voltage structure.

3. PROPOSED LOW VOLTAGE CURRENT MIRROR CIRCUIT

3.1 Circuit Description

Figure 7 shows the proposed low-voltage current mirror circuit. In this proposed circuit the transistors M_4 and M_5 are generating the bias current. At node 1, two currents i.e. input current (I_{in}) and bias current (I_{bias}) are injecting in which the input current is transferred to the output terminal (node 4).In accordance with KCL, the value of W/L of transistor M_0 is chosen in such a manner that the current ($I_{in} + I_b$) will flow through it. The gate-to-source voltages of transistors M_0 and M_1 are equal hence; the same current ($I_{in} + I_b$) will flow through these transistors. Rest of the transistors are used to copy the currents and transfer to the relevant nodes. Finally, the output current (I_{out}) through transistor M_8 is same as the input current (I_{in}).

The bulk terminal of P-MOS M_4, M_5, M_6 and M_7 are connected to input current circuit for reducing the threshold voltage of P-MOS instead of connecting it supply V_{dd}. As a result of above connection the supply voltage is effectively reduced to + 0.85 V.

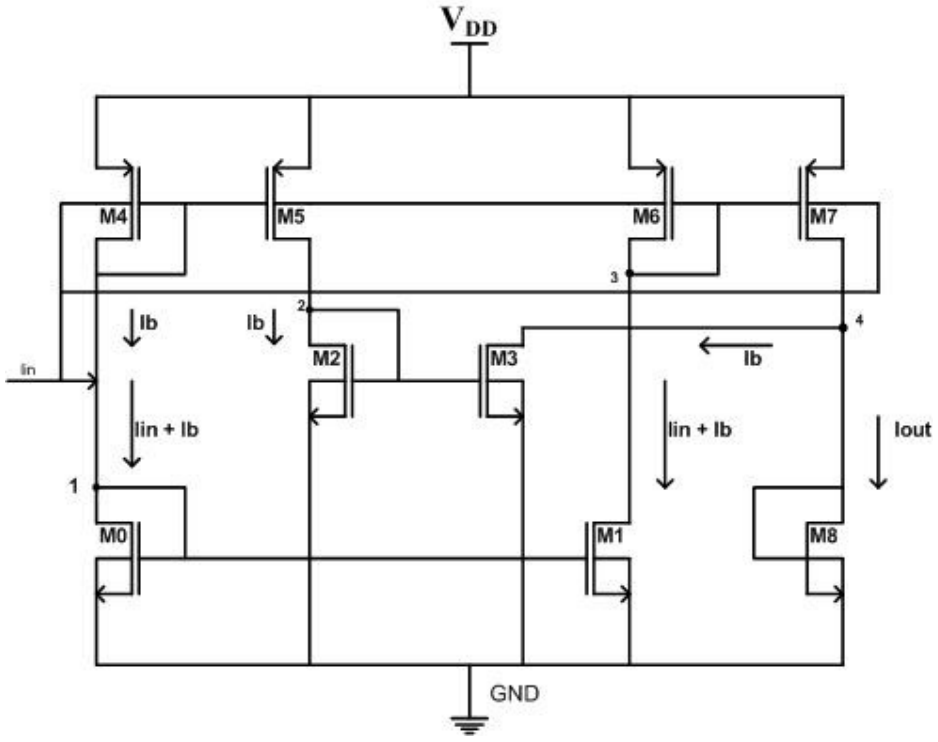

Figure 7 Proposed Low Voltage Current Mirror Circuit.

In Figure 7 KCL at node 4, we get

$$I_{out} + I_b = I_{in} + I_b \quad (1)$$

Now (1) reduces

$$I_{out} = I_{in} \tag{2}$$

From (2), it is clear that the proposed circuit behaves as current mirror circuit. The Bulk terminal of PMOS used in the circuit is connected to input current source so as to provide biasing of PMOS. The current into bulk terminal is very small i.e. current necessary for biasing the PMOS. The transconductance parameters and parasitic capacitances of the transistors are selected as

$$g_{m0} = g_{m1}; g_{m2} = g_{m3}; g_{m4} = g_{m5}; g_{m6} = g_{m7}$$
$$C_{gs0} = C_{gs1}; C_{gs2} = C_{gs3}; C_{gs4} = C_{gs5}; C_{gs6} = C_{gs7} \tag{3}$$

3.2 AC analysis of the proposed circuit.

In this section the AC analysis of the proposed current mirror circuit is discussed. The AC equivalent model of the proposed circuit is shown in Figure 8

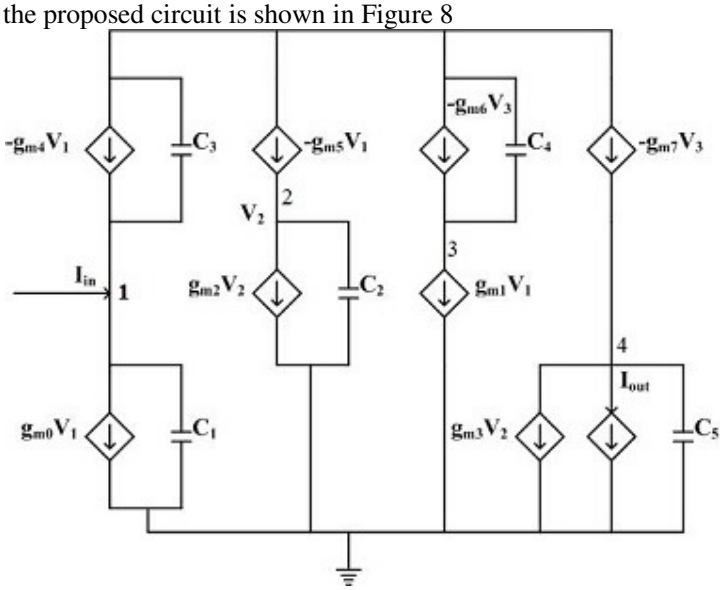

Figure 8 AC equivalent model of proposed current mirror

In this model, it is assumed that

$$C_1 = C_{gs0} + C_{gs1}; C_2 = C_{gs2} + C_{gs3}; C_3 = C_{gs4} + C_{gs5};$$
$$C_4 = C_{gs6} + C_{gs7}; C_5 = C_{gs8} \tag{4}$$

From Figure 8, The output current I_{out} is

$$I_{out} = g_{m8} V_{out} \tag{5}$$

where g_{m8} is the transconductance of the transistor M_8 and V_0 is the output voltage.
Applying KCL at nodes 1, 2, 3 and 4 different expressions can be written as follows

$$I_{in} - g_{m4} V_1 = g_{m0} V_1 + sc_3 V_1 + sc_1 V_1 \tag{6}$$
$$-g_{m5} V_1 = g_{m2} V_2 + sc_2 V_2 \tag{7}$$

$$-g_{m6}V_3 = g_{m1}V_1 + sc_4V_3 \quad (8)$$

$$-g_{m7}V_3 = g_{m8}V_{out} + g_{m3}V_2 + sc_5V_{out} \quad (9)$$

After simplification (6), (7), (8) and (9) reduces to (10), (11), (12) and (13) respectively as:

$$I_{in} = V_1[g_{m0} + sc_1 + sc_3 + g_{m4}] \quad (10)$$

$$V_2 = \frac{-g_{m5}V_1}{(sc_2+g_{m2})} \quad (11)$$

$$V_3 = \frac{-g_{m1}V_1}{(sc_4+g_{m6})} \quad (12)$$

$$V_{out}(sc_5 + g_{m8}) = -(g_{m3}V_2 + g_{m7}V_3) \quad (13)$$

Substituting (11) and (12) in (13), the output voltage V_{out} is

$$V_{out} = \frac{1}{(sc_5+g_{m8})}\left[\frac{g_{m3}g_{m5}V_1}{(sc_2+g_{m2})} + \frac{g_{m1}g_{m7}V_1}{(sc_4+g_{m6})}\right] \quad (14)$$

Using (14) in (5), the output current I_{out} is

$$I_{out} = \frac{g_{m8}}{(sc_5+g_{m8})}\left[\frac{g_{m3}g_{m5}V_1}{(sc_2+g_{m2})} + \frac{g_{m1}g_{m7}V_1}{(sc_4+g_{m6})}\right] \quad (15)$$

Dividing (15) by (10), the current gain is

$$\frac{I_{out}}{I_{in}} = \frac{g_{m8}[g_{m1}g_{m7}(sc_2+g_{m2})+g_{m3}g_{m5}(sc_4+g_{m6})]}{(sc_5+g_{m8})(sc_1+sc_3+g_{m0}+g_{m4})(sc_2+g_{m2})(sc_4+g_{m6})}$$

The above relation can be written as:

$$\frac{I_{out}}{I_{in}} = \frac{g_{m8}\left[\frac{g_{m1}g_{m7}}{c_4}\left(s+\frac{g_{m2}}{c_2}\right)+\frac{g_{m3}g_{m5}}{c_2}\left(s+\frac{g_{m6}}{c_4}\right)\right]}{c_5(c_1+c_3)\left(s+\frac{g_{m2}}{c_2}\right)\left(s+\frac{g_{m6}}{c_4}\right)\left(s+\frac{g_{m8}}{c_5}\right)\left(s+\frac{g_{m0}+g_{m4}}{c_1+c_3}\right)} \quad (16)$$

The transconductance parameters and parasitic capacitances of the transistors are selected as

$$g_{m0} = g_{m1};\quad g_{m2} = g_{m3};\quad g_{m4} = g_{m5};\quad g_{m6} = g_{m7}$$
$$C_{gs0} = C_{gs1}; C_{gs2} = C_{gs3}; C_{gs4} = C_{gs5}; C_{gs6} = C_{gs7} \quad (17)$$

Using (17) in (16), (16) becomes

$$\frac{I_{out}}{I_{in}} = \frac{g_{m8}\left[\frac{g_{m1}g_{m7}}{c_4}\left(s+\frac{g_{m2}}{c_2}\right)+\frac{g_{m3}g_{m5}}{c_2}\left(s+\frac{g_{m6}}{c_4}\right)\right]}{c_5(c_1+c_3)\left(s+\frac{g_{m2}}{c_2}\right)\left(s+\frac{g_{m6}}{c_4}\right)\left(s+\frac{g_{m8}}{c_5}\right)\left(s+\frac{g_{m0}+g_{m4}}{c_1+c_3}\right)} \quad (18)$$

From (18), it is clear that the transfer function exhibits a dominant pole $\left(\text{at } s = -\frac{g_{m6}}{c_4}\right)$ which decide the bandwidth of the proposed circuit.

3.3 Proposed current mirror circuit with enhanced bandwidth.

The bandwidth of the proposed circuit has been enhanced by customizing the circuit as shown in Figure 9. In this circuit, a resistance R is connected between drain and gate terminals of the transistor M_0. The working of circuit is similar to first circuit. In this figure, the resistance (R) connected between drain and gate terminals of the transistors M_0 which create the potential difference between two terminals.

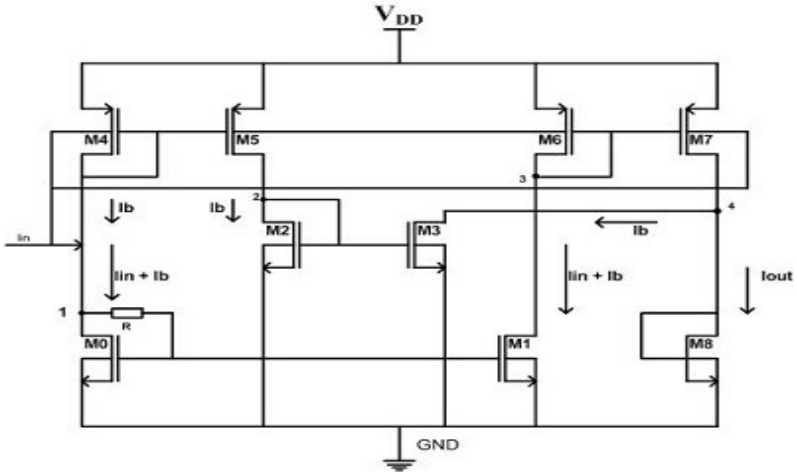

Figure 9 Proposed current mirror circuit with enhanced bandwidth.

3.4 AC analysis of the proposed current mirror circuit with enhanced bandwidth.

In this section the AC analysis of the proposed circuit with enhanced bandwidth has been performed and the AC equivalent model of this circuit is shown in Figure 10

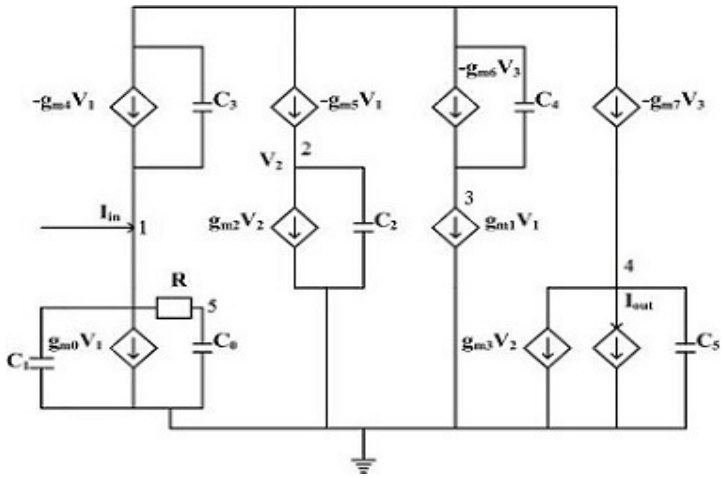

Figure 10 AC equivalent model of enhanced bandwidth current mirror circuit

In this model, it is assumed that

$$C_0 = C_{gs0}; C_1 = C_{gs1}; C_2 = C_{gs2} + C_{gs3}; C_3 = C_{gs4} + C_{gs5};$$
$$C_4 = C_{gs6} + C_{gs7}; C_5 = C_{gs8} \quad (19)$$

From Figure 10, The output current I_{out} is

$$I_{out} = g_{m8} V_{out} \tag{20}$$

where g_{m8} is the transconductance of the transistor M_8 and V_0 is the output voltage.

Applying KCL at nodes 1, 2, 3 and 4 different expressions can be written as follows

$$I_{in} - g_{m4} V_1 = g_{m0} V_1 + sc_3 V_1 + sc_1 V_1 + \frac{V_1 - V_0}{R} \tag{21}$$

$$-g_{m5} V_1 = g_{m2} V_2 + sc_2 V_2 \tag{22}$$

$$-g_{m6} V_3 = g_{m1} V_1 + sc_4 V_3 \tag{23}$$

$$-g_{m7} V_3 = g_{m8} V_{out} + g_{m3} V_2 + sc_5 V_{out} \tag{24}$$

$$\frac{V_0 - V_1}{R} + sc_0 V_0 = 0 \tag{25}$$

where g_{mi} (i = 0 to 8) is the transconductance of the i^{th} transistor. Voltages V_0, V_1, V_2 and V_3 are the voltages at nodes 0, 1, 2 and 3 respectively.

After simplification (21), (22), (23), (24) and (25) reduces to (26), (27), (28), (29) and (30) respectively as:

$$I_{in} = V_1 \left[g_{m4} + \frac{1}{R} + c_1 + c_3 \right] + V_0 \left[g_{m0} - \frac{1}{R} \right] \tag{26}$$

$$V_2 = \frac{-g_{m5} V_1}{(sc_2 + g_{m2})} \tag{27}$$

$$V_3 = \frac{-g_{m1} V_1}{(sc_4 + g_{m6})} \tag{28}$$

$$V_0 = \frac{V_1}{1 + RsC_0} \tag{29}$$

Substituting (29) in (26), the input current I_{in} is

$$I_{in} = V_1 \left[g_{m4} + \frac{1}{R} + sc_1 + sc_3 \right] + \frac{V_1}{1 + Rsc_0} \left[g_{m0} - \frac{1}{R} \right] \tag{30}$$

With further calculation (30), may be written as

$$I_{in} = \frac{V_1 [s^2 Rc_0 (c_1 + c_3) + s(Rg_{m4} c_0 + c_0 + c_1 + c_2) + g_{m0} + g_{m4}]}{(1 + Rsc_0)} \tag{31}$$

Using (27) and (28) in (24), the output voltage V_{out} is

$$V_{out} = \frac{1}{(sc_5 + g_{m8})} \left[\frac{g_{m3} g_{m5} V_1}{(sc_2 + g_{m2})} + \frac{g_{m1} g_{m7} V_1}{(sc_4 + g_{m6})} \right] \tag{32}$$

Substituting (32) in (20), the output current I_{out} is

$$I_{out} = \frac{g_{m8}}{(sc_5 + g_{m8})} \left[\frac{g_{m3} g_{m5} V_1}{(sc_2 + g_{m2})} + \frac{g_{m1} g_{m7} V_1}{(sc_4 + g_{m6})} \right] \tag{33}$$

Dividing (33) by (31), the current gain is

$$\frac{I_{out}}{I_{in}} = \frac{g_{m8}[g_{m1}g_{m7}(sc_2 + g_{m2}) + g_{m3}g_{m5}(sc_4 + g_{m6})]}{(sc_5 + g_{m8})(sc_2 + g_{m2})(sc_4 + g_{m6})} \times \frac{(Rsc_0+1)}{[s^2Rc_0(c_1+c_3)+s(Rg_{m4}c_0+c_0+c_1+c_3)+g_{m0}+g_{m4}]} \quad (34)$$

The above relation can be written as:

$$\frac{I_{out}}{I_{in}} = \frac{g_{m8}\left[\frac{g_{m1}g_{m7}}{c_4}\left(s + \frac{g_{m2}}{c_2}\right) + \frac{g_{m3}g_{m5}}{c_2}\left(s + \frac{g_{m6}}{c_4}\right)\right]}{\left(s + \frac{g_{m2}}{c_2}\right)\left(s + \frac{g_{m6}}{c_4}\right)\left(s + \frac{g_{m8}}{c_5}\right)\left(s + \frac{g_{m0} + g_{m4}}{c_1 + c_3}\right)} \times \frac{(s+\frac{1}{Rc_0})}{(c_1+c_3)\left[s^2 + s\frac{c_0(1+g_{m4}R)+c_1+c_3}{(c_1+c_3)} + \frac{g_{m0}+g_{m4}}{(c_1+c_3)}\right]} \quad (35)$$

The transconductance parameters and parasitic capacitances of the transistors are selected as

$$g_{m0} = g_{m1};\quad g_{m2} = g_{m3};\quad g_{m4} = g_{m5};\quad g_{m6} = g_{m7}$$
$$C_{gs0} = C_{gs1}; C_{gs2} = C_{gs3}; C_{gs4} = C_{gs5}; C_{gs6} = C_{gs7} \quad (36)$$

Using (36) in (35), (35) becomes

$$\frac{I_{out}}{I_{in}} = \frac{g_{m8}\left[\frac{g_{m0}g_{m6}}{c_4}\left(s + \frac{g_{m2}}{c_2}\right) + \frac{g_{m2}g_{m4}}{c_2}\left(s + \frac{g_{m6}}{c_4}\right)\right]}{\left(s + \frac{g_{m2}}{c_2}\right)\left(s + \frac{g_{m6}}{c_4}\right)\left(s + \frac{g_{m8}}{c_5}\right)\left(s + \frac{g_{m0} + g_{m4}}{c_1 + c_3}\right)} \times \frac{(s+\frac{1}{Rc_0})}{(c_1+c_3)\left[s^2 + s\frac{c_0(1+g_{m4}R)+c_1+c_3}{(c_1+c_3)} + \frac{g_{m0}+g_{m4}}{(c_1+c_3)}\right]} \quad (37)$$

From (37), it is clear that the transfer function has two zeros and five poles. In (18), the transfer function consist of one zero and four poles. Therefore, it is visible that the resistance R connected between drain and gate of the transistor M_0 proposes a zero and a pole in the transfer function of Figure 9. This proposed zero cancels the dominant pole and therefore, the bandwidth of the proposed circuit (Figure 7) is now improved.

The MOSFETs sizes in case of channel width to length ratio are listed in Table 1

Table 1 MOSFET Channel Width to length ratio

MOSFET	W/L Ratio (μm)
M_0	44.8/2.0
M_1	44.8/2.0
M_2	1.8/0.9
M_3	1.8/0.9
M_4	5.3/0.9
M_5	5.3/0.9
M_6	93.6/1.44
M_7	93.6/1.44
M_8	16.38/0.9

4. SIMULATION RESULTS

4.1 Current Transfer characteristics.

The proposed current mirror is simulated using Cadence Design Environment in the UMC 180 nm CMOS Technology. This proposed current mirror circuit is operated with supply voltage of +0.85 V. Figure 11 shows the current transfer characteristics of the proposed circuit and plots the graph between output current and input current. The input current changes from 0 to 100 uA. From the plot, it is seen that output current follow the input current with $\pm$ 10% error in copying current.

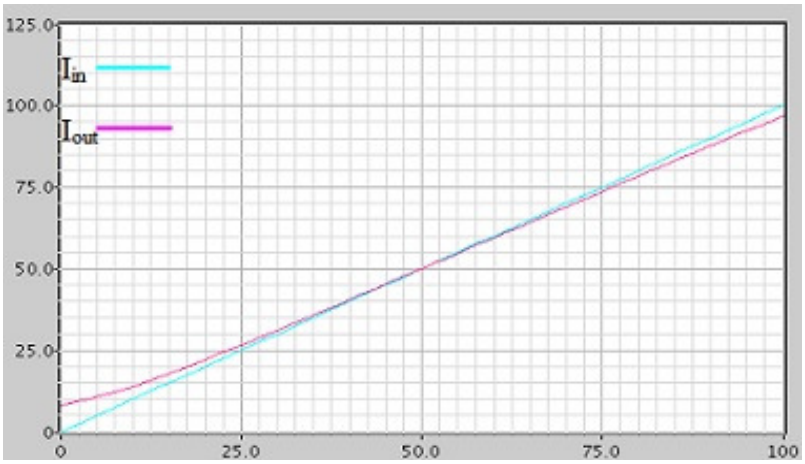

Figure 11 DC characteristics of the proposed current mirror circuit.

4.2 AC characteristics.

Figure 12 shows the frequency response of the proposed circuit. In this figure current gain versus frequency graph is plotted. In the same figure, frequency response of the proposed current mirror circuit with bandwidth enhancement resistor (R_1=3.7KΩ) is also plotted. The bandwidths of the proposed circuits without and with compensation resistor are 38 MHz and 92 MHz, respectively.

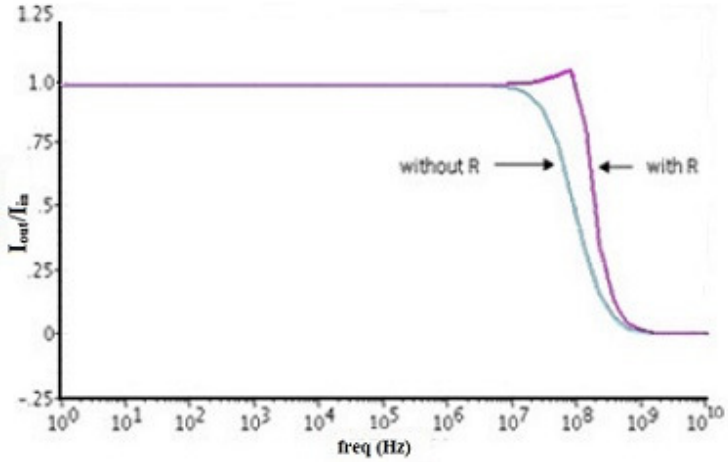

Figure 12 Frequency response of the proposed circuit.

TABLE 2 Comparison of proposed current mirror with other reported current mirror.

Circuit Parameters	Current mirror [4]	Current mirror [1]	Proposed current mirror
Power supply	+1.5 V	+1.3 V	+0.85 V
CMOS Technology	180 nm	180nm	180nm
Input Current Range	0 to 100uA	0 to 100uA	0 to 100uA
Bandwidth	577MHz	163MHz	92MHz

5. CONCLUSION

This work presents a new low voltage current mirror circuit operating with a supply voltage of +0.85 V. The proposed circuit can be used for wide variety of low voltage and low power application. The bandwidth of the circuit has been enhanced using resistive compensation technique. The mathematical analysis of the proposed low voltage current mirror has also been presented.The simulation results have been presented to validate the usefulness of the proposed current mirror circuit.

ACKNOWLEDGEMENTS

First of all, i am thankful to mrs. laxmi kumre, assistant professor, electronics and communication engineering department, maulana azad national institute of technology, bhopal for his patient guidance and support throughout this work.

I am thankful to entire faculty and staff electronics and communication engineering department. Finally, i would like to thank my family and friends for standing by me through all the joys and sorrows that life had to offer.

REFERENCES

[1] Manish Tikyani and Rishikesh pandey, “A New Low-Voltage Current Mirror Circuit with Enhanced Bandwidth”, International Conference on Computational Intelligence and Communication Networks, pp 42-46, Oct 2011.

[2] Naresh Lakkamraju and Ashis Kumar Lal, “A Low Voltage High Output Impedance Bulk Driven Regulated Cascode Current Mirror.” International Conference on Electronics Computer Technology (ICECT), pp. 79-83, April 2011.

[3] F. Khateb, D. Biolek, N.Khatib and Vavra, “Utilizing the Bulk Driven Technique in Analog Circuit Design.” IEEE DDCES 2010, pp. 16-19, 14-16 April 2010.

[4] Hassan Faraji Baghtash and Seyed Javad Azhari, “Very low input impedance low power current mirror,” Analog Integrated Circuits and Signal Processing, Vol. 66, No. 1, pp. 9-18, 2010.

[5] B.Aggrawal, M.Gupta, “Low Voltage Cascode Current Mirror Based on Bulk Driven MOSFET and FGMOS Techniques.” International Conference on Advances in Recent Technologies in Communication and Computing, pp.473-477, 2009.

[6] Jasdeep Kaur, Nupur Prakash and S.S. Rajput, “Low voltage high performance self cascade CCII.” IEEE Proc.-INMIC, pp. 7-11, Dec 2008.

[7] Susheel Sharma, S.S. Rajput, L.K. Magotra and S.S Jamuar, “FGMOS based wide range low voltage current mirror and its applications.” Asia-Pacific Conference on Circuits and Systems, Vol. 2, pp. 331 – 334, Oct 2002.

[8] S. S. Rajput and S. S Jamuar, "Low voltage, low power, high performance current mirror for portable analogue and mixed mode applications," IEEE Proc.-Circuits, Devices and systems, Vol. 148, No. 5, pp. 273-278, Oct 2001.
[9] Z.Zhu, J.Mo, Y.Yang, "A Low Voltage Bulk-driving PMOS Cascode Current Mirror." International Conference on Solid State and Integrated Circuit Technology, pp.2008-2011, 2008.
[10] Jasdeep Kaur, Nupur Prakash and S.S. Rajput, "Low Voltage high Performance Self Cascode CCII." IEEE Proc. INMIC, pp.7-11, Dec 2008.
[11] Louis-Francois Tanguay, Mohamad Sawan and Yvon Sawaria, "A very High Output Impedance Current Mirror for very low Biomedical Analog Circuits." Asia-Pacific Conference on Circuits and Systems, pp.642-645, Nov 2008.
[12] Rohan Sehgal, "A 0.8V Operational Amplifier using Floating Gate MOS Technology." International Conference on Semiconductor Electronics, pp.795-799, Dec 2006.
[13] B.J. Blalock and P.E. Allen, "Low Voltage Bulk Driven MOSFET Current Mirror for CMOS Technology." IEEE ISCAS Vol.3, pp.1972-1975, 1995.
[14] T. Voo and C. Toumazau, "High speed Current Mirror resistive compensation technique," Electronic Letters, Vol. 31, pp. 248-250, Feb 1995.

AUTHORS

Anuj Dugaya received his B.E. degree in Electronics and Communication Engineering from the Rajiv Gandhi Technical University, Bhopal, India in 2010, and currently pursuimg M.Tech from Maulana Azad National Institute of Technology, Bhopal, India. His current area of interest includes low power analog circuits.

Laxmi Kumre received her B.Tech Degree in Electronics and Communication engineering in 1998, M.Tech Degree in Digital Communication in 2010 and currently pursuing Ph.D in Low Power Digital System Design. She is working as Senior Assistant Professor in D epartment of Electronics and Communication Engineering in MANIT, BHOPAL. Her field of Interest are Low Power Digital Circuit Design Techniques, VLSI Digital System design and Communication Systems. She is Fellow member of IEEE, INDIA.