DESIGN OF 6-BIT FLASH ANALOG TO DIGITAL CONVERTER USING VARIABLE SWITCHING VOLTAGE CMOS COMPARATOR

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ABSTRACT

This paper presents the design of 6-bit flash analog to digital Converter (ADC) using the new variable switching voltage (VSV) comparator. In general, Flash ADCs attain the highest conversion speed at the cost of high power consumption. By using the new VSV comparator, the designed 6-bit Flash ADC exhibits significant improvement in terms of power and speed of previously reported Flash ADCs. The simulation result shows that the converter consumes peak power 2.1 mW from a 1.2 V supply and achieves the speed of 1 GHz in a 65nm standard CMOS process. The measurement of maximum differential and integral nonlinearities (DNL and INL) of the Flash ADC are 0.3 LSB and 0.6 LSB respectively.

KEYWORDS

Variable switching voltage, threshold inverter quantization, comparator, Flash ADC.

1. INTRODUCTION

Analog-to-digital converter (ADC) has become essential structure for most of the electronics and communication systems. Comparator constitutes the main component in analog to digital conversion (ADC). It is basically the first stage in ADC, which converts the signal from analog to digital domain. The Flash ADC is the fastest ADC among all types of available ADC architectures. An N-Bit Flash ADC employs the 2^N-1 comparators for data conversion. However, these comparators consume large power as they work simultaneously in parallel fashion. The Flash ADC also requires resistor ladder circuit or capacitor array circuit for reference voltage generation [2], which again makes the converter more power hungry & therefore Flash ADC consumes highest power among all types of ADCs. For low power data conversion circuits, the power dissipation has become one of the most important limitations. In reality, power efficiency has been considered as an essential design criterion in many battery employed applications such as wireless sensor node, pacemakers and other implanted RFID chips as biomedical imaging devices in the human body [4]. The objective in such cases is minimum power consumption for maximum battery life time. The designed 6-Bit Flash ADC in this paper meets the requirement for such low power applications.

2. RELATED RESEARCH WORK

In order to minimize the power consumption and improve the performance matrices of ADC, the researches basically focus on the optimization of the comparator circuit. In this section, the

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research work under discussion contains only Flash ADC design using threshold voltage scaling of the comparator. In [5], a static inverter circuit has been explored as programmable logical buffer circuit and it has been suggested that the logic threshold voltage of CMOS inverter can be programmed to different specific logical voltages. These variable logical voltages can be evaluated mathematically. In [7], the thorough theoretical background of static CMOS inverter is elaborated. Using the aforementioned concept, a CMOS inverter has been realized as a threshold inverter quantization (TIQ) comparator [6]. The design of proposed TIQ comparator is a simpler as compared to traditional analog differential comparator. The basic thought is to simply apply the digital inverter as an analog voltage comparator. This also eliminates the resistive reference voltage circuit in Flash ADC. Thereby, static power consumption by resistive ladder circuit is removed. Inspired by the threshold voltage scaling, a reduced kickback comparator has been reported in literature [9]. Basically, it is a differential type of comparator, which can be designed with inbuilt threshold voltages. The design presented in [10] explored the TIQ comparator for 6-bit Flash ADC. It was basically implemented for system on chip (SOC) applications. The designed ADC was simpler and faster than other Flash ADCs. In this paper, the same research has been extended with the modified version of the comparator. The simulation results are better than the earlier reported works and the design 6-bit Flash ADC excels in terms of speed and power consumption.

3. COMPARATOR

The function of a comparator is to generate an output voltage, which is high or low depending on whether the amplitude of the input is greater or lesser than a reference signal. It produces a binary output whose value is based on a comparison of two analog inputs. Typical comparators have differential type of architecture, and they can be further divided into open-loop and dynamic comparators. The open-loop comparators are fundamentally operational amplifier [4]. Dynamic comparators use positive feedback similar to flip-flops to accomplish the comparison of the magnitude between input and the external reference signal. However these differential types of comparator are intrinsically complex in design and consume high amount of power. On the other hand, single ended comparator architecture may be deployed as an analog comparator instead of using a whole analog block of comparator. The threshold inverter quantization (TIQ) comparators have been used to design the Flash ADC. The TIQ inverter based comparator consists of two cascaded inverters as shown in figure 1.

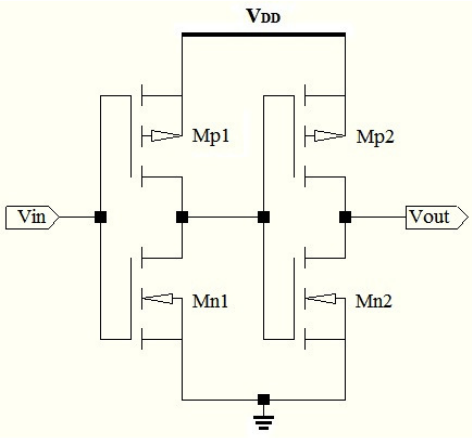

Figure 1. TIQ Comparator [6]

The inverter requires lesser number of transistors as compared to traditional comparator. In fact, a traditional comparator requires two input signal, while inverter based comparator requires only one input signal. The logic reference or switching voltage is generated by the inverter itself [5]. Graphically, the switching voltage can be identified at the intersection of the input voltage (Vin) and the output voltage (Vout) signal. At this point, both the transistor PMOS and NMOS are in the saturation region. By equating the drain current of devices, the switching threshold voltage can be determined. The mathematical formula for these switching voltages is given by the following equation [7].

$$V_{sv} = \frac{\left(V_{DD} - \lfloor V_{tp1} \rfloor\right)\sqrt{k\,\frac{w_p}{w_n}} + V_{tn1}}{\sqrt{k\frac{w_p}{w_n} + 1}} \tag{1}$$

Wherein, k denotes the mobility ratio of hole and electron, w_p & w_n are the channel width of PMOS (Mp1) & NMOS (Mn1) respectively, V_{tn1} & V_{tp1} are the threshold voltages of the devices Mn1 and Mp1 respectively. Further the equation can be simplified in terms of the channel width ratio of Mp1 and Mn1.

$$V_{sv} = \frac{\left(V_{DD} - \lfloor V_{tp1} \rfloor\right)\sqrt{k\,w_r} + V_{tn1}}{\sqrt{k\,w_r} + 1} \tag{2}$$

Where, w_r is the ratio of channel width of devices Mp1 and Mn1. While driving the equation of switching voltage, it has been assumed that both transistors PMOS & NMOS have the same channel length. The logic threshold voltage of a CMOS inverter is determined by the channel width ratio W_r of the PMOS and NMOS transistors. However at 65nm standard CMOS process, the switching voltage is not governed by the equation (2), it is due to the fact that short channel devices do not follow the square law relation and in such case, the switching voltage is controlled by effective resistance of the devices [8], it is therefore given by following equation.

$$V_{sv} = V_{DD}\frac{r_{mn1}}{r_{mn1} + r_{mp1}} \tag{3}$$

Where r_{mn1} and r_{mp1} are the effective switching resistances of NMOS (Mn1) and PMOS (Mp1) transistors of the first stage inverter at channel length (L) =65nm, respectively. The resistance r_{mn1} and r_{mp1} are the function aspect ratio (W/L) of the devices, thus the switching voltages can be programmed to specific values by varying the aspect ratio.

3.1. VARIABLE SWITCHING VOLTAGE COMPARATOR

The proposed variable switching voltage (VSV) comparator is shown in figure 2. The proposed comparator comprises eight numbers of transistors. However the number of transistor has been doubled as compared to traditional TIQ comparator. In spite of this, the proposed comparator consumes lesser power than the TIQ comparator. It is due to the fact that, the addition of M1 and M2 provides negative feedback in the comparator.

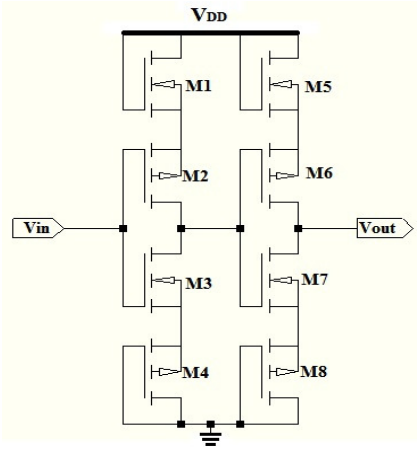

Figure 2. Proposed VSV Comparator

This causes reduction in the drain current of Mn1 and Mp1 of the first stage. This in turn decreases the power consumption of the first stage. The same remark is applied to the second stage of the comparator. In fact, the second stage provides sharper switching of the logical voltages and it is used to invert the output of the first stage. Note that the devices M1, M4, M5 and M8 are always in saturation because drain and gate terminals are at the same potential i.e. V_G=V_D. The saturated device offers an active resistance, which can be determined by its transconductance (g_m). For the NMOS device, it is given by the following equation.

$$g_m = \frac{\partial I_D}{\partial V_{gs}} = \sqrt{2\left(\frac{w}{L}\right)_n \mu_n C_{\mathrm{ox}} \mathrm{I_D}} \tag{4}$$

This can be further simplified in terms of the aspect ratio (A_{rn}) and process transconductance (k'_n) of NMOS device.

$$g_m = \sqrt{2A_{rn}k'_n \mathrm{I_D}} \tag{5}$$

Similarly for the PMOS device, the transconductance (g_m) may be given as.

$$g_m = \sqrt{2A_{rp}k'_p I_D} \tag{6}$$

The switching voltage of first stage of the proposed comparator can be evaluated in the same manner as in equation 3.

$$V_{sv} = V_{DD}\frac{\mathrm{r_{m3}} + \frac{1}{\mathrm{g_{m4}}}}{\frac{1}{\mathrm{g_{m1}}} + \mathrm{r_{m2}} + \mathrm{r_{m3}} + \frac{1}{\mathrm{g_{m4}}}} \tag{7}$$

Where $1/g_{m1}$ & $1/g_{m4}$ are the active resistance of M1 and M4 respectively, while r_{m2} & r_{m3} are the effective switching resistances of M2 and M3 transistors. Since the switching resistance of a transistor depends on its channel width, therefore the width of the devices M1, M2 and M3, M4 is varied to obtain the 63 different switching voltages as shown in figure 3.

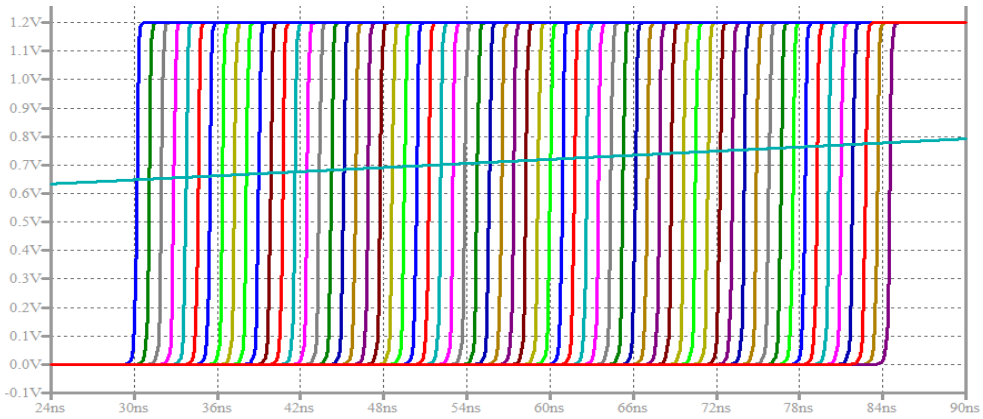

Figure 3. Switching voltages of 6-bit Flash ADC

Using the proposed comparator, a low-power 6-bit Flash ADC is designed and simulated. A comparative analysis is also presented to justify the power reduction in the proposed comparator.

3.2 Flash ADC

The generalized block diagram of N-bit Flash ADC is shown in the figure 4. A 6-bit Flash ADC requires 63 numbers of comparator at the input side of the block diagram. An analog input voltage (Vin) goes through each comparator, the comparators compare the input voltage with internal reference voltages, which are determined by the aspect ratio of CMOS transistors of VSV Comparator. These comparators work simultaneously. The comparator's output will be either '1' or '0' depending on internal reference voltage of the comparator.

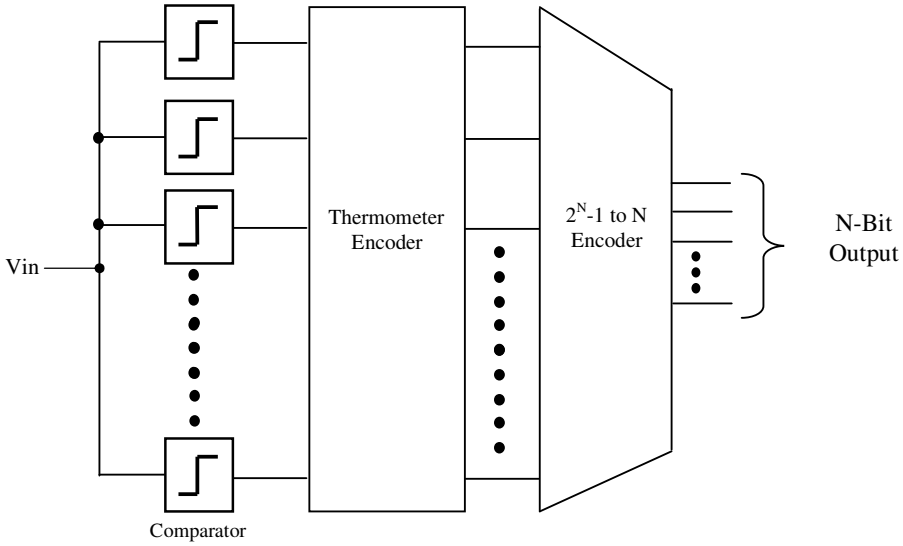

Figure 4. VSV comparator based Flash ADC Architecture

For 6-bit Flash ADC, the digital switching signals (thermometer codes) are produced by the array of 63 comparators. The thermometer codes are converted into intermediate codes to minimize the bubble error in the code. The output of the thermometer encoder is shown in figure 6.

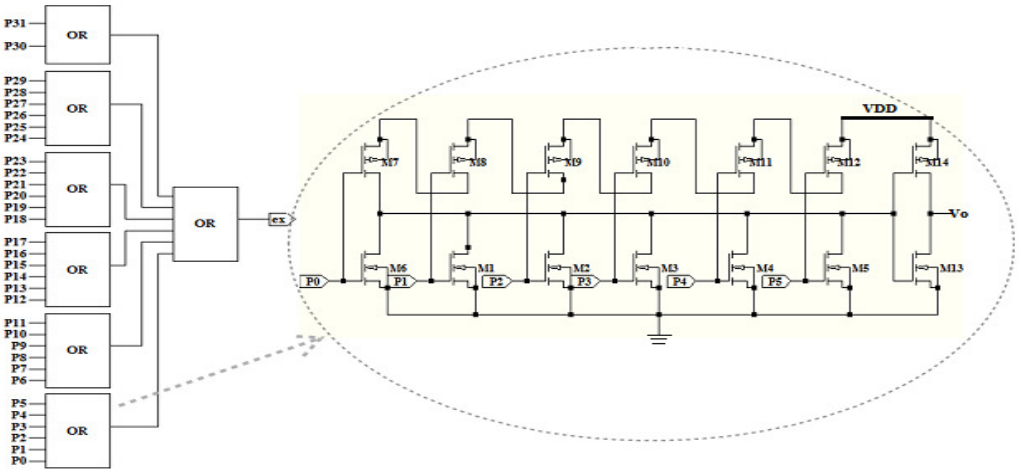

Figure 5. Second Stage Encoder

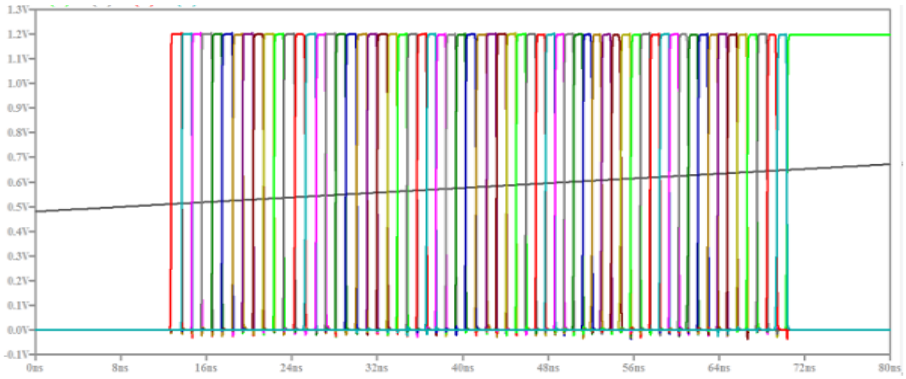

Figure 6. Waveform of 63 Intermediate codes

The intermediate codes are fed to 2^N-1 to N encoder block. The encoder performs second step of encoding as shown in figure 5. Basically, it encodes the single bit. There are as such 6 encoder blocks associated with each bit for performing the encoding process. Table 1 summarizes this final encoding process for all 6-bits.

Table 1. Encoder Input Combinations

Encoder Input	**Encoder Output**					
	E_5	**E_4**	**E_3**	**E_2**	**E_1**	**E_0**
P_0	I_{32}	I_{16}	I_8	I_4	I_2	I_1
P_1	I_{33}	I_{17}	I_9	I_5	I_3	I_3
P_2	I_{34}	I_{18}	I_{10}	I_6	I_6	I_5
P_3	I_{35}	I_{19}	I_{11}	I_7	I_7	I_7
P_4	I_{36}	I_{20}	I_{12}	I_{12}	I_{10}	I_9

P_5	I_{37}	I_{21}	I_{13}	I_{13}	I_{11}	I_{11}
P_6	I_{38}	I_{22}	I_{14}	I_{14}	I_{14}	I_{13}
P_7	I_{39}	I_{23}	I_{15}	I_{15}	I_{15}	I_{15}
P_8	I_{40}	I_{24}	I_{24}	I_{20}	I_{18}	I_{17}
P_9	I_{41}	I_{25}	I_{25}	I_{21}	I_{19}	I_{19}
P_{10}	I_{42}	I_{26}	I_{26}	I_{22}	I_{22}	I_{21}
P_{11}	I_{43}	I_{27}	I_{27}	I_{23}	I_{23}	I_{23}
P_{12}	I_{44}	I_{28}	I_{28}	I_{28}	I_{26}	I_{25}
P_{13}	I_{45}	I_{29}	I_{29}	I_{29}	I_{27}	I_{27}
P_{14}	I_{46}	I_{30}	I_{30}	I_{30}	I_{30}	I_{29}
P_{15}	I_{47}	I_{31}	I_{31}	I_{31}	I_{31}	I_{31}
P_{16}	I_{48}	I_{48}	I_{40}	I_{36}	I_{34}	I_{33}
P_{17}	I_{49}	I_{49}	I_{41}	I_{37}	I_{35}	I_{35}
P_{18}	I_{50}	I_{50}	I_{42}	I_{38}	I_{38}	I_{37}
P_{19}	I_{51}	I_{51}	I_{43}	I_{39}	I_{39}	I_{39}
P_{20}	I_{52}	I_{52}	I_{44}	I_{44}	I_{42}	I_{41}
P_{21}	I_{53}	I_{53}	I_{45}	I_{45}	I_{43}	I_{43}
P_{22}	I_{54}	I_{54}	I_{46}	I_{46}	I_{46}	I_{45}
P_{23}	I_{55}	I_{55}	I_{47}	I_{47}	I_{47}	I_{47}
P_{24}	I_{56}	I_{56}	I_{56}	I_{52}	I_{50}	I_{49}
P_{25}	I_{57}	I_{57}	I_{57}	I_{53}	I_{51}	I_{51}
P_{26}	I_{58}	I_{58}	I_{58}	I_{54}	I_{54}	I_{53}
P_{27}	I_{59}	I_{59}	I_{59}	I_{55}	I_{55}	I_{55}
P_{28}	I_{60}	I_{60}	I_{60}	I_{60}	I_{58}	I_{57}
P_{29}	I_{61}	I_{61}	I_{61}	I_{61}	I_{59}	I_{59}
P_{30}	I_{62}	I_{62}	I_{62}	I_{62}	I_{62}	I_{61}
P_{31}	I_{63}	I_{63}	I_{63}	I_{63}	I_{63}	I_{63}

In the conventional Flash ADC, all the comparators are identical and reference voltages are generated by resistor ladder circuit. On the other hand, In the VSV comparator based Flash ADC, the desired internal reference voltage is generated by comparator itself just like TIQ comparator based Flash ADC. Therefore 2^N-1 different sizes of comparators are needed for generation of 2^N-1 reference voltages and resistor ladder network is not required for the external reference voltage generation.

4. RESULTS & DISCUSSION

The proposed comparator has been simulated at 65nm standard CMOS process with the supply voltage of 1.2V. The power is measured & compared for both TIQ comparator [6] and proposed VSV comparator. It has been observed that the peak power for proposed VSV comparator is 96.37μW & its average power is only 2.144μW. While reported TIQ comparator [6] consumes peak power of 380μW and its average power is 26.407 μW. There is almost 70% reduction in the peak power. This is highly desirable for low power application of data conversion circuits.

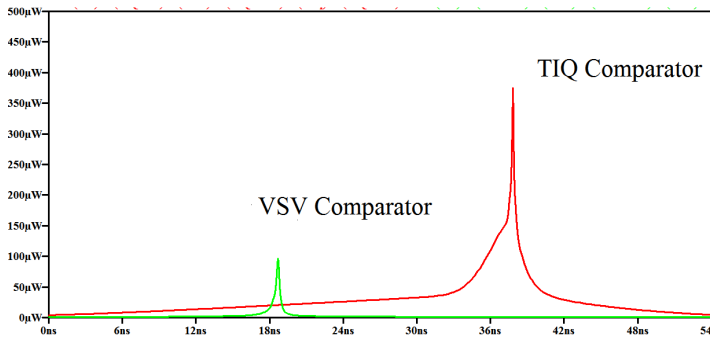

Figure 7. Power comparison of VTV comparator & TIQ comparator

The comparison of power consumption between TIQ comparator and proposed VSV comparator is shown in figure 7. For 6-bit Flash ADC, the power consumption of TIQ comparator array and proposed VSV comparator array are shown in figure 9 and 10 respectively.

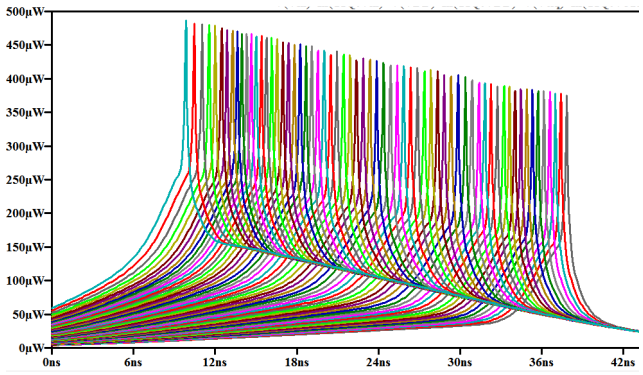

Figure 8. Power consumption of TIQ comparators array

Using the proposed comparator, a 6-Bit Flash ADC has been designed and simulated at 65nm standard CMOS process. The design is simpler than the conventional Flash ADC and it does not require the resistive ladder for reference voltage generation.

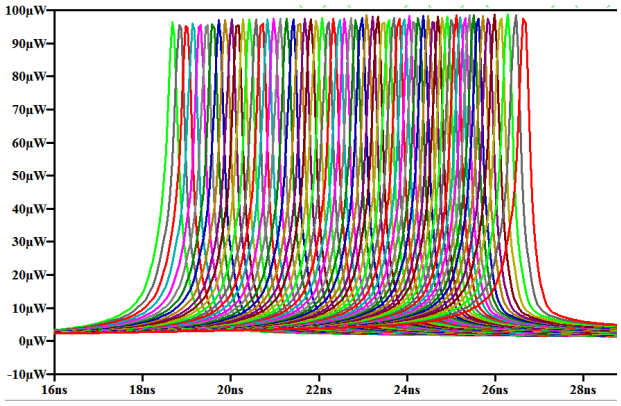

Figure 9. Power consumption of proposed VSV comparators array

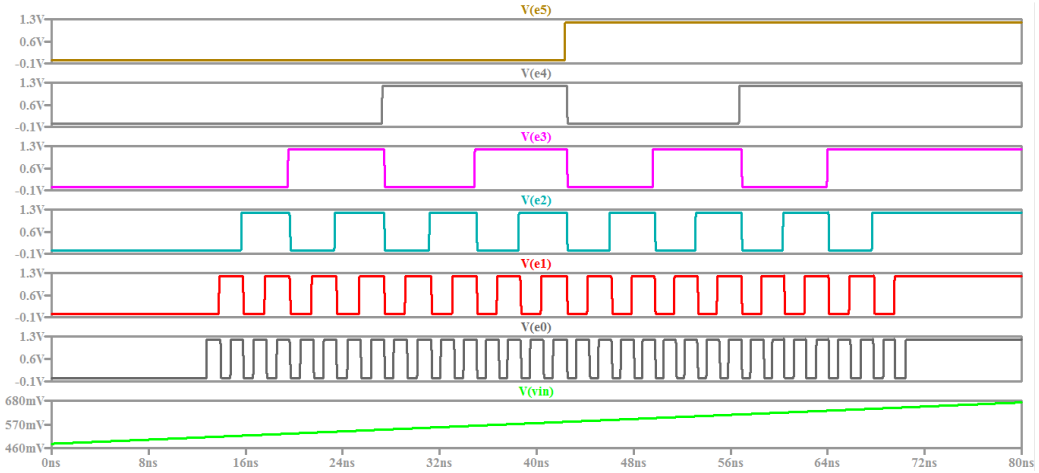

Figure 10. Transient analysis of the 6-bit Flash ADC

The transient analysis of the ADC is made by giving a ramp input signal ranging from 562mV to 680 mV and each LSB voltage level is of 2.1mV. The digital codes are obtained correctly for 6-bit ADC as shown in figure 10. The plot of the measured differential nonlinearity (DNL) for the designed ADC is shown in figure 11.

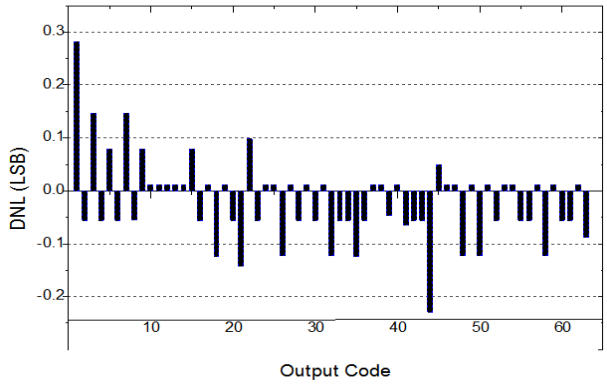

Figure 11.Measurement of DNL of the 6-Bit Flash ADC

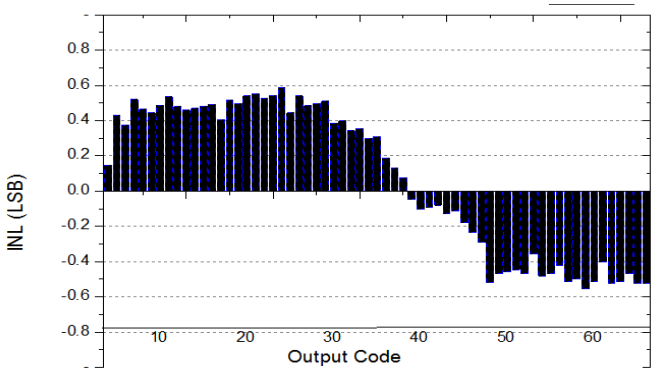

Figure 12. Measurement of INL of the 6-Bit Flash ADC

The measurement of integral nonlinearity (INL) is drawn in the figure 12. It is clear from the plot that, the measured INL is lesser than 0.6 LSB. This shows functional correctness of the designed 6-bit Flash ADC

Table 2. Comparison Summary of Simulation Results

Parameter	Proposed work	Reported work [1]	Reported work [2]	Reported work [3]	Reported work [10]
Resolution	6-bit	6-bit	6-bit	6-bit	6-bit
Architecture	Flash	Flash	Flash	Flash	Flash
Technology	65 nm	90 nm	130 nm	65 nm	250 nm
DNL (LSB)	0.3	0.5	0.4	0.5	--
INL (LSB)	0.6	0.96	0.6	0.5	--
Voltage Supply	1.2 V	0.9 V	1.2 V	1.2 V	2.5 V
Power Dissipation	2.1 mW	98 mW	90 mW	12 mW	66.8 mW
Samples/sec.	1G	3.5G	600M	800M	1G
Ladder Network	No	Yes	Yes	Yes	No

The different parameters obtained for 6-bit Flash ADC are compared with earlier reported work in Table 2. For transparent comparison, only Flash ADC architectures of 6-bit resolution have been selected. It can be observed from the above table that the proposed comparator based Flash ADC consume the lowest power at the speed of 1 GHz. The measured DNL and INL are also lesser than 1 LSB. This guarantees that, the designed 6-bit flash ADC is monotonic in nature.

5. CONCLUSION

A 6-bit Flash ADC has been designed by employing the proposed VSV comparator. The design has been carried out in digital 65nm standard CMOS technology. Further lower feature size and smaller supply voltage can be incorporated in the design. At 1 GHz speed, the Flash ADC dissipates peak power of 2.1mW and average power of only 244μW. The measured maximum differential and integral nonlinearities (DNL and INL) for a ramp input are found to be 0.3 LSB & 0.6 LSB respectively. The parameters DNL & INL are improved as compared to earlier reported works. The designed 6-bit Flash ADC exhibits significant improvement in terms of power and speed of previously reported Flash ADCs. This makes it highly suitable ADC for high speed and low power application.

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