DESIGN OF A NOVEL CURRENT BALANCED VOLTAGE CONTROLLED DELAY ELEMENT

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ABSTRACT

This paper presents a design of fast voltage controlled delay element based on modified version of low noise Current Balanced Logic (CBL). This delay element provides identical rising and falling edge delays controlled by the single control voltage. The post layout tunable delay range is from 140 ps to 800 ps over control voltage range of 0 to 2.1 V. An analysis for the delay element is also presented, which is in agreement with the simulated delays. A Delay Lock Loop (DLL) is designed using this delay element to verify its performance.

KEYWORDS

Current Balanced Logic (CBL), Source Coupled Logic (SCL), Current Starved Inverter (CSI), Delay Lock Loop (DLL), Phase Lock Loop (PLL)

1. INTRODUCTION

Delay Element (DE) is a vital block in Delay Lock Loop (DLL) [1], Phase Lock Loop (PLL) [2], microprocessor and memory circuits [3] and Time-to-Digital Converters [4]. The aim is to design a delay element, which assists in time interval (TI) measurement [4] with high resolution (< 200 ps) for High Energy Physics (HEP) experiments. A variety of DEs already has been reported in the literature [5] with their merits and limitations. The Current Starved Inverter (CSI) is used as a delay element in time measurement circuits. This structure ensures wide delay regulation range and low power consumption. The reported delay using CSI is 244 ps [6] in 0.35 µm CMOS process.

Transmission gate based delay element [5] is fast due to relatively low resistive path between input and output. It is power and area efficient and has full swing output. However, the delay increases quadratically with the number of cascaded transmission gates [7]. Differential DE based on low noise Source Coupled Logic (SCL) [8] [9] [10] mitigates the common mode noise, which is prevalent in CSI. They are fast but have partial output swing and are power inefficient due to the high static current. In addition, they require a complex bias circuitry for delay variation.

This paper presents a design of voltage controlled delay element based on modified version of Current Balanced Logic (CBL) [11] and is referred here as Modified CBL (MCBL) delay element. The salient features of this delay element are identical delays in the rising and falling edge transitions, high speed, area efficient, less contribution in the generation of 'di/dt' switching noise and low power consumption as compared to other architectures of differential delay elements.

The paper is organized in the following sections: In section 2, an overview of current balanced logic and architecture of MCBL DE is presented. A detailed analysis of the circuit is also provided. The simulation results are compared with the analytical results. In section 3, a design of

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Delay Lock Loop (DLL) has been presented using MCBL delay element. In Section 4, post layout simulation results are presented. In section 5, conclusions are drawn.

2. CURRENT BALANCED LOGIC (CBL)

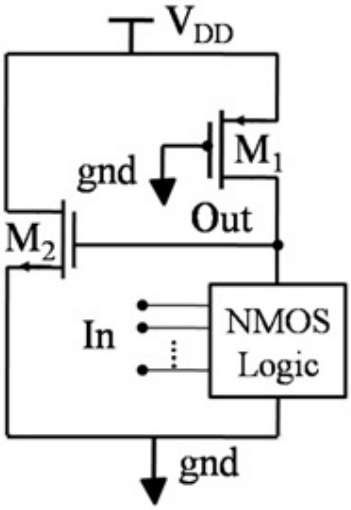

Figure 1. Current Balanced Logic Circuit

Current Balanced Logic (CBL) [10] is the low noise logic family that reduces 'di/dt' switching noise. The noise reduction technique aims to keep the supply current steady. This scheme modifies pseudo NMOS logic by adding the NMOS transistor 'M_2' as shown in Figure 1. When NMOS logic block is on, the output node 'Out' is pulled down, which keeps M_2 in cut-off operating region and there is a static supply current through M_1. When NMOS logic block is off, M_2 is in saturation and draws the same supply current assuming M_1 and M_2 are well matched.

2.1. Architecture of MCBL delay element

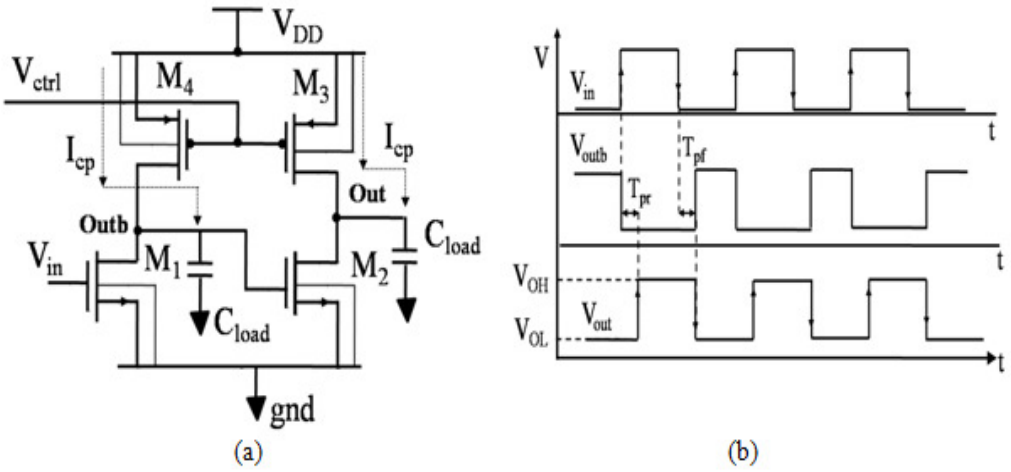

Figure 2. MCBL Delay element (a) Schematic Diagram (b) Timing Diagram

Figure 2 represents the schematic and timing diagram of MCBL delay element. The amount of charging current 'I_{cp}' through PMOS transistors 'M_3' and 'M_4' controls the rising and falling edge propagation delays respectively. The current 'I_{cp}' is determined by the control voltage 'V_{ctrl}'. Both rising 'T_{pr}' and falling 'T_{pf}' edge delays are identical as PMOS 'M_3' and 'M_4' as well as NMOS 'M_1' and 'M_2' are matched transistors, the nodes 'Out' and 'Outb' face the same capacitive load (C_{load}).

As shown in Figure 2(b), when rising edge transition of 'V_{in}' clock is applied, the 'Outb' node pulls down. The NMOS transistor M_2 enters in the cut-off region and PMOS 'M_3' starts pulling up the node 'Out' by charging the load capacitance 'C_{load}' using 'I_{cp}'. When falling edge transition of V_{in} is applied, 'M_1' is turned off. Subsequently 'M_4' starts pulling up the node 'Outb'. This turns on 'M_2', which pulls down the node 'Out'. The pull down is fast as aspect ratio 'W/L' of NMOS is designed to be higher than PMOS transistors. The signals V_{in} and V_{out} are of same polarity with identical rising 'T_{pr}' and falling 'T_{pf}' edge delays. The variation in the supply current is small as equal current path is maintained in rising and falling edge transitions. This ensures the current balancing.

This MCBL DE can be interfaced to the standard cells available in the PDK (Process Design Kit) owing to its large output swing. It is fast as compared to CSI, shown in Figure 3, as the resistance of charging path of capacitive load 'C_{load}' is less. There is only one transistor 'M_3' in the charging path for MCBL while in CSI, there are two series connected transistors M_7 and M_8. In the cascaded delay line, the MCBL DE faces a single transistor (M_1) load (gate capacitance) as compared to two transistors (M_6 and M_7) load in CSI. This further reduces the propagation delay of MCBL DE. The static current is small as compared to differential delay elements. Further, this DE has wide delay tuning range with respect to control voltage.

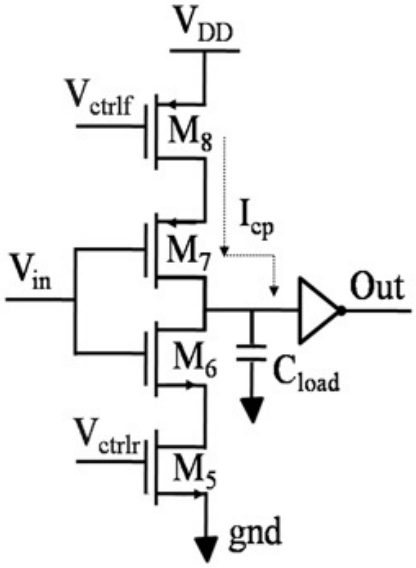

Figure 3. Schematic Diagram of CSI

2.2. Analysis of the MCBL delay element

This section describes the equation for propagation delay as well as output voltages V_{OL} (maximum output voltage in logic '0') and V_{OH} (minimum output voltage in logic '1').

2.2.1. Calculation of V_{OL} and V_{OH}

To ensure the compatibility of DE to be interfaced with the standard cells, it is required to calculate V_{OL} and V_{OH} over a control voltage range. In the calculation of V_{OL}, it is assumed that V_{in} is less than the threshold voltage 'V_{tn}' of M_1 ($V_{in} < V_{tn}$) (Figure 2(a)). The NMOS transistor M_1 is turned off and subsequently M_2 is turned on. There is a static current through M_3 and M_2. The expression of V_{OL} is derived by applying KCL at node 'Out':

$$I_{M3(saturation)} = I_{M2(linear)} \quad (1)$$

$$\frac{1}{2}(\mu_p)(C_{ox})\left(\frac{W}{L}\right)_{M3}\left(V_{ctrl} - V_{DD} - V_{tp}\right)^2 = (\mu_n)(C_{ox})\left(\frac{W}{L}\right)_{M2}\left((V_{DD} - V_{tn})V_{out} - \frac{{V_{out}}^2}{2}\right) \quad (2)$$

where, μ_n and μ_p are the mobility of electrons and holes in cm^2/Volt-sec, C_{ox} is oxide capacitance per unit area, W/L is aspect ratio of transistors, and V_{tn} and V_{tp} are threshold voltage of NMOS and PMOS transistors respectively. On simplification, equation (2) can be written as-

$$A\left(V_{ctrl} - V_{DD} - V_{tp}\right)^2 = 2(V_{DD} - V_{tn})V_{out} - {V_{out}}^2 \quad (3)$$

Where, $A = \frac{\mu_p\left(\frac{W}{L}\right)_{M3}}{\mu_n\left(\frac{W}{L}\right)_{M2}}$

On simplifying, we get a quadratic equation (4) in terms of V_{out}:

$${V_{out}}^2 - 2V_{out}(V_{DD} - V_{tn}) + A\left(V_{ctrl} - V_{DD} - V_{tp}\right)^2 = 0 \quad (4)$$

The roots of quadratic equation $ax^2+bx+c=0$ are given by:

$$x = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \quad (5)$$

Equating the corresponding coefficients of equation (4) and (5) we get:

$$V_{out} = [V_{DD} - V_{tn} \pm S] \quad \text{Where, } S = \sqrt{(V_{DD} - V_{tn})^2 - A\,(V_{ctrl} - V_{DD} - V_{tp})^2}$$

Expression for V_{OL} is given with negative root of above quadratic equation as value of V_{OL} should be in between 0 to V_{DD}.

$$V_{out} = V_{OL} = V_{DD} - V_{tn} - S \quad (6)$$

V_{OL} is designed to be low by keeping the aspect ratio of NMOS transistors (M_1 and M_2) higher than PMOS transistors (M_3 and M_4). To calculate V_{OH}, the assumption is $V_{in} > V_{tn}$. Consequently 'M_2' is turned off so that $I_{M2} = 0$. By applying KCL at node 'Out', we get:

$$I_{M3} = I_{M2} = 0$$

$$\Rightarrow \frac{K_p W}{2L}\left\{2\left(V_{ctrl} - V_{DD} - V_{tp}\right)(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2\right\} = 0 \quad (7)$$

The only valid solution of equation (7) is $V_{out} = V_{OH} = V_{DD}$. In order to verify the analytical equations for V_{OL}, technological and operating parameters, as shown in Table (1) are used. Figure 4 (a) shows the comparison of simulated and analytical data for V_{OL} over the control voltage 'V_{ctrl}'. The maximum deviation is 20 mV. The values of V_{OL} over the entire range of control voltage are small. Therefore, they can be interfaced with the standard cells in the design of DL

2.2.2 Propagation Delay equation

The aim is to find the rising edge propagation delay 'T_{pr}' (Figure 2(b)) of the circuit with respect to control voltage 'V_{ctrl}'. When V_{in} is at logic '1', V_{outb} pulls down to V_{OL}. Consequently, the NMOS transistor M_2 enters in the cut-off region. In the calculation explained below, it is assumed that M_2 enters in cut-off after a constant delay. It is not modeled to avoid the complexity in the calculation. Assuming negligible current through M_2, the current 'I_{cp}' through M_3 is used to charge the load capacitance 'C_{load}'. The relation between the current 'I_{cp}' and delay 'T_{pr}' is given by equation (8).

$$T_{pr} = C_{load} \int_{V_{OL}}^{V_{DD}/2} \frac{dV_{out}}{I_{cp}(V_{out})} \tag{8}$$

The channel length 'L' of PMOS transistor M_3 is designed to be 0.35 µm. The value of V_{DSAT} is 1.7 V in 0.35 µm AMS CMOS process. It is a good approximation to assume velocity saturated behavior from V_{OL} to $V_{DD}/2$. The current I_{cp} in velocity saturation operating region is given by equation (9), where K_p is the gain factor for PMOS transistor and λ is channel length modulation factor.

$$I_{cp} = I_{sd} = -I_{ds} = -\frac{K_p}{2}\left(V_{ctrl} - V_{DD} - V_{tp}\right)(1 + \lambda\,(\mathrm{V_{out}} - \mathrm{V_{DD}}))$$

$$= \frac{K_p}{2}\left(V_{DD} - V_{ctrl} + V_{tp}\right)(1 + \lambda\,(\mathrm{V_{out}} - \mathrm{V_{DD}}) \tag{9}$$

This equation holds for the transition time of 'Out' node when it attains the voltage $V_{DD}/2$. Substituting this value of current in (8):

$$T_{pr} = \frac{2\times C_{load}}{K_p} \int_{V_{OL}}^{V_{DD}/2} \frac{dV_{out}}{(V_{DD} - V_{ctrl} + V_{tp})(1+\lambda\,(V_{out} - V_{DD}))}$$

$$T_{pr} = \frac{2\times C_{load}}{K_p \times (V_{DD} - V_{ctrl} + V_{tp})} \int_{V_{OL}}^{V_{DD}/2} \frac{dV_{out}}{(1+\lambda\,(V_{out} - V_{DD}))}$$

$$T_{pr} = K_1\,[\ln(1 + \lambda\,(V_{out} - V_{DD})]_{V_{OL}}^{V_{DD}/2} \quad \text{Where, } K_1 = \frac{2\times C_{load}}{\lambda K_p (V_{DD} - V_{ctrl} + V_{tp})}$$

$$T_{pr} = K_1\, ln[\frac{\left(1+\lambda\left(\frac{V_{DD}}{2} - V_{DD}\right)\right)}{(1+\lambda(V_{OL} - V_{DD}))}] \tag{10}$$

Figure 4(b) shows the comparison of simulated and analytical data for delay T_{pr} over control voltage. There is sufficient matching in the analytical and simulated data for usable range of control voltage from 0 V to 2.1 V.

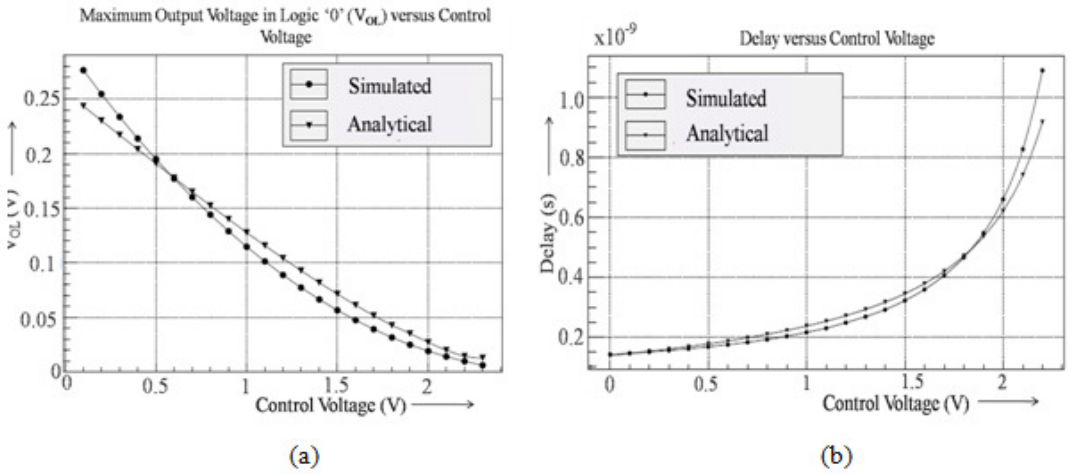

Figure 4. (a) V_{OL} versus Control Voltage (b) Delay versus Control Voltage of MCBL delay element for simulated and analytical model

Table 1. Parameters and their values

μ_n = 475E-4 m^2/V-Sec	μ_p = 148E-4 m^2/V-Sec
V_{tn}= 0.5V	V_{tp} = -0.69V
C_{ox} =4.4fF/μm^2	V_{DD} = 3.3V
T=27^{0}C=300K	K_p= 0.000651.2 F/V-sec
λ = 0.13V^{-1}	C_{load} = 14 fF
$(W/L)_{M3}=(W/L)_{M4}$=1µ/0.35µ	$(W/L)_{M1}=(W/L)_{M2}$=1.5 µ/0.35µ

3. DESIGN OF DLL USING THE MCBL DELAY ELEMENT

In this section, the functionality of MCBL delay element has been verified by realizing a DLL. The block diagram of DLL is shown in Figure 5 (a), where the designed key building blocks are Voltage Controlled Delay Line (VCDL), bias circuit, Phase Detector (PD), Charge Pump (CP), loop filter capacitor (16 pF) and start control circuit.

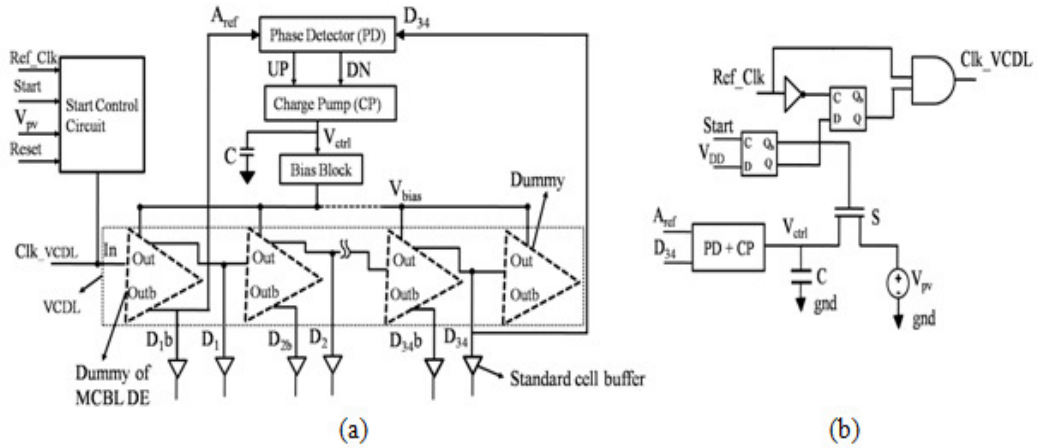

Figure 5. (a) Block diagram of DLL (b) Schematic diagram of start control circuit

The VCDL is realised by N cascaded MCBL delay elements. The number N = 33 is calculated using equation (11), where, T_{ref} = 10 ns is the reference clock period and T_d = 150 ps is unit target delay. The delay elements are loaded with standard cell buffers. To provide the identical load environment, two dummy delay elements at the beginning and end of VCDL are used.

$$N = \frac{T_{ref}}{2 \times T_d} \tag{11}$$

The start control circuit shown in Figure 5(b) is designed to avoid false harmonic locking of DLL. It sets the initial voltage 'V_{pv}' (preset voltage) of loop filter capacitor before the commencement of locking process. Initially, the preset switch 'S' is on. It sets the voltage across loop filter capacitor 'C' to the voltage 'V_{pv}' = 0.5 V for unit delay of 170 ps. The value of 'V_{pv}' is deduced from delay characteristic of DE with bias circuit as shown in Figure 7(b).The bias circuit shown in Figure 6(a) modifies delay versus control voltage characteristic. It improves the range of control voltage and makes the delay a monotonic function with respect to control voltage.

The operation of DLL starts with the assertion of 'Start' signal. It turns off the preset switch 'S' and enables the reference clock 'Ref_Clk' inside VCDL. The delayed output clock 'D_{34}' from VCDL is applied to PD shown in Figure 6(b), where its rising edge is compared with the rising edge of reference clock A_{ref} (Figure 5(a)). The PD converts the phase error into equivalent time duration pulse 'UP' and 'DN'. The output of PD controls the charge pump [12]. If phase error is positive, the time duration error is given by UP signal, which controls the discharging of filter capacitor. If phase error is negative, it is given by DN signal, which controls the charging of filter capacitor. For the applied V_{pv}, the control voltage 'V_{ctrl}' decreases by the correction of loop and stabilizes at 0.3 V for unit delay of 150 ps as shown in Figure 8(a). After iterations of 20 clock cycles, the DLL locks the delay of VCDL to half clock period (5 ns) of reference clock.

The advantage of this delay element is that, only one control loop (including PD, charge pump, filter capacitor, and bias circuit) is required to control both rising and falling edge delays. The output of VCDL provides delayed replicas 'D_1' to 'D_{34}' of Clk_VCDL with time interval of 150 ps.

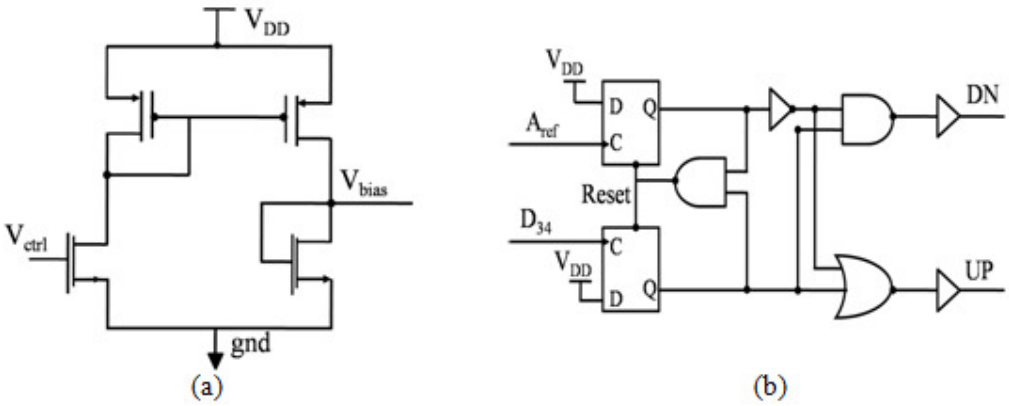

Figure 6. Schematic Diagram of (a) Bias Circuit (b) Phase Detector

4. SIMULATION RESULTS

The MCBL delay element is implemented using 0.35 µm CMOS technology. The results presented in this section are based on post layout simulation by Spectre using device models of standard CMOS process. The area of unit delay cell is 10×10 μm^2. The static current of single DE is 140 µA at 0.5 V control voltage. The static current reduces with the increment in control voltage.

A linear sweep of control voltage in the range of 0 V to 3.3 V with a step size of 0.1 V is applied to bias circuit. Figure 7(a) shows the bias voltage over the range of control voltage from 0 V to 3.3 V. The bias voltages applied to delay element causes identical variation in rising and falling edge delays of delay element. Figure 7(b) shows the plot of delay versus control voltage on typical corner.

The transient response of control voltage on typical corner is shown in Figure 8(a). Figure 8(b) depicts the consecutive uniformly delayed replicas of clock D_1 to D_9 generated from VCDL. In Table 2, the performance of delay element is compared with the other existing architectures in 0.35µm CMOS technology.

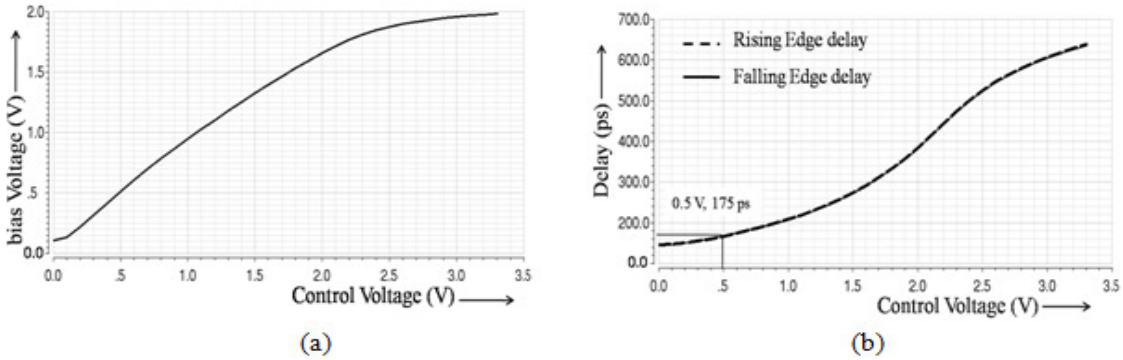

Figure 7. (a) Bias voltage (V_{bias}) with respect to control voltage (b) Delay with respect to control voltage

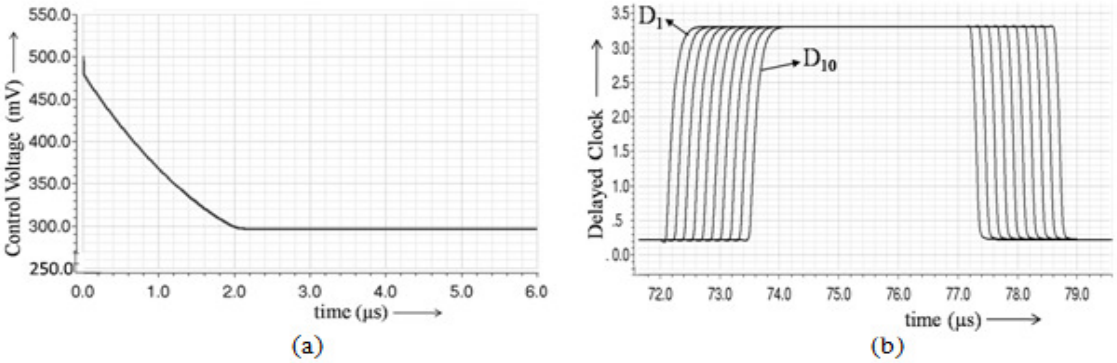

Figure 8. (a) Profile of Control Voltage 'V_{ctrl}' of DLL (b) Delayed clocks generated from VCDL

Table 2. Performance Comparison

DE	**This Work**	**[6]**	**[8]**	**[10]**
Type	MCBL with bias circuit	Current Starved INV	Differential	Differential (SCL)
T_{min} (ps)	140	244	2500	29.3
T_{max} (ps)	680	----	16000	----
Power with DLL	25 mW @ 100 MHz	14 mW @ 32 MHz	132 mW @130 MHz	675mW @ 3 V (without DLL)
N	33	128	10	64
Swing	Full	Full	Partial	Partial
Process	0.35 µm	0.35 µm	0.35 µm	0.35 µm

5. CONCLUSION

In this paper, a MCBL delay element and its analysis is presented. The analytical delays sufficiently match with the simulated ones. This delay element attains small propagation delays 147 ps with large swing and relatively low static current (140 μA @ 0.5 V). It provides identical rising and falling edge delays, which enables us to control both delays with a single control loop. This DE can be interfaced with the standard cells as the maximum value of V_{OL} is 0.25 V at 0.1 V control voltage. This delay element has potential to be incorporated in the mixed signal design due to MCBL logic.

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