IMPACT OF PARAMETER VARIATIONS AND OPTIMIZATION ON DG-PNIN TUNNEL FET

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ABSTRACT

The downscaling of conventional MOSFETs has come to its fundamental limits. TFETs are very attractive devices for low power applications because of their low off-current and potential for smaller sub threshold slope. In this paper, the impact of various parameter variations on the performance of a DG-PNIN Tunnel field effect transistor is investigated. In this work, variations in gate oxide material, source doping, channel doping, drain doping, pocket doping and body thickness are studied and all these parameters are optimized as performance boosters to give better current characteristics parameters. After optimization with all these performance boosters, the device has shown improved performance with increased on-current and reduced threshold voltage and the I_{on}/I_{off} *ratio is >* 10^6.

KEYWORDS

Tunnel Field Effect Transistor (TFET), Band to Band Tunneling (BTBT), DG-PIN TFET, DG-PNIN TFET, I_{on}/I_{off} *Ratio*

1. INTRODUCTION

Since the invention of transistor at Bell labs, the semiconductor industry has been witnessed a record growth in terms of revenue and transistor count on a chip with the trend following the well known Moore's law [1]. With each generation of scaled technology, the transistor performance has been improved. But, the aggressive scaling of MOSFET to meet various design constraints like low power consumption, smaller area, higher speed etc. is approaching to its fundamental limits [2-3]. To replace conventional MOSFET, new device structures are being investigated which must be compatible to CMOS circuit architecture and technology. Due to their low sub threshold swing (SS<60mv/dec), less susceptibility to short channel effects (SCEs), very low leakage current, Tunnel Field Effect Transistor (TFET) has been considered as an alternative for low power CMOS applications[4-12].

However the main disadvantage of TFET is, its low on-current. Therefore many TFET performance enhancing solutions have been proposed to enhance on-current such as 1) Modification of the TFET architecture (Like Hetero structures [13-15], Strained Silicon [16], High-k gate dielectric [17-18]), 2) Use of small band gap materials at tunnel junction to reduce the tunneling height [19-23]), 3) Use of a pocket at source channel tunnel junction to reduce the tunneling width[24] etc. All these ideas are considered as performance boosters but, all of these performance boosters are often applied independently. Therefore, in consideration to achieve better current characteristics of TFET, as many as possible performance boosters should be applied to the device.

Tunnel FETs are gated reverse biased PIN diodes, where the gate is used to modulate an effective tunneling barrier height. The injection mechanism of Tunnel FETs is based on band to band tunneling (BTBT). To switch the device on, the diode is reverse biased and a voltage is applied to

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the gate. When device is off, there will be a large tunnel barrier between the bands. Hence, charge carriers will not tunnel from valence band to conduction band and a very small off-current will flow. When the device is on, the bands are pushed down towards each other and current flows.

In this work, a double gate PNIN Tunnel field effect transistor (DG-PNIN-TFET) device is designed and the impact of various parameter variations (like gate oxide material, doping, and body thickness variations) has been investigated. Now based on the variation analyses, the device parameters are optimized in order to work as performance boosters. After that, all these performance boosters are applied to the device to get superior current characteristics.

2. DEVICE STRUCTURE AND SIMULATION PARAMETERS

By increasing the doping level of some part of channel region near the source region, electric field can be increased. This small region is known as pocket and the device is called pocket doped TFET [24]. In this paper, an n-type pocket layer is used near the p+ heavily doped source region. The intrinsic region is lightly doped and drain region is n+ heavily doped. This device can be also termed as PNIN TFET device. Fig.1 shows the basic device structure of double gate PNIN (DG-PNIN) TFET. In this paper, double gate structure will be used due to better gate control provided by both gates.

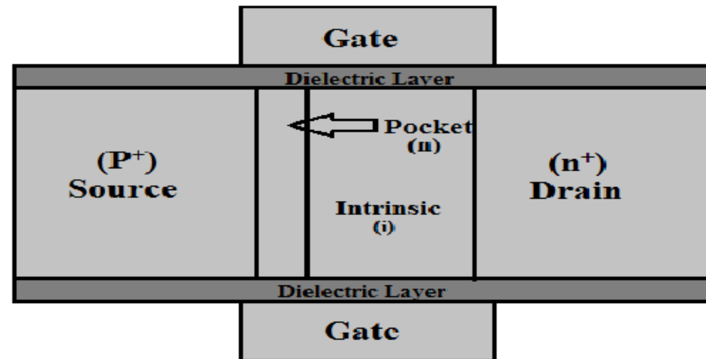

Figure 1. DG-PNIN-TFET Device Structure

The fundamental device parameters used for the device simulations are listed in table 1. All simulations are performed using SILVACO ATLAS with nonlocal BTBT model, Shockley Read Hall (SRH) and Fermi Dirac models [25] at room temperature with V_{gs}=1V.

Table 1. Parameters used in the simulation of the TFET

No.	Parameter	Value
1	Gate Oxide Thickness (t_{ox})	3nm
2	Silicon Body Thickness (t_{Body})	15nm
3	Gate Length (L_g)	60nm
4	Gate Work Function	4.0ev
5	Channel Doping ($N_{channel}$)	10^{17} atoms/cm^3
6	Source Doping (p^+) and Drain Doping (n^+)	10^{20} atoms/cm^3
7	Pocket Doping (N_{pocket})	10^{19} atoms/cm^3
8	Pocket Length (L_{pocket})	10nm
9	Gate Source Overlap (L_{ov})	5nm

A comparison graph of I_{ds}-V_{gs} characteristics of various TFET topologies like SG-PIN, SG-PNIN, DG-PIN and DG-PNIN TFET is presented in Fig. 2 and from the graph it can be seen that

for PNIN-TFET device, on current is higher than the PIN -TFET device. The impact of double gate with improved performance can also be seen in the graph. All these devices are simulated with parameters listed in table 1 and SiO_2 layer is used as gate oxide material.

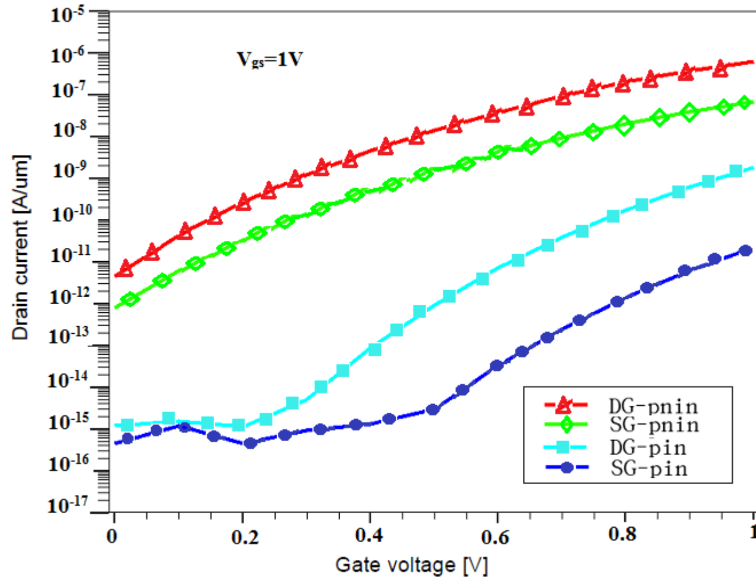

Figure 2. Comparison of I_{ds}-V_{gs} characteristics of DG-PNIN, DG-PIN, SG-PNIN and SG-PIN TFET

3. Impact of Parameter Variations

In this section the impact of various parameter variations on DG-PNIN TFET device is studied and investigated.

3.1. Gate Oxide Material Variations

Effect of gate oxide material on the performance of DG-PNIN TFET is evaluated and the materials that have been analyzed are SiO_2, Si_3N_4 and HfO_2 whose dielectric constant is 3.9, 7and 25 respectively. Fig.3 shows the Id-V_{gs} characteristics of the PNIN TFET device with different gate oxide material. From the figure, it is clear that by using high-k gate oxide dielectric layer (i.e. HfO_2) the on-current is increased due to better gate coupling provided by the high-k dielectric. With high-k dielectric, the Off-current is also increased but it is acceptable because it's still very low. So for all the further simulations HfO_2 layer will be used as a gate oxide for better performance.

3.2. Doping Variations

The doping levels of the Tunnel FET device must be carefully optimized in order to maximize on current and I_{on}/I_{off} ratio and minimize off-current. In DG-PNIN TFET, there are four types of doping level and these are source, drain, intrinsic and pocket doping levels. When doping level increases, the band gap reduces. With the reduction in band gap, current characteristics parameters of the device will improve. Here, by using this fact, these doping levels are studied and investigated.

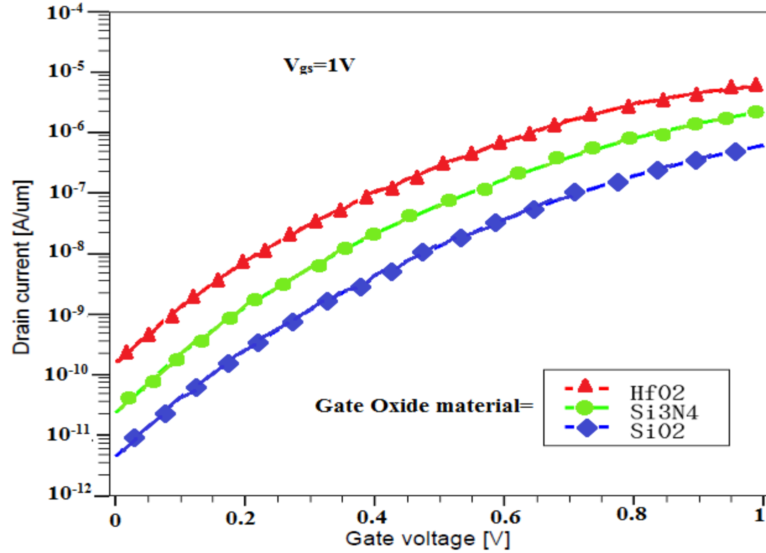

Figure 3. I_{ds}-V_{gs} characteristics of DG-PNIN TFET with varying gate oxide materials

3.2.1 Source Doping Variations

In TFET tunneling takes place between source and intrinsic region therefore, source doping (N_s) has a great effect on that tunneling phenomenon. The PNIN TFET device is simulated at various source doping levels such as $1*10^{20}$, $1.5*10^{20}$ and $2*10^{20}$. Fig. 4 shows, the comparison graph of I_d-V_{gs} characteristics of DG-PNIN TFET device with varying source doping. As source doping increases, on-current also increases due to electric field enhancement at tunneling junction. Thus, the highest feasible source doping is preferable for DG-PNIN TFET optimization.

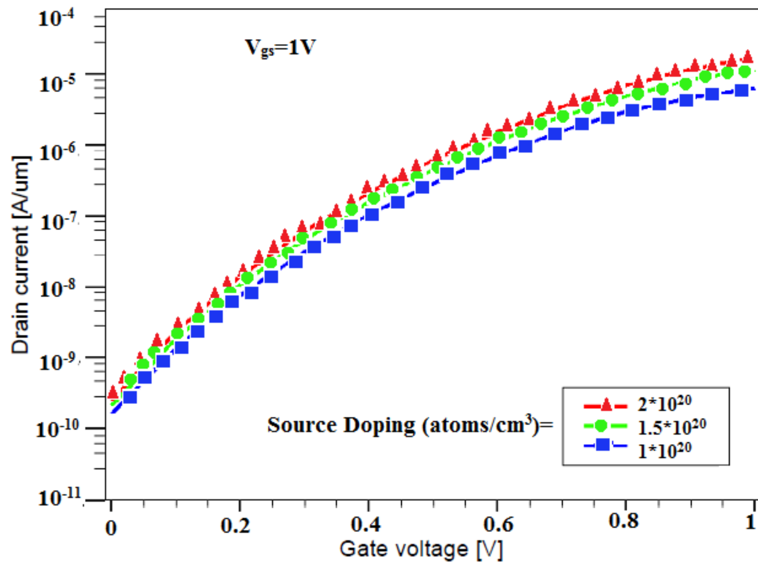

Figure 4. I_{ds}-V_{gs} characteristics of DG-PNIN TFET with varying Source doping

3.2.2 Drain Doping Variations

Now the next doping level is drain doping level and this doping level is important for another reason. The effect of drain doping level on a device characteristic can be seen when it is operating in negative region. Fig. 5 shows, the comparative graph of current characteristic of DG-PNIN TFET device with varying drain doping. When the device is in positive region there is no effect of drain doping variations on the current characteristic but, for negative region it shows the ambipolar characteristics which are undesirable for the circuit designers. The DG-PNIN TFET shows ambipolar behavior when drain doping level is equal to the source doping level. So for the device optimization, a low drain doping is preferable but it should not be too low that the contact formation becomes difficult.

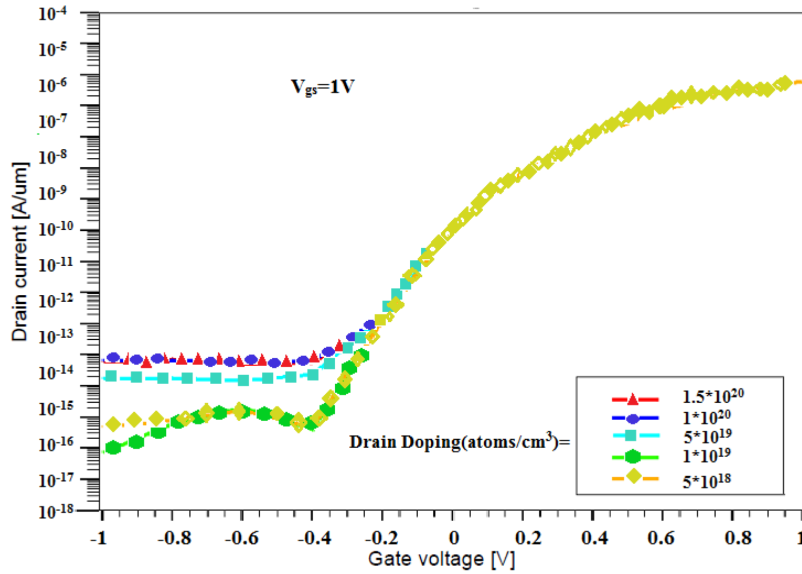

Figure 5. I_{ds}-V_{gs} characteristics of DG-PNIN TFET with varying Drain doping

3.2.3 Intrinsic Doping Variations

Now the next doping level is intrinsic region doping level. This doping level has a little effect on Tunnel FET characteristics until the doping level becomes high. Fig. 6 shows the comparative graph of current characteristic of device with varying intrinsic doping from 10^{15} atoms/cm^3 to 10^{19} atoms/cm^3. When intrinsic doping is less than 10^{18} atoms/cm^3 it has a little effect on the current characteristics of DG-PNIN TFET device and exact concentration and type is not important because at low concentration it does not affect the gates ability to control the band to band tunneling at tunneling junction. But when the intrinsic doping level increases, off-current also increases rapidly because at higher doping level intrinsic region is no more intrinsic. Thus a lightly doped intrinsic region is preferable for DG-PNIN TFET optimization.

3.2.4 Pocket Doping Variations

Now the next and the last doping level is pocket doping level which has to be considered for TFET optimization. In PNIN TFET device, an n-type layer is used as pocket in channel region near the source region to increase I_{on}/I_{off} ratio. So this pocket doping level also has a great effect on the device characteristics. Here, the DG-PNIN TFET device is simulated at various pocket doping levels and the comparative current characteristics of the device is shown in Fig. 7. When the pocket doping increases or becomes equal to source doping then it gives a large amount of off-current due to great amount of charge carrier available at the channel region which will tunnel

from channel to source in off-state resulting off-current. And if the pocket doping is made too low then the advantage of using pocket cannot be utilized. So balanced pocket doping level is preferable for the DG-PNIN TFET optimization.

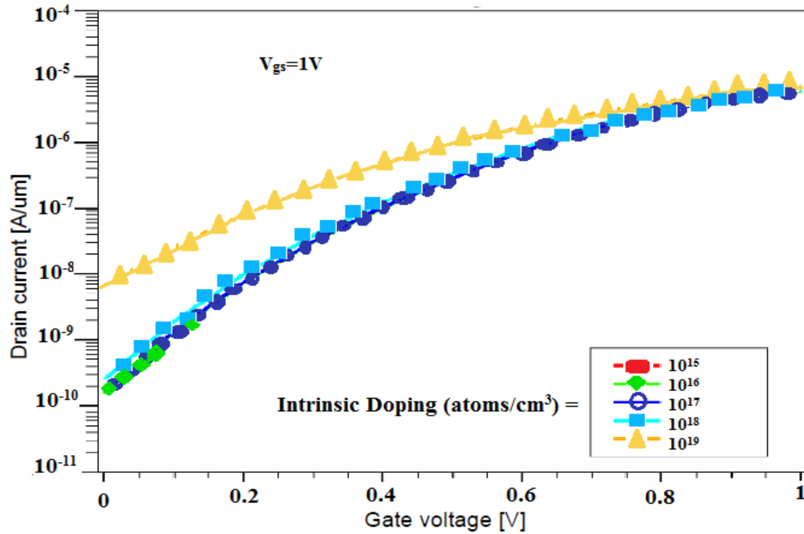

Figure 6. I_{ds}-V_{gs} characteristics of DG-PNIN TFET with varying Intrinsic doping

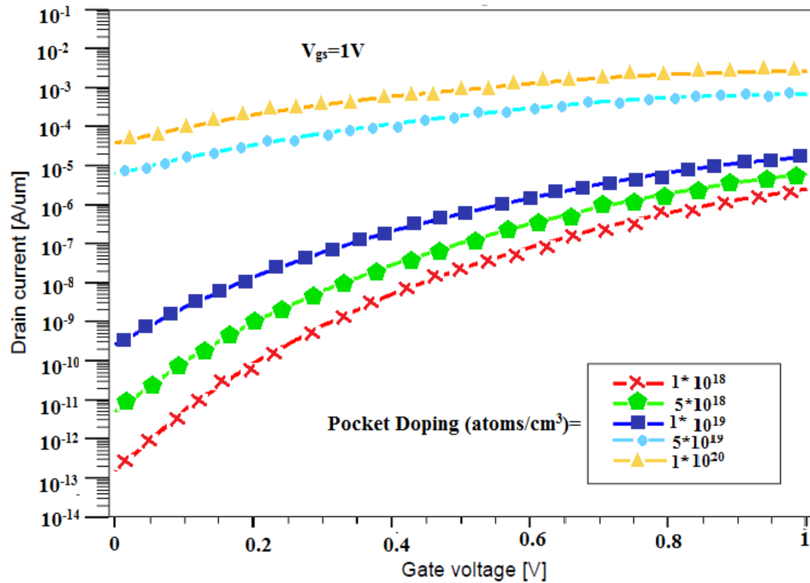

Figure 7. I_{ds}-V_{gs} characteristics of DG-PNIN TFET with varying Pocket doping

3.3. Body Thickness Variations

Another important parameter is body thickness of Silicon and TFET device is very much sensitive to this thickness. Fig. 8 shows, the comparison of current characteristics of DG-PNIN TFET device with varying body thickness. For larger body TFET device, the tunneling probability reduces thus on-current also reduces. Therefore, thin body TFET structures are needed for better performance. As body thickness becomes smaller than 10nm the on-current decreases in a large amount due to decreased tunneling area for the current flow of the device. So for DG-

PNIN TFET optimization, thin body structures are beneficial but it must stay above some critical thickness so that on-current will not degrade.

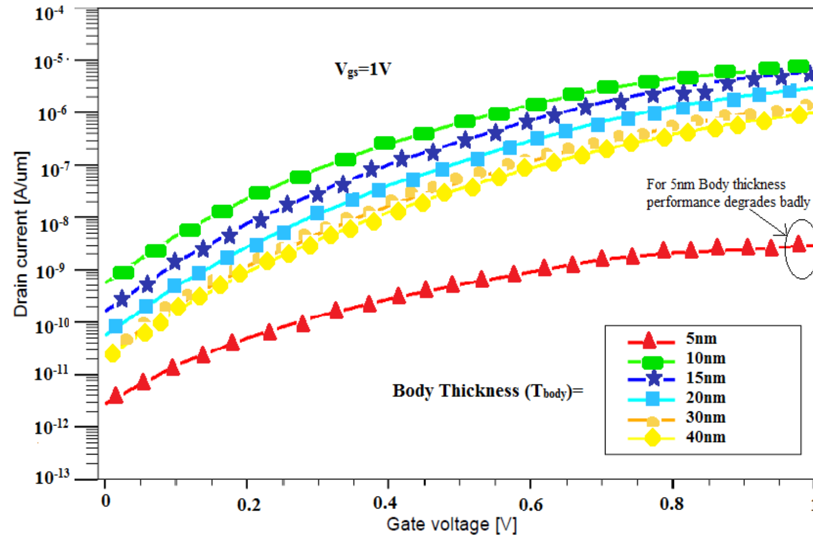

Figure 8. I_{ds}-V_{gs} characteristics of DG-PNIN TFET with varying Body thickness

4. DG-PNIN TFET OPTIMIZATION

In this section the optimization of fundamental DG-PNIN TFET parameters has been done based on the parameter variation analysis. The main analysis that has been done is, the on-current increases with the high-k gate oxide layer due to increased dielectric permittivity, At source channel tunnel junction with increased source doping on-current also increases due to band bending in between conduction and valance bands, to suppress ambipolar behavior drain doping should be low, at high intrinsic doping off-current increases so low intrinsic doping is desirable, pocket doping should be moderate because at high pocket doping off-current increases and low doping leads to on-current decrement, Finally a thin body TFET structure is needed for current improvement but it must be above 10nm because below 10nm the performance degrades badly due to small tunneling area.

The Tunnel FETs have a low off-current and the potential for a small SS, but they suffer from a lower on-current than conventional MOSFETs. Many solutions and topologies have been proposed, but performance boosters are often suggested independently, like just adding a high-k dielectric, or just using a thin body or just decreasing the band gap at the tunnel junction etc. These techniques, though they increase on-current and reduce sub threshold swing, only have limited power to improve device characteristics. In order to achieve superior characteristics for Tunnel FETs, it is essential to apply as many boosters as possible to the same device, so that the improvements in device performance are progressive. Then with the fully optimized device, parameter fluctuations can be investigated in great detail.

With Wentzel-Kramer-Brillouin (WKB) approximation and taking the tunnel barrier as a triangularly shaped potential barrier the band-to-band tunneling transmission is given by equation 1.

$$T(E) \cong \exp\left(\frac{-4\lambda\sqrt{2m^*}\,E_g^{3/2}}{3\hbar\left(E_g+\Delta\phi\right)}\right) \quad where,\lambda=\sqrt{\frac{\varepsilon_{Si}\, t_{Si}\, t_{ox}}{2\varepsilon_{ox}}} \qquad (1)$$

In this equation E_g represents the band-gap of the material, m* is the effective mass of the tunneling particle (material dependent), $\Delta\phi$ is the energy range over which tunneling takes place, λ is the screening length and it depends on ε_{Si}(permittivity of silicon), t_{ox} (oxide thickness), t_{Si} (Silicon body thickness) and ε_{ox}(permittivity of gate oxide layer). To get higher current, tunneling probability must be higher.

There are three main parameters that can help to increase T(E) of TFET device. These parameters are m*, E_g andλ. Where m* and E_g are material dependent and by using small band gap and smaller mass materials the tunneling probability can increase, λ is the device dependent parameter. It depends on dielectric layer thickness, body thickness etc. and by optimizing these parameters, λ can also be optimized and tunneling probability will increase. That is why m*, E_g and λ are considered as performance boosters for TFET. With the help of these performance boosters, TFET performance can be boosted to meet its target parameters, that are high on-current (in the range of hundreds of mA), sub threshold slope (SS) less than 60mv/dec and I_{on}/I_{off} ratio greater than 10^6. By achieving these target parameters, TFET can give the performance comparable to CMOS in future technology. Based on the above all parameter variations analysis, these parameters are optimized in such a manner that device current characteristics parameters improves. The optimized parameters of the TFET device are listed in table 2. The column 2 of the table 2 describes the parameter on which optimization has been performed and column 3 and 4 describes the value of these parameters before and after optimization.

. Table 2. DG-PNIN TFET parameters before and after optimization

No.	Parameter	Before Optimization	After Optimization
1	Gate Oxide Material	SiO_2	HfO_2
2	Source Doping (N_s)	10^{20} atoms/cm^3	$2*10^{20}$ atoms/cm^3
3	Drain Doping (N_d)	10^{20} atoms/cm^3	10^{19} atoms/cm^3
4	Channel Doping ($N_{channel}$)	10^{17} atoms/cm^3	10^{15} atoms/cm^3
5	Pocket Doping (N_{pocket})	10^{19} atoms/cm^3	$5*10^{18}$ atoms/cm^3
6	Body Thickness(T_{body})	15nm	10nm

Now the DG-PNIN TFET device (Fig.1) is simulated in SILVACO ATLAS with all optimized parameters with t_{ox}=3nm, L_g=60nm with nonlocal band to band tunneling (BTBT), Shockley Read Hall (SRH) and Fermi Dirac models at room temperature. Fig. 9 shows the comparative graph of current characteristics of the device with and without parameter optimization. From the figure it is clear, that due to heavy source doping, lesser body thickness and due to high-k dielectric layer the on-current is increased. Because, as source doing increases the electric field increases at tunnel junction and because of that, band bending occurs between valence and conduction bands. As intrinsic doping is reduced, so there will be lesser electric field in reverse direction so, off-current is still low and in acceptable range.

A comparison of current characteristics parameters for before and after optimization has been done in table 3. By applying all optimized parameters together the device performance improves with on-current enhancement from 0.8µA to 45µA. Its off-current also increases slightly but still very low in pA and lies within the acceptable range. The threshold voltage (V_{th}) for optimized device is 0.39V calculated by constant current method. The I_{on}/I_{off} ratio is greater than 10^6 which is good.

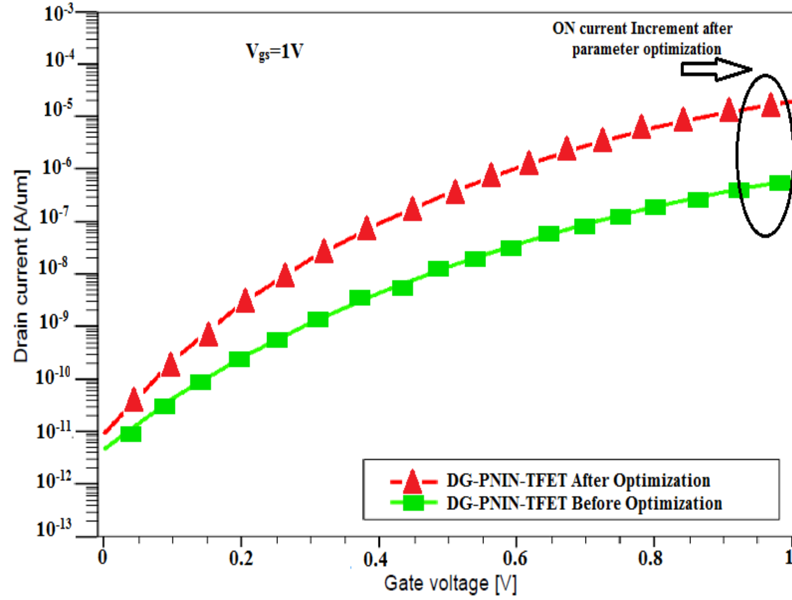

Figure 9. Comparison of I_{ds}-V_{gs} characteristics of DG-PNIN-TFET before and after optimization

Table 3. DG-PNIN TFET current characteristics parameters before and after optimization

	I_{on}	I_{off}	I_{on}/I_{off}	V_{th}
Before Optimization	0.8μA	6pA	$1.33*10^5$	0.71V
After Optimization	45 μA	10pA	$4.5*10^6$	0.39V

5. CONCLUSIONS

A DG-PNIN Tunnel field effect transistor is designed and investigated with different parameter variations. The main findings are:- (1) By using HfO_2 as dielectric layer material instead of SiO_2 dielectric layer material, the on-current increases due to better gate coupling provided by high-k dielectric material (i.e. HfO2). (2) To improve the current characteristics, a high source doping is beneficial to increase tunneling between source and channel regions by increasing electric fields, a low drain doping is desirable to suppress the ambipolar behavior in negative regions and a lightly doped intrinsic region (below 10^{18} atoms/cm^3) is desirable to decrease off-current in off-state. (3) Smaller body thickness is required to increase tunneling probability by optimizing the tunneling area of the device but, it must not be below from the critical thickness of body (i.e. 10nm). Based on these analyses, an optimization has been performed on PNIN TFET device parameters for on-current improvement. So resulting optimized device had a double gate, a high-k dielectric layer, a high source doping, a low drain doping, a lightly doped intrinsic region, smaller body thickness that should be above of its critical thickness. With these optimized parameters the on-current increases from 0.8μA to 45μA with high I_{on} / I_{off} ratio (>10^6). But the on-current is still in μA range and the further enhancement of on-current is required without any compromise in off-current to meet the TFET target parameters.

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