LOW POWER 16-CHANNEL DATA SELECTOR FOR BIO-MEDICAL APPLICATIONS

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ABSTRACT

This paper demonstrates the design of the 16-channel data selector with improved DTMOS switch logic of low power, low on-resistance for bio-medical applications, This 16 channel data selector can operate at dynamic range of 1uV to 0.2V. The ON resistance is achieved 36 ohm with a switching speed of 10MHz and it Operated at a dual supply voltage ranges from ± 0.2V. The power dissipation is obtained around 0.04uW. PVT Corner analysis has carried out for the characteristics are mentioned at various temperatures.

KEYWORDS

Analog Data selector, DTMOS, PVT Corners.

1. INTRODUCTION

One of the instruments that are very much helpful for the cardiac patients is Electrocardiogram (ECG). ECG is a graphic display of time variant voltages produced by the myocardium during cardiac cycle. ECG is used to monitor and observe the heart functionality. The bio-potentials generated from various parts of the body results in the Cardiograph. ECG consists of instrumentation amplifier, with inverting and non inverting terminals. These inputs are acquired by the analog data selector which was fed by the different sensing leads connected to the body. ECG measurement information is collected by electrodes placed at designated locations on the body. It is the best way to measure and diagnose abnormal rhythms of the heart [1], particularly abnormal rhythms caused by damage to the conductive tissue that carries electrical signals, or abnormal rhythms caused by electrolyte imbalances [2]. Electrodes connected to the body in order to record ECG are called leads. These leads are divided into three types i) Bipolar limb leads ii) Unipolar limb leads iii) Unipolar chest leads.

These leads collect information which is in the analog form having less amplitude. In order to process these signal it has to be amplified and hence instrumentation amplifier is required. Two different analog data selectors are used to acquire the inputs for both the terminals of an instrumentation amplifier. The DTMOS technique was first introduced in 1994 [3], [4]. Since then, many novel circuit applications of this technique have been proposed. analog designers must continuously find low-voltage circuit techniques in order to be consistent with technology trends [5], [6].Multi-channel data selector system selects one of several analog inputs and forwards the selected input into a single output line. Data selector of 2n inputs has n selection lines, these selection lines are used to select one input at a time to appear as the output. Here selection lines are generated by decoder.

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2. DESIGN OF A CMOS SWITCH

The complementary-MOS process (CMOS) consists of P-channel and N- channel MOSFETs. CMOS switch can be obtained by connecting the PMOS and NMOS devices in parallel form. This combination reduces the on-resistance, and also produces a resistance which varies much less with signal voltage.

The ideal analog switch has low on-resistance, infinite off resistance and zero time delay. In practice, a CMOS analog switch doesn't meet any of these criteria. In the ON state, its resistance is few ohms, while in the OFF state, the resistance increases to several mega ohms. MOSFET transistors are bilateral, they can switch positive and negative voltages and conduct positive and negative currents with equal ease.

The DTMOS technique is mostly used in digital applications in which the gate and body of the MOSFET are tied and threshold voltage changes dynamically by using the relationship from equation.

$$V_{TH} = V_{TO} + \gamma(\sqrt{|2\emptyset_F| + V_{SB}} - \sqrt{|2\,\emptyset_F|})$$

This is to reduce the leakage current during off state and reducing the threshold voltage during on state to increase the overdrive voltage. It is also possible to use the DTMOS technique in bulk CMOS technology for analog circuit applications. However, in analog applications the body terminal of the MOSFET transistor is normally used as a fourth terminal.

In the standard bulk CMOS technology, it is possible to use the body of PMOS transistors as a fourth terminal to the MOSFET. Dynamic threshold MOS transistor body tied- to gate DTMOS Figure 1 & 2 can be operated at low power supply while maintaining a large drain current for high speed application, without introducing any extra amount of standby current, therefore it is suitable for low voltage VLSI applications.

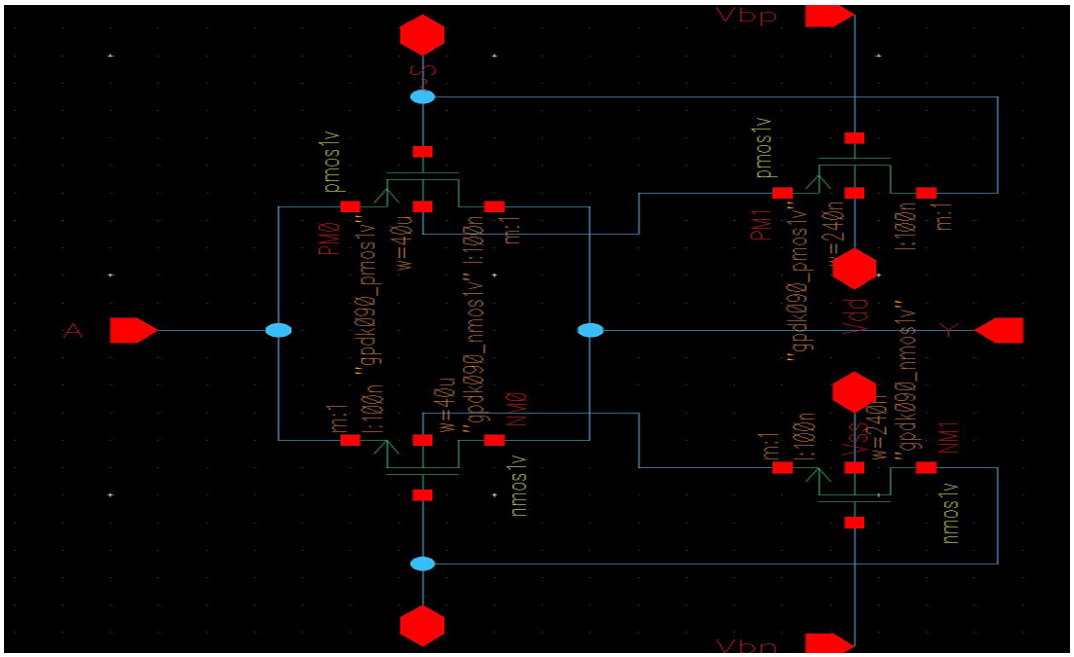

Figure 1 CMOS analog switch with body biasing

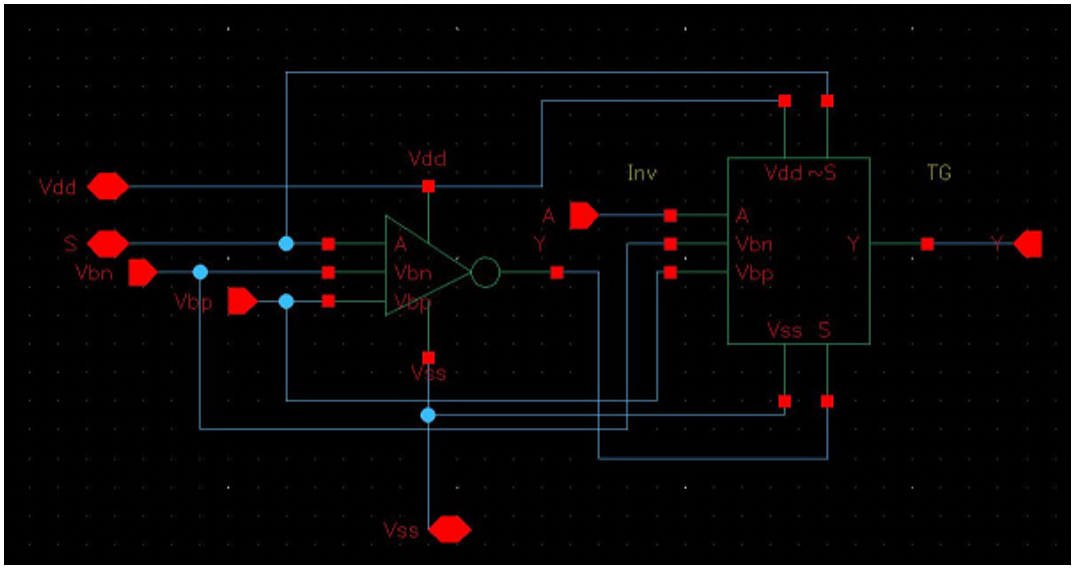

Figure 2 Testing circuit diagram of analog switch

The output resistance of MOS transistors is reduced as CMOS technology scales down, which consequently reduces the maximum achievable gain of the transistor. Similarly, the reduced output resistance makes the design of supply independent biasing network a challenging task. When the gate voltage is HIGH, the body bias of n-MOSFET is VDD and body bias of p-MOSFET is VSS. The source substrate junctions of both the transistors are forward biased.
The transmission gate is ON. When it is LOW, the body bias of n-MOSFET is switched to VSS and p-MOSFET switched to VDD. When the source-substrate junctions of both the transistors are reversed biased. The transmission gate is fully "off".

3. 16 CHANNEL DATA SELECTOR

Data selector has been designed by using decoder and the switch logic. The output of the decoder allows the switch to pass the any one of the no of input signals. Decoder is a combinational circuit that converts binary information from 'n' coded inputs to a maximum of 2^n unique outputs. From 2^n outputs, any of the one output is at logic high state remaining outputs at the logic low state. In 16-channel Data selector, having four selection inputs are applied to the decoder and hence producing 16 unique outputs. These are acts as control signals to the 16 different switches, allowing only one switch to be ON- state and that corresponding input of the switch is collected by the output terminal.

The Figure 3. shows CMOS 16-Channel analog data selector which consists of 16 switches are used to process the input depends on the selection line. Selection lines are from the 4 to 16 decoder.

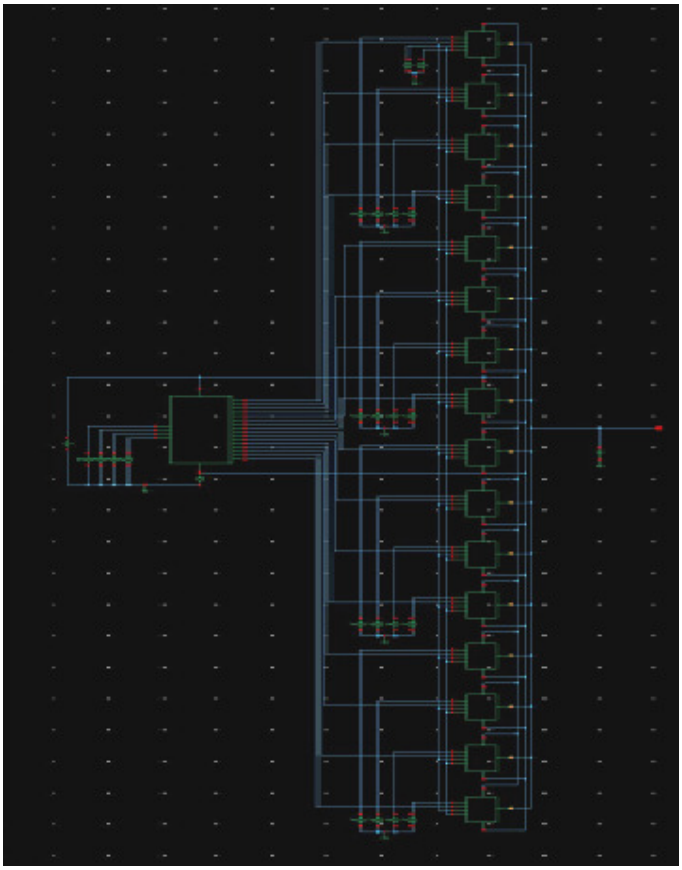

Figure 3. 16 Channel Data selector

4. RESULTS

4.1 Switching Frequency vs. Power Dissipation

The CMOS analog switch and 16 to 1 data selector multiplexer simulated and outputs are shown in figure 4 and 5. As the switching frequency increases the speed of the device also increases and at different switching frequencies of data selector the power dissipation values are calculated. As the increase in the switching frequency causes the load capacitor to charge and discharge very quickly the dissipation increases tremendously. Fig 6 shows the relation between the switching frequency and the power dissipation. Also for different power supply the power dissipation is plotted for different switching frequencies. The power dissipation is almost equal for switching frequencies up to 10 KHz with same power supply voltage. After this point of $f_{switch,}$ the dissipation increases rapidly.

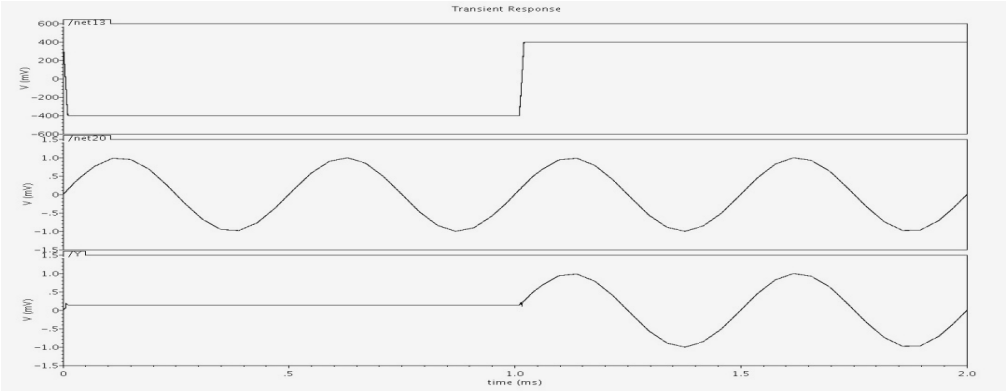

Figure 4. CMOS Analog Switch Output Wave Form

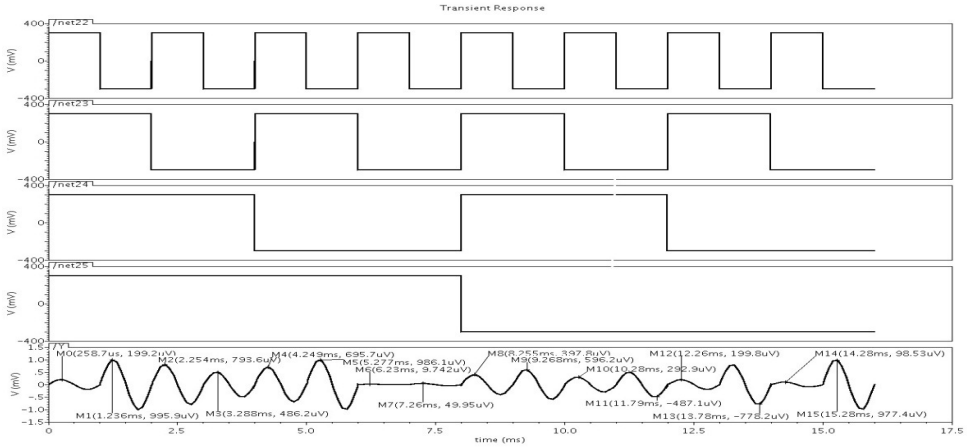

Figure 5. 16 Channel Data selector output with different amplitude

Supply ±200mV, V_{IN} = 1mV, Input Signal frequency = 100Hz, C_L=1nF.

Table 1 Power dissipation for ±200mV supply voltage

f_{Switch}	$I_{Leakage}$ (nA)	P_{static} (nW)	$P_{Dynamic}$ (µW)	P_{Total} (µW)
1K	270	9.624	0.040	0.04962
10K	270	9.874	0.400	0.40987
100K	270	10.67	4.000	4.010
1M	270	20.11	40.000	40.02

Supply ±250mV, V_{IN} = 1mV, Input Signal frequency = 100Hz, C_L=1nF.

Table 2 Power dissipation for ±250mV supply voltage

f_{Switch}	$I_{Leakage}(nA)$	$P_{static}(nW)$	$P_{Dynamic}(\mu W)$	$P_{Total}(\mu W)$
1K	1.1518	33.18	0.0625	0.0956
10K	1.1518	34.04	0.625	0.6590
100K	1.1518	34.83	6.250	6.284
1M	1.1518	50.06	62.500	62.55

Supply ±300mV, V_{IN} = 1mV, Input Signal frequency = 100Hz, C_L=1nF.

Table 3 Power dissipation for ±300mV supply voltage

f_{Switch}	$I_{Leakage}(nA)$	$P_{static}(nW)$	$P_{Dynamic}(\mu W)$	$P_{Total}(\mu W)$
1K	4.023	154.6	0.090	0.2446
10K	4.023	157.5	0.900	1.057
100K	4.023	157	9.000	9.157
1M	4.023	179.6	90.000	90.179

Supply ±350mV, V_{IN} = 1mV, Input Signal frequency = 100Hz, C_L=1nF.

Table 4 Power dissipation for ±350mV supply voltage

f_{Switch}	$I_{Leakage}(nA)$	$P_{static}(nW)$	$P_{Dynamic}(\mu W)$	$P_{Total}(\mu W)$
1K	10.709	807	0.1225	0.929
10K	10.709	815.1	1.225	2.040
100K	10.709	810.3	12.250	13.31
1M	10.709	842.1	122.500	123.342

Supply ±400mV, V_{IN} = 1mV, Input Signal frequency = 100Hz, C_L=1nF.

Table 5 Power dissipation for ±350mV supply voltage

f_{Switch}	$I_{Leakage}(nA)$	$P_{static}(nW)$	$P_{Dynamic}(\mu W)$	$P_{Total}(\mu W)$
1K	22.16	4.14	0.160	4.3
10K	22.16	4.169	1.600	5.769
100K	22.16	4.154	16.000	20.154
1M	22.16	4.197	160.000	164.197

The Tables show power analysis of analog data selector at different switching frequencies and at different supply voltages 0.2V, 0.25V, 0.3V, 0.35V, 0.4V). As the switching frequency increases power dissipation also increases because dynamic power is CV^2f_{switch}.

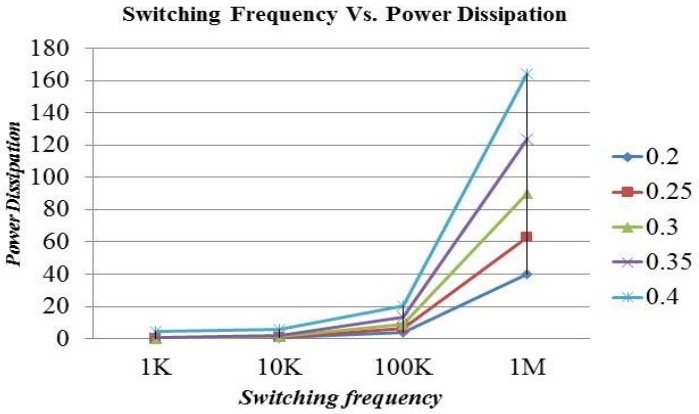

Figure 6 Switching Frequency Vs Power Dissipation

4.2 CORNER ANALYSIS

A process corner is an example of a technique that refers to a variation of fabrication parameters used in applying an integrated circuit design. The increasing sensitivity of circuit performance to process, temperature, and supply voltage (PVT) variations has led to an increase in the number of process corners that are required to verify circuit timing[8],[9].

Table 6 Corner analysis of CMOS analog switch at input voltage of 1mV.

V_{DD} (V)	FF			SS			TT		
	-40°C	27°C	125°C	-40°C	27°C	125°C	-40°C	27°C	125°C
0.3	0.975	0.989	0.979	0.975	0.989	0.979	0.975	0.989	0.979
0.35	0.973	0.990	0.980	0.973	0.990	0.980	0.973	0.990	0.980
0.4	0.973	0.988	0.979	0.973	0.988	0.979	0.973	0.988	0.979

The Table 6 shows the output voltage information of the switch for various process corners. The voltages mentioned in the above are in Volts.

Table 7 Corner analysis (average current) of CMOS analog switch at input voltage of 1mV

V_{DD} (V)	FF			SS			TT		
	-40°C	27°C	125°C	-40°C	27°C	125°C	-40°C	27°C	125°C
0.3	28.67	202.3	4,180	22.58	126.3	2,270	25.04	165.3	3,225
0.35	28.67	202.3	4180	22.58	126.3	2,270	25.04	165.3	3,225
0.4	28.67	202.3	4,184	22.58	126.3	2,270	25.04	165.3	3,225

The Table 7 shows corner analysis of CMOS analog switch at different supply voltages and different temperatures. The currents values mentioned in the Table VII are measured in nA. The output current is measured by applying the input voltage of 1mV.

5. CONCLUSION

The proposed 16 channel data selector is an efficient design that suits the requirements of portable, low power Bio-medical application. This design is tested for several supply voltages with various switching frequencies and the PVT corner analysis has been included in the design testing. At 200mV supply, 100KHz switching frequency the power dissipation is 4µW and 20.15µW at 400mV supply with same switching frequency. From the experimental results mentioned its suits for low power, portable bio-medical applications.

REFERENCES

[1] Braunwald E. (Editor), Heart Disease: A Textbook of Cardiovascular Medicine, Fifth Edition, p. 108, Philadelphia, W.B. Saunders Co., 1997. ISBN 0-7216-5666-8.

[2] Van Mieghem, C; Sabbe, M; Knockaert, D (2004). "The Clinical value of the ECG in no cardiac conditions" Chest 125(4):1561–76.Doi:10.1378/chest.125.4.1561.PMID 15078775.

[3] F. Assaderaghi, D. Sinitsky, S. Parke, J. Bokor, P. K. Ko, and C. Hu, "A Dynamic Threshold voltage MOSFET (DTMOS) for ultra- low voltage operation," in Int. Electron Devices Meeting, Techn. Digest, 1994, pp.b809–812.

[4] F. Assaderaghi, "DTMOS: Its derivatives and variations, and their potential applications," in Proc. 12th Int. Conf. Microelectron., 2000, pp.9–10.
[5] F. Maloberti, F. Francesoni, P. Malcovati, and O. J. A. P. Nys, "Design considerations on low-voltage low-power data converters," IEEE Trans. Circuits Syst. I, Fundam. Theory Appl., vol. 42, no. 11, pp.853–863, Nov. 1995.
[6] V. Peluso, P. Vancoreland, A. M. Marques, M. S. J. Steyaert, and W. Sansen, "A 900-mV low-power delta-sigma A/D converter with 77-dB dynamic range," IEEE J. Solid-State Circuits, vol. 33, no. 12,pp. 1887–1897, Dec. 1998.
[7] C. Zhang, A. Srivastava and P. K. Ajmera, "0.8-V ultra low-power CMOS analog multiplexer for remote biological and chemical signal processing," Proc. of SPIE, Vol 5389, pp.13-19, 2004.
[8] J. J. Nian, S. H. Tsai, and C. Y. Huang. A unified multi-corner multi-mode static timing analysis engine. In ASP-DAC, pages 669–674, 2010.
[9] S. Birla, M. Pattanaik and R. K. Singh, "Static Noise Margin Analysis of Various SRAM Topologies," IACSIT International Journal of Engineering and Technology, Vol. 3, No. 3, 2011, pp. 304-309.
[10] Weste, Neil H.E. and Harris, David (2005). CMOS VLSI Design: A Circuits and Systems Perspective, 3rd Ed., Addison-Wesley, pp.231-235. ISBN 0-321-14901-7.

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