PERFORMANCE ANALYSIS OF GATED RING OSCILLATOR DESIGNED FOR AUDIO FREQUENCY RANGE ASYNCHRONOUS ADC

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ABSTRACT

This paper presents performance analysis of Gated Ring Oscillator (GRO). Proposed GRO is designed to employ in implementation of Time to Digital Converter (TDC) block of Asynchronous ADC. For an audio frequency range ADC, minimum GRO stages are designed using asynchronous technique. So leads to reduced area and power. Compared to conventional Ring Oscillator (RO), we avoided to employ the gated clock; to evade clock design related problems like jitter, additional area and power. Instead we preferred gating of ring oscillator itself. Consequently during sleep mode, GRO disables automatically which saves the dynamic power. Furthermore it also provides first order noise shaping of the quantization and mismatch noise. Proposed GRO is implemented with 0.18µm CMOS Digital Technology in Cadence Virtuso environment. GRO performance analysis shows oscillation frequency as 286 KHz with 327ps jitter and average power consumption of 1.08µW.

KEYWORDS

Gated Ring Oscillator (GRO), Time to Digital Converter (TDC), Noise Shaping, Delay Stages, Dynamic Power

1. INTRODUCTION

Transistor and parasitic mismatch has become the significant problem due to scaling in CMOS advanced technology [1]. Therefore analog circuit design has become critical. Comparatively digital circuits benefit from technology scaling like; improved resolution due to decrease in minimum gate delay. GRO is an important building block of Time to Digital Converters (TDC) [2], [3]. TDC finds applications in Time-based Analog-to-Digital Converters (TADC) [4], DPLL for clock generation and data recovery [5] as well MDLL-Based Clock Multiplier [6]. Achieving high performance in such systems depends on TDC implementation and performance [7]. To realize highly digital ADC implementation, the investigation is till persistent. It is specifically for unconventional approaches to use time-based quantization within an ADC [4].

In an asynchronous ADC (A-ADC), TDC measures the instantaneous time difference between the output pulse width edges with reference frequency. The desired properties of TDC implementations are to achieve high resolution in time measurement with large Dynamic Range (DR) [7]. GRO is required in TDC block to count the transitions during the specific measuring cycle. GRO-TDC has a good effective resolution due to intrinsic first-order noise shaping

property [8]. This work presents a GRO which can employ for implementation of TDC block of A-ADC with audio frequency range. Proposed GRO uses the basic principle of gating functionality with the advantages like simplicity, low noise, minimum jitter, low power and reduced area.

The gated oscillator requires a simple digital counter, whereas conventional circuits need analog input/output or an analog-to-digital / digital-to-analog converter [9]. In addition, common digital timing generators, which are often used in other sampling circuits, such as in [10] and [11], can be adopted for the timing generator of this circuit. Thus, the proposed measurement system can be easily embedded by using only digital standard cells.

2. FUNDAMENTALS: GRO IMPLEMENTATION

Ring oscillator is a closed loop constructed from an odd number of identical inverters. It emerges as a negative feedback system. Oscillation period becomes twice the sum of gate delays in the ring. RO is gated to design GRO, as it executes first order noise shaping of the quantization error. Figure 1 illustrates the key concept of a GRO-TDC as in [3]. Unlike a traditional oscillator-based TDC, the GRO structure only allows the oscillator to have transitions (i.e., to be "gated" on) during a given measurement, and strives to freeze the ring oscillator state between measurements. This helps in power saving as compared to the free running RO. The major benefit of gating the oscillator is first order quantization noise shaping; as the residue at the end of a give measurement interval is transferred to the next measurement interval [3]. With $T_{start}[k] = T_{stop}[k-1]$, the quantization error for a particular period is:

$$T_{error}[k] = T_{stop}[k] - T_{start}[k] = T_{stop}[k] - T_{stop}[k-1] \tag{1}$$

This discrete-time domain first-order difference recounts in the frequency domain, as a first order noise shaping. In fact GRO sets up with „HIGH" at Enable; and else it stops. Role of counter is to count the oscillator edge transitions for each sample. In turn, it proportionately presents the enable pulse width. After every sample the oscillator state is detained. As a result, the initial position for the subsequent sample is the end point of the preceding sample. Consequently, the first order noise shaping occurs due to scrambling of residue [12].

Conceptually GRO is the traditional Ring Oscillator (RO) with appended gating functionality. It is possible just by adding transistor switches for each inverter as shown in Figure 2. Closed switches, enables the oscillation and it behaves like a classical RO as in Figure. 2(a). On the contrary oscillation is suspended with the open switches, as shown in Figure 2(b). Hence there is no path for charging and discharging of output parasitic capacitance. As a result charge will be stored on the parasitic capacitance of the delay elements and mismatch errors for preceding sample is conveyed to and deducted from the subsequent sample. Thus at the end of enabled state, GRO holds the oscillator phase throughout the disabled state [3].

Overall GRO processing is comparable to Barrel-Shift Algorithm as well the delay element variance is also first-order noise shaped. With a specified input; delay elements" selection is comparable to dynamic element matching. Overall the GRO-TDC realizes intrinsic scrambling of its quantization and first-order noise shaping of variance error [3]. We employ these fundamentals for the proposed GRO design to achieve reduced power and compact area.
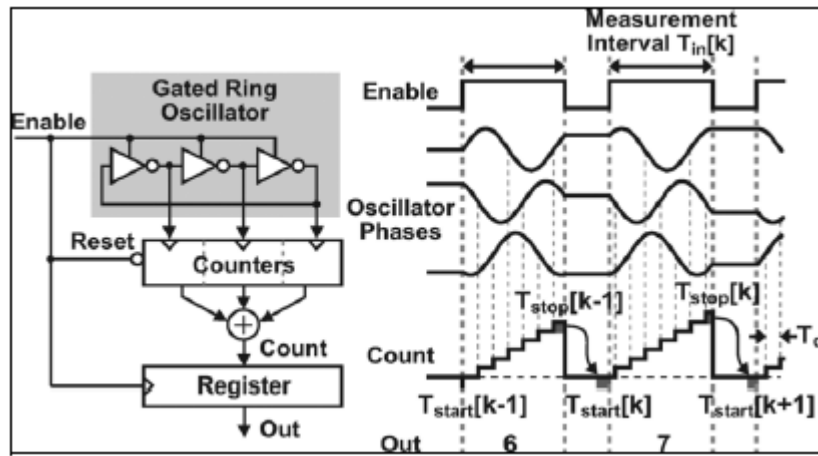
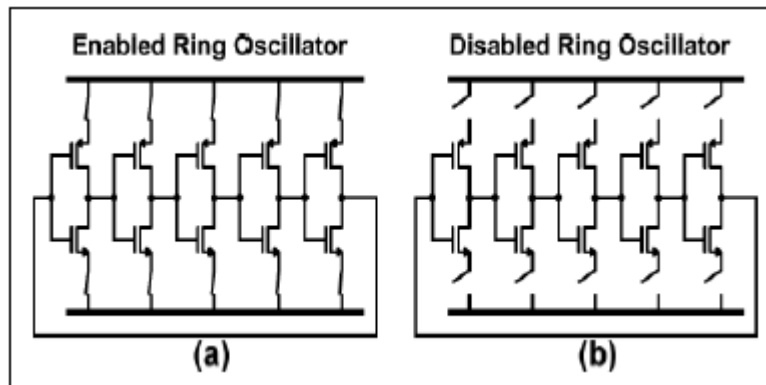Figure 1. Gated Ring Oscillator Based TDC [3]

Figure 2. Conceptual Implementation of gating a ring oscillator [3]

3. PROPOSED GRO DESIGN AND IMPLEMENTATION

In this paper we propose a simple clockless GRO implementation which can be used for TDC implementation. To achieve minimum GRO stages we preferred to employ asynchronous techniques used by Kyu-Dong Hwang and Lee-Sup Kim. This leads to about 40% to 70% gate count reduction compared to synchronous GRO-TDC [2]. Design intention is the signal processing of the output from an Audio Frequency Range Asynchronous Modulator. These modulators convert the event based analog signal into varying pulse width. The proposed design uses ring oscillator with enabled gated „ON" and else it is „OFF" and thus completely avoids the need for a clock. It accurately measures the time of a pulse width and also scrambles the residual timing error. We implemented the design for oscillations as per the Barkhausen Criterion of gain and phase shift as in [13].

3.1 Number of Delay Stages

GRO implementation uses series of closed loop CMOS inverters as shown in the Figure 3. Number of inverter stages should be odd for oscillations with proper phase. An N-stage ring oscillator has a period of 2N stage delays because a value must propagate twice around the ring to regain the original polarity. Asynchronous modulator output i.e. the square wave with varying pulse width is applied to "Enable" pin of the GRO. This square wave signal with two clearly distinct voltage levels (LOW and HIGH) clearly defines transitions between these two levels. During the time when the pulse width takes the higher voltage, the GRO turns "ON" and it starts oscillating with the switching frequency f_{SW}. This frequency is the function of transistor currents, alternately the transistor sizes of the inverter stages. For a required frequency of oscillation, the number of stages N can be designed for a specified rise time t_r and fall time t_f as well with a period of $2N$ using the equation:

$$f_{SW} = \frac{1}{2N \cdot (t_r + t_f/2)} = \frac{1}{2N \cdot t_{PD}}$$

(2)

where t_{PD} is the propagation delay of each delay stage and consider proportionality constant η typically close to one. Since rise and fall time depends on output capacitance C_{OUT}, transistor currents of inverter stages I_D and power supply V_{DD}, so (2) can also be expressed as:

$$f_{SW} = \frac{I_D}{2N \cdot C_{OUT} \cdot V_{DD}}$$

(3)

At the end of pulse width signal switches from 'HIGH' to 'LOW' and disables the GRO. It halts the oscillations and GRO hold its phase till the start of the subsequent 'ON' pulse. Significantly the GRO holds its phase, during the two measurement intervals and achieves the first order noise shaping of the quantization error.

3.2 Dynamic Power

Power performance trade-off is the key challenge of VLSI design. With 180 nm technology, we can neglect the static power dissipation for this particular design. Actively switching circuits consume dynamic power to charge and discharge the total output capacitance. Let E is the energy consumed over the switching time interval r i.e with switching frequency f_{SW}. Thus the capacitive load charges and discharges for $(T \cdot f_{SW})$ times. Hence average switching power becomes:

$$P_{SW} = E/T = (T \cdot f_{SW} \cdot C_{OUT} \cdot V_{DD}^2)/T = C_{OUT} \cdot V_{DD}^2 \cdot f_{SW}$$

(4)

Alternately, it depends on sizes and number of transistors with every switching (Refer (3) and (4)). To achieve the least possible switching power, minimum gate lengths are set for the calculated stage delay. Since this quadratic term V_{DD} contributes for greater dynamic powers

dissipation, minimum possible V_{DD} is selected to support the requisite frequency of operation. Delay stage design is optimized for minimum possible load capacitance.

Practically P_{SW} also depends on activity factor α, i.e. probability of switching the specific node from 'LOW (0)' to 'HIGH (1)'. So (4) modifies to;

$$P_{SW} = (C_{OUT}.V_{DD}^2.f_{SW})$$

(5)

We include the activity factor as the each transistor gate does not switch with every transition. So the event based random data for Asynchronous Modulator, has the switching probability equal to 0.5, so an activity factor α is maximum up to 0.5. Thus (5) modifies to;

$$P_{SW} = 0.5(C_{OUT}.V_{DD}^2.f_{SW})$$

(6)

Conventionally, 10% of switching power is added as a short circuit power. The sensitivity of the short-circuit power P_{sc} is the function of the ratio, r = (threshold voltage Vt / supply voltage VDD). Practically for $(0.2 < r < 0.3)$, short-circuit power shows variations $(10\% \text{ of } P_{SW} < P_{SC} < 2\% \text{ of } P_{SW})$.

With the selected transistor sizes and 1.8V supply voltage, we achieved r = 0.277, so short circuit power dissipation is hardly $3\% \text{ of } P_{SW}$ Practically it is negligible or to be very precise, total dynamic power for the proposed GRO becomes:

$$P_{DY\,max} = P_{SW} + P_{SC}$$

$$= (0.5).C_{OUT}.V_{DD}^2.f_{SW} + 0.03(0.5.C_{OUT}.V_{DD}^2.f_{SW})$$

(7)

Thus, $P_{DY\,max} = (0.515).C_{OUT}.V_{DD}^2.f_{SW}$

(8)

The best way to minimize the dynamic power is to deactivate GRO during OFF period of a modulator. Conventional ROs uses clock gating to turn it off during inactive signal, which turns off the power supply. We avoided employing the gated clock. Instead we preferred the gating of ring oscillator itself; so that during sleep mode, GRO disables automatically with 'HIGH' to 'LOW' signal transition. Hence the proposed GRO implementation avoids clock related issues like jitter, associated power consumption and added area. Thus overall system is designed for compact implementation with reduced power and better performance.
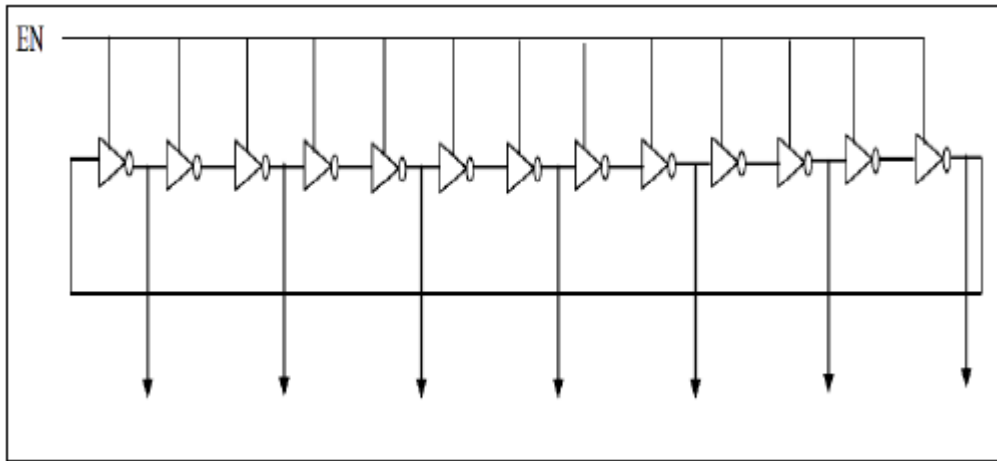
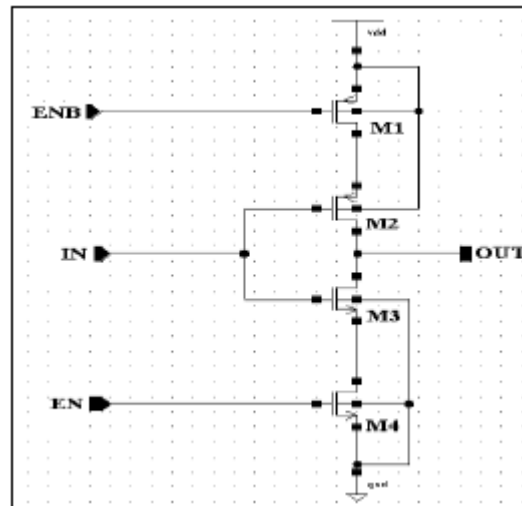Figure 3: Proposed Implementation of 13stage GRO for Audio frequency Range

Figure 4: Implementation: Inverter Delay stage for GRO

3.3 GRO Implementation

Proposed GRO is implemented with 0.18μm CMOS Digital Technology in Cadence Virtuso environment with 1.8V of V_{DD}. GRO is designed for output signal processing of Asynchronous Modulator with 15 KHz. So it uses 13 stages with the switching frequency of 390KHz. Figure 3 shows the proposed GRO implementation with 13 stages and with outputs taken from alternate 7 delay stages. These outputs will be connected to the counters which is the next stage of TDC implementation. The counter counts number of pulses generated at the output of GRO during the 'ON' pulse width interval.

Inverter delay stage implementation used in proposed GRO is as shown in Figure 4. Inverter transistor sizes of M2 and M3 is designed to achieve the required stage delay with minimum power consumption. The transistors M1 and M4 act as 'ON' switches during the measurement interval. Else M1 and M4 turn 'OFF' and disable the GRO. In consequence, inverter is unable to

charge or discharge the output capacitance between the two measurement intervals. Obviously, the GRO holds its state between the consecutive measurements. This implementation is further analyzed to study the performance.

4. RESULTS AND DISCUSSION

Proposed GRO is simulated using Cadence Spectre Simulator. Figure 5 shows the simulation result which demonstrates how the GRO holds its phase from end of one measurement interval to the start of subsequent measurement interval. It clearly shows disabled GRO (no oscillations) with low signal i.e. between successive measurement intervals. It also indicates that GRO continues from the preceding phase when the next enable signal arrives. Thus it has a vital role for quantization error noise shaping. Figure 6 shows the DC transfer characteristics of the inverter delay stage.
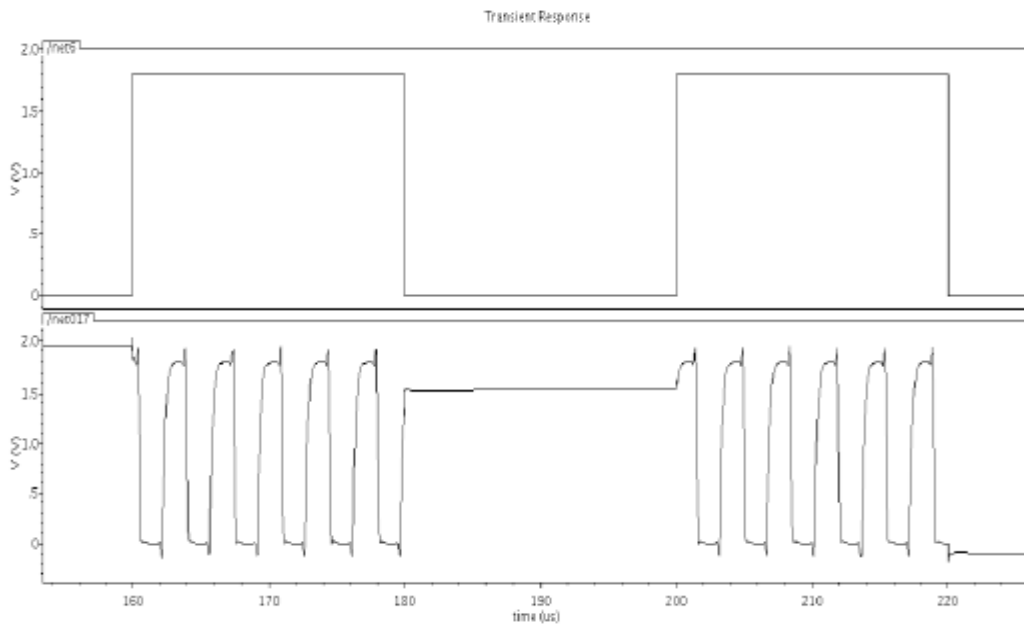

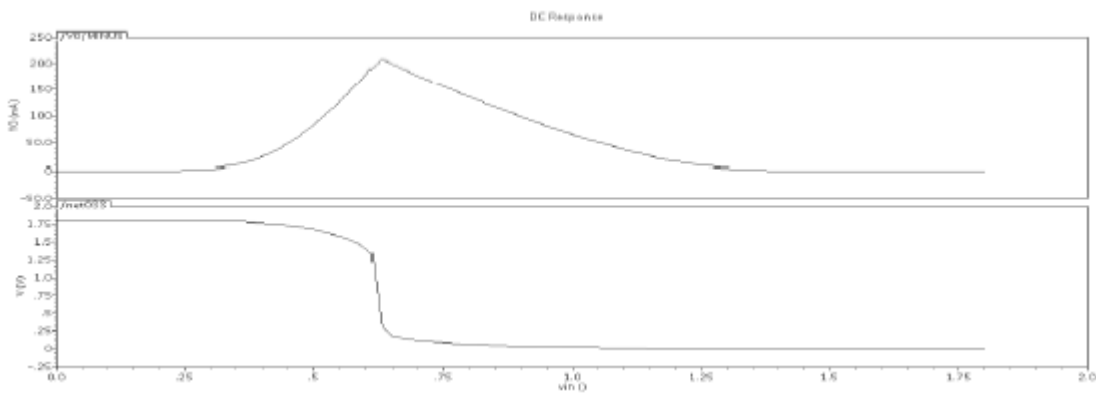Figure 5: GRO holds its phase during successive measurement intervals

Figure 6. DC Transfer Characteristics of Inverter Cell

Figure 7 shows the plot for magnitude and phase response of proposed GRO. It indicates 0dB, at 285.7 kHz i.e. unity gain is obtained nearly at the oscillating frequency which is the essential condition for GRO. The phase response indicates zero phase at the switching frequency. Thus the proposed design has achieved the necessary condition for oscillations i.e 0^0 phase shift around the loop.
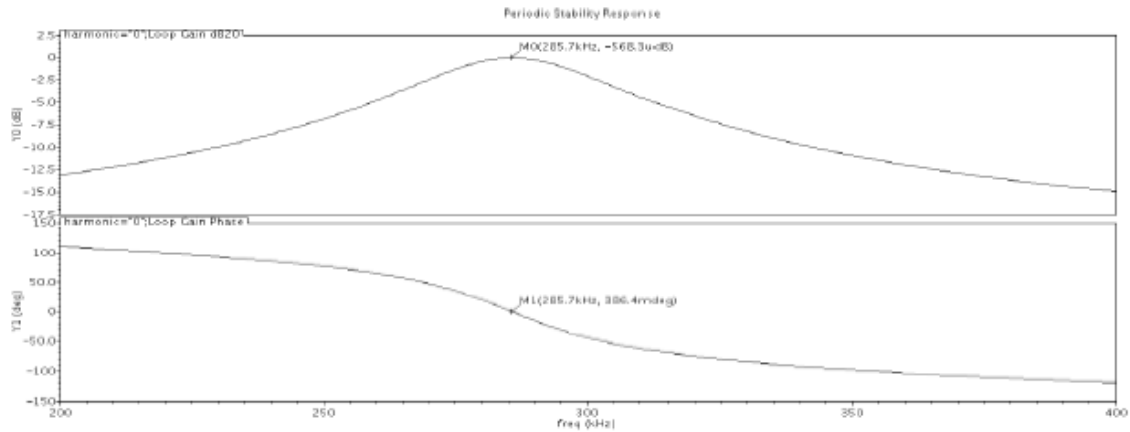

Figure 7. Magnitude and Phase response of GRO

The variation in GRO switching frequency with supply voltage variation is also studied. Figure 8 shows these deviations and also indicates the switching frequency as 287.5 KHz at 1.8V, which nearly same as calculated frequency. As the phase noise insights the decision on trade- offs of power, area and noise performance [14], we further studied the phase noise. It fundamentally also limits the dynamic range. Figure 9 shows the phase noise response at the GRO output. It indicates the phase noise as -110dBc/Hz with an offset of 10 kHz w.r.t. the carrier. Cycle to cycle jitter of 327ns (rms) is obtained by integrating phase noise for the frequency offset range 100 Hz to 1MHz. These two results as in Figure 8 and Figure 9 are obtained by PSS and PNoise simulations of GRO.

For the designed W/L, average power consumed by each inverter cell is 82.81nW. Thus for the proposed 13 stages, total power consumption is 1.08μW which is practically very less. Figure 10 shows the layout for proposed 13 stage GRO. Post layout simulations on various parameters are compared against the pre layout simulation parameters. Table I presents this comparison. Process corners' analysis for post layout simulation, is summarized in the Table II. It shows the variations in GRO frequency, output power and total power dissipation against various process corners. Proposed GRO implementation achieves the highest oscillation frequency at "Fast_Best" corner and the lowest power dissipation at "slow_worst" corner.

The variations in frequency of oscillation for GRO with temperature are shown in Figure 11. It is done for both pre layout and post layout simulations. With the temperature variations from – 25^0C to 125^0C the frequency of oscillations decreases from 336.6 KHz to 223.4 KHz for pre layout simulations. For post layout simulations the frequency decreases from 297.6 KHz to 199.1 KHz.
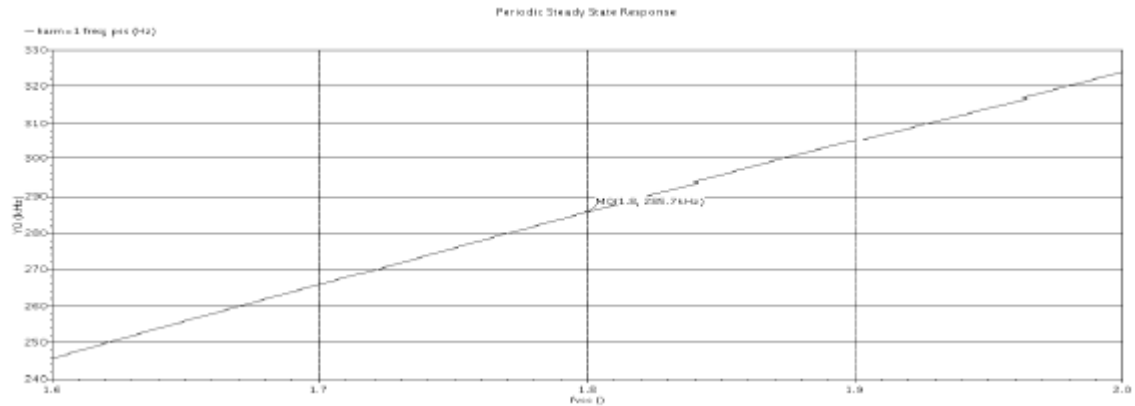
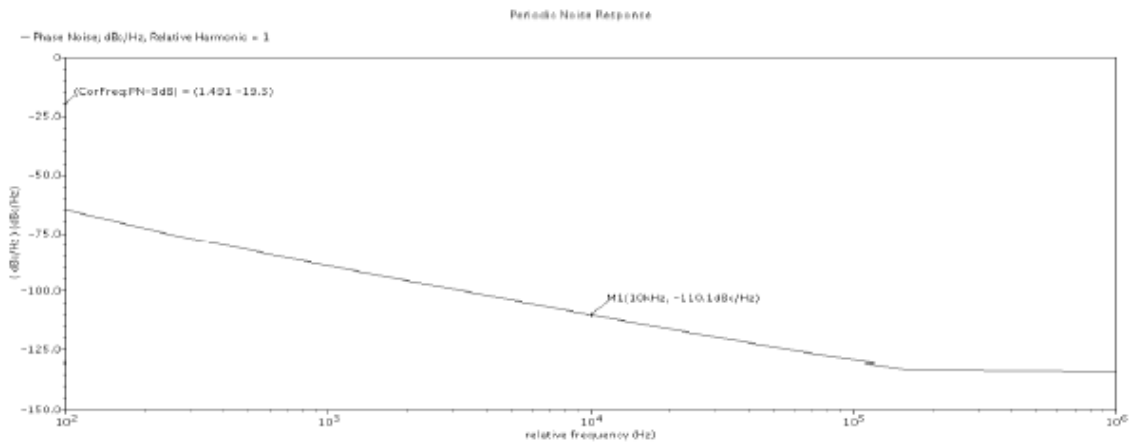Figure 8. Switching frequency variation with supply voltage variations

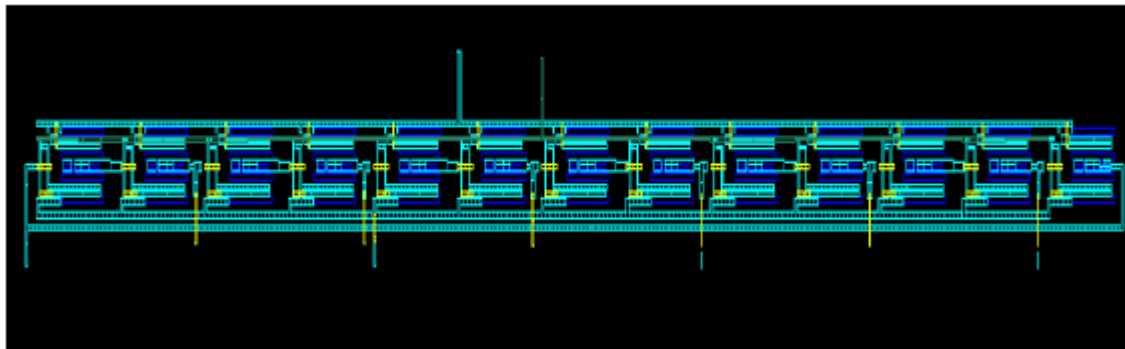

Figure 9. Measured Phase noise

Figure 10. Layout :13 Stage GRO

Table I. Pre Layout vs. Post Layout Simulation Results

Parameters / Layout	Pre – Layout	Post layout
f_{SW}	285.7kHz	253.3kHz
Phase Noise (at 10kHz offset)	-110dBc/Hz	-111.1dBc/Hz
Jitter (Cycle to Cycle)	327ps	1.193ns(rms)
Output Power	-12.08dBm(61.94μW)	-12.05dBm(62.37μW)
Total Power dissipated	-28.97dBm(1.26μW)	-29.01dBm(1.25μW)

Table II. Process Corners Analysis

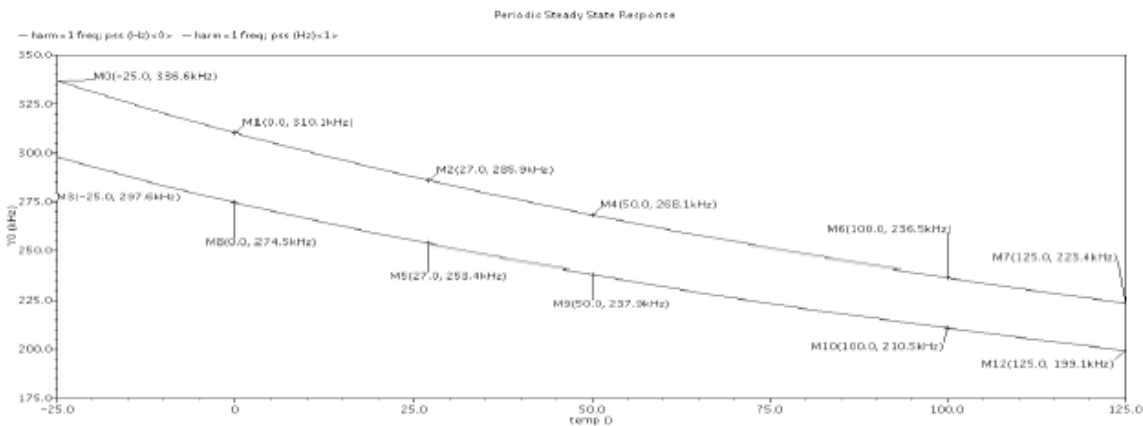| Parameters / Corners	Fast_Best	Fast_Slow	Slow_Fast	Typical	Slow_Worst
GRO Frequency	331kHz	34kHz	277.5kHz	254.8kHz	197.8kHz
Output Power	-12.07dBm	-12.07dBm	-12.02dBm	-12.05dBm	-12.02dBm
Total Power Dissipation	-27.55dBm	-29.29dBm	-28.68dBm	-28.99dBm	-30.42dBm

Figure 11. Frequency of Oscillation vs. Temperature

5. CONCLUSIONS

The proposed Gated Ring Oscillator (GRO) block designed for audio frequency range Asynchronous ADC is successfully implemented. GRO is required in TDC block to count the transitions during the specific measuring cycle. Proposed GRO uses the basic principle of gating functionality with the advantages like simplicity, low noise, minimum jitter, low power and reduced area as compared to the free running Ring Oscillators (RO). Conceptually GRO is the traditional Ring Oscillator (RO) with appended gating functionality. It uses Barrel-Shift Algorithm as well the delay element variance is also first-order noise shaped. This leads to about 40% to 70% gate count reduction compared to synchronous GRO-TDC. Significantly the GRO

holds its phase, during the two measurement intervals and achieves the first order noise shaping of the quantization error. Performance analysis also shows that it holds the preceding signal phase till the arrival of next signal. Thus provides first order noise shaping for calculated switching frequency with less jitter. To minimize the dynamic power GRO is deactivate during OFF period of a modulator without using any clock. Due to gating functionality dynamic power consumption is very less. Overall the proposed GRO shows expected performance for audio frequency range signal processing. Since it is simple, compact and efficient; can be exploited for a TDC block of Asynchronous ADC.

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