A NOVEL LOW POWER HIGH DYNAMIC THRESHOLD SWING LIMITED REPEATER INSERTION FOR ON-CHIP INTERCONNECTS

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ABSTRACT

In Very Large Scale Integration (VLSI), interconnect design has become a supreme issue in high speed ICs. With the decreased feature size of CMOS circuits, on-chip interconnect now dominates both circuit delay and power consumption. An eminent technique known as repeater/buffer insertion is used in long interconnections to reduce delay in VLSI circuits. This paper deals with some distinct low power alternative circuits in buffer insertion technique and it proposes two new techniques: Dynamic Threshold Swing Limited (DTSL) and High Dynamic Threshold Swing Limited (HDTSL). The DTSL uses Dynamic Threshold MOSFET configuration. In this gate is tied to the body and it limits the output swing. High Dynamic Threshold Swing Limited (HDTSL) also uses the same configuration along with a high threshold voltage(high-Vth). The simulation results are performed in Cadence virtuoso environment tool using 45nm technology. By simulating and comparing these various repeater circuits along with the proposed circuits it is analyzed that there is trade off among power, delay and Power Delay Product and the 34.66% of power is reduced by using the high- V_{th} in HDTSL when compared to DTSL.

KEYWORDS

Buffer Insertion, Boostable repeater, Swing Limited Interconnect circuit, Dynamic Threshold, Multi V_{th}

1. INTRODUCTION

In recent years, increasing prominence of portable system and the need to limit power consumption in very high density VLSI chips have led to rapid and innovative development in low-power. From the last few decades, the CMOS technology has emerged as a predominant technology in the field of nano electronics. As the technology has become compact there is rapid increase in demand of high performance and low power digital systems. The interconnect is a widely recognized cause of bottleneck in chip performance. Interconnect can no longer be seen as a simple resistor but the associated parasitics such as capacitance and inductance also need to be considered [1]. Thus any signal propagating through interconnect can be expected to be delayed. One popular technique that reduces the delay is buffer insertion.

1.1. Buffer Insertion

As the VLSI technology is being scaled to nanometer, interconnect delay has becoming a overriding constraint in the circuit design. The 50% of total path delay is exploited by interconnect delay. Buffer insertion/repeater technique [2] is very efficient one to reduce the

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delay over long interconnect. This technique is used to restore the signal strength in long interconnects. Various factors can deteriorate the signal performance in long interconnects, so repeater insertion is needed. The buffer insertion technique divides the long interconnect into equal smaller sections[3] and this is inserted between a driver and a receiver to drive each of these sections. So the total delay can be reduced by insertion of these repeaters along the interconnect wire length.

The paper is organised as follows. Section 2 explains various existing alternative circuits. They are as follows boostable repeater, schmitt trigger, transient sensitive accelerator (TSA), swing limited interconnect circuit (SLIC). Section 3 explains the proposed dynamic threshold swing limited (DTSL) and high dynamic threshold swing limited (HDTSL). The operation of these circuits is explained below in detail. These circuits are inserted in buffer insertion technique and outputs are analyzed. The simulation results for the existing and proposed circuits are performed for the various power supply and temperature variations are shown in section 4. By comparing the simulation results of these two proposed circuits it is observed that the HDTSL offer significant power savings upto 34.66% than DTSL. Finally Section 5 contains the conclusion.

2. CONVENTIONAL WORK

2.1. Boostable Repeater

In VLSI circuits the power efficiency is one of the main challenges as they are being scaled to nanometer regime. So due to this the process variations and aging may cause degradation to the circuits. Power consumption can be allocated uniformly across the fabricated instances during the design time only, although many instances may not have variations. To compensate these variations a circuit is used i.e., Adaptive circuit [4]. Adaptive design provides a power efficient approach to these variations; the power will be used only when the variations of circuit are harmful. So a new approach to fine grained voltage adaptation is Boostable Repeater [5]. Figure 1 shows the circuit diagram of Boostable Repeater. The main idea to introduce a Boostable repeater design is, it will increase its internal voltage rail momentarily to boost up the switching speed. The main advantage of using the Boostable repeater design is to achieve precise voltage adaptation without using any voltage regulators or any power grid. This is operated in two modes. (1) Boosting ON and (2) Boosting OFF. The boosting ON again consist of two phases (i) Charging Phase and (ii) Boosting phase [5]. In Boosting phase the capacitor gets discharged and it pulls up the output voltage. the boosting accelerates the rising transition of the output and hence it improves the switching speed.

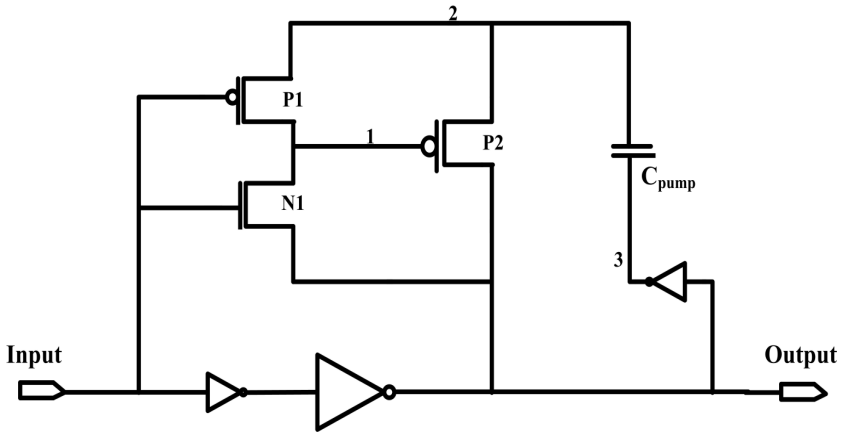


Figure 1. Boostable Repeater

2.2. CMOS Schmitt Trigger

In digital systems, the Schmitt trigger is one kind of regenerative circuit. The CMOS Schmitt triggers [6] are the circuit that converts the varying voltage to stable logic signal. The basic Schmitt trigger- inverter circuit is shown in the Figure 2. Schmitt triggers are usually used to generate fast transitions when a slowly varying function exceeds a predetermined level. The designed Schmitt trigger as a buffer is inserted at a higher frequency through an interconnect length in order to propagate the signal exactly from transmitting to receiving end so as to reduce the delay and power. Schmitt trigger switches faster when compared to ordinary CMOS buffer. Thus it leads to delay reduction.

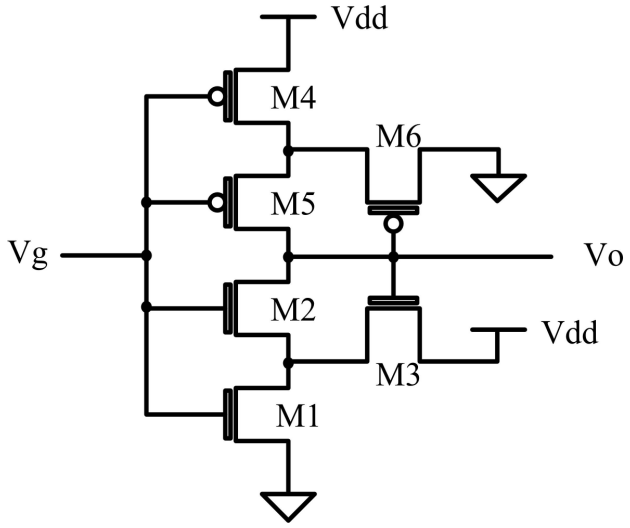


Figure 2. CMOS Schmitt Trigger

2.3. Transient Sensitive Accelerator

Transient sensitive Accelerator(TSA) is a circuit that used for highly resistive interconnects. The main advantage of TSA [8] is, it scales down both the delay time and cross talk voltages. Another advantage is that it can operate in self-time and can be applied to bidirectional signal communication. The circuit diagram of TSA is shown below as Figure 3. The TSA internally comprises of three sub-circuits: Transient Sensitive Trigger (TST), Clamp Transistors and Accelerator Transistors [8]. For the long interconnects the RC delay time can be reduced by using TST [7]. It changes its logical threshold voltage depending upon the input signal transition. This threshold voltage can be set to some constant value by decreasing the size of the transistors N1 and P1 or by increasing the size of the transistors N2 and P2. This results in fast detection of signal voltage transition. The lower half of the circuit consists of Schmitt trigger followed by an inverter. The interconnect voltage is assumed to have a long rise and fall time stemming from the large RC constant. The TST senses the transition at an early stage and the Schmitt trigger detects the change at the end of the transition. This timing difference in the sensing can be utilized as an acceleration period if the circuit turns ON during the interval. The clamp transistors and accelerator work alternatively. The clamp transistors work in the steady state and the accelerator transistors are turned ON during the transition interval. During the transition interval, the path through the clamp transistors gets disappears and accelerates the voltage transition. The main purpose of this circuit is to prevent TST from reacting to a small voltage fluctuations, it slightly delays the signal detection of the TST.

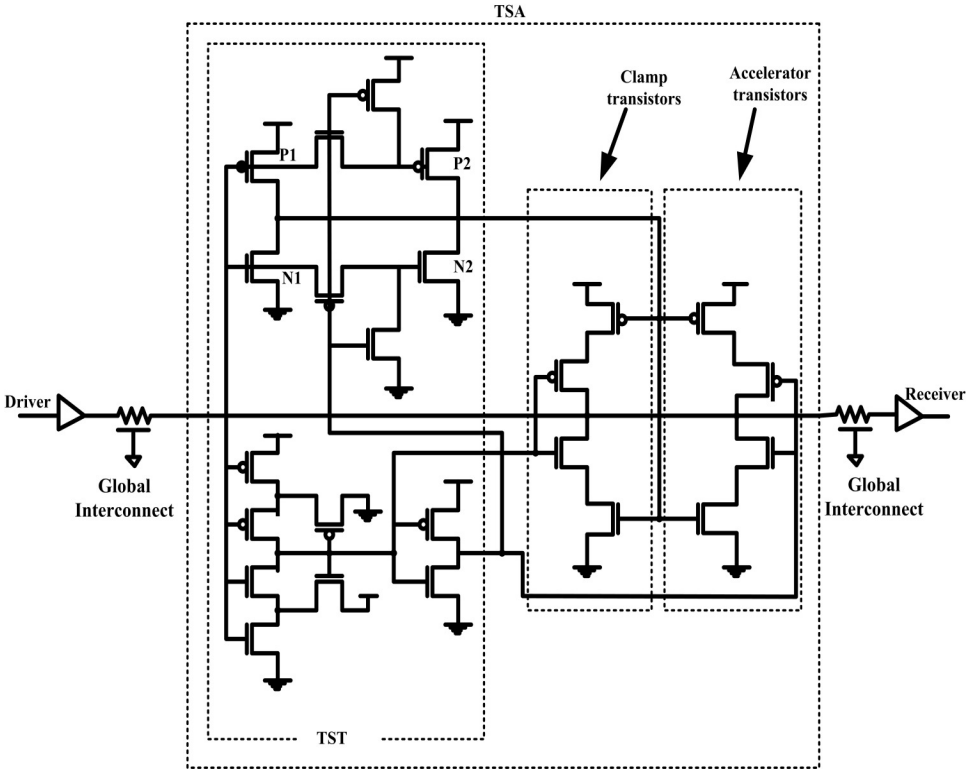


Figure 3. Transient Sensitive Trigger (TSA)

2.4. Swing Limited Interconnect Circuit

One of the solutions to achieve better energy efficiency is to reduce the swing voltage of the signal on the interconnect. The principal behind the low-swing techniques is the dependence of dynamic power on swing voltage. By the use of this results in reduced charging and discharging of interconnect capacitance. Reducing the swing voltage results in faster signalling method for on chip interconnects. The low swing interconnect architecture is presented in [9].

Swing Limited Interconnect circuit (SLIC) [10] mainly restricts the swing at the input. The output of interconnect is never allowed to its full rail. The circuit for SLIC is shown in figure 4. SLIC is a three stage cascaded inverter configuration with keeper transistors. M1 and M2 are the keeper transistors. The main function of the keeper transistors is to limit the swing from full rail to reduced rail. Inverter 1 acts as a level restoration circuit. It converts the input full rail voltage to reduced rail swing. This inverter also provides the necessary operating voltage for keeper transistors M1 and M2. The inverter 2 converts reduced signal swing to full rail. The NMOS is tied to Vdd and PMOS to ground. The main idea for this is to use them to hold inverter-1 input to just around the switching threshold. When the input is high, the output of inverter 1 is low, due to this the PMOS is turned ON and NMOS is turned OFF which pulls down the output of inverter 1. This output is pulled down below the midpoint of the supply voltage by the PMOS. After this point the PMOS automatically gets OFF and the NMOS is turned ON. This intern pulls the output of interconnect. Thus the output of interconnect in never allowed to discharge and charge to its full-rail.

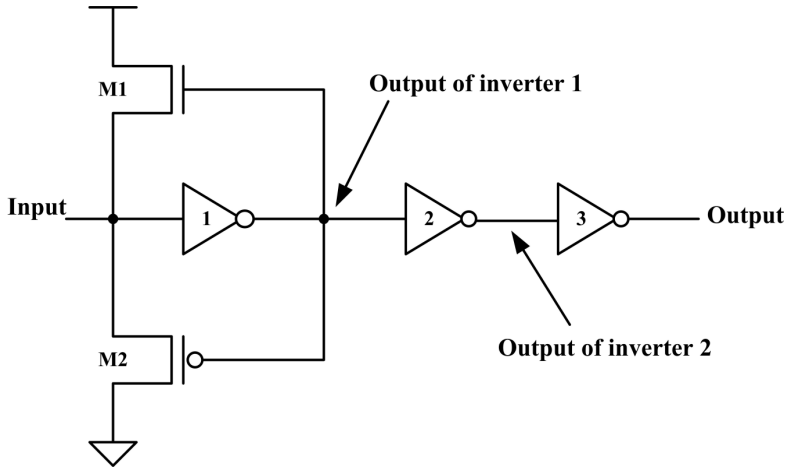


Figure 4. Swing Limited Interconnect Circuit (SLIC)

3. PROPOSED WORK

3.1. Dynamic Threshold Swing Limited

One of the most promising ways to attain both high speed and low power at low supply voltage is to vary threshold voltage of the MOSFETs. The configurations have been reported for many devices and circuits for variable voltage threshold. One is Dynamic Threshold MOSFET configuration (DTMOS) [11].

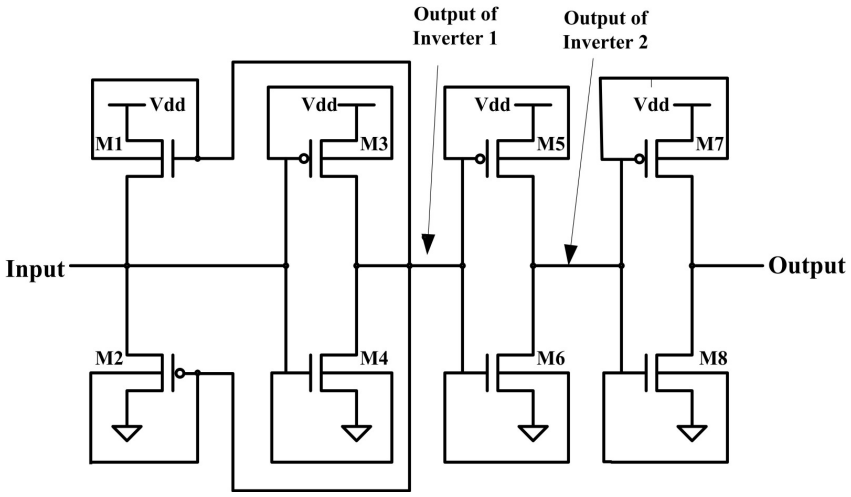


Figure 5. Dynamic Threshold Swing Limited (DTSL)

The dynamic power dissipation is marginal compared to speed enhancement. DTMOS has a nonzero static power dissipation component. This DTMOS contains the high V_t at zero bias and low V_t at $V_{gs}=V_{dd}$. The gate is tied to the body in the DTMOS. The DTMOS inverter is shown in[ ]. The Swing Limited Interconnect circuit is modified by using this dynamic threshold MOSFET forming a new circuit called Dynamic Threshold Swing Limited(DTSL). The circuit for DTSL is shown in Figure 5. This also uses the low-swing signalling technique. Several low- swing signalling schemes are proposed in[12]. The power consumption can be reduced by using this Dynamic Threshold MOSFETS. The operation of this circuit is that it limits the swing at the input along with dynamic threshold. This is due to the keeper transistors. The output of this is the

reduced rail when compared to the input. This designed DTSL is connected in buffer insertion technique with particular interconnect length.

3.2. High Dynamic Threshold Swing Limited

High-performance and low-power are the two main criteria in modern digital design. MTCMOS [13] is an effective circuit level technique. The performance and design is improved by utilizing high threshold voltage transistors. This technology is straight forward to use because existing designs can be easily be modified into MTCMOS blocks by simply adding high-V_{th} power supply, yet circuits can be easily placed in low leakage states at fine grain level of control. we assume that the values of the threshold voltages are specified by the process technology and cannot be variables in the optimization process[14]. This is usually true since the threshold voltage is very difficult to control accurately and the designers are not at the liberty of selecting a value that is not supported by the process. The goal of the selection process is to enable a subsequent power optimization of the circuit to reduce the dynamic component of the power dissipation. Henceforth, the low and high threshold voltage values will be called VtL and VtH , respectively, and the corresponding gates will be referred to as low-Vt and high-Vt gates, respectively

In this paper, HDTSL based on high-V_{th} CMOS technology is proposed. Keeper transistors are used which reduces the leakage current while saving exact logic state. The DTSL circuit is modified by using this high-V_{th} CMOS forming a new circuit called High Dynamic Threshold Swing Limited(HDTSL). The circuit for HDTSL is shown in Figure 6. This is also a three stage cascaded inverter but with high-V_{th}. Here M1 and M2 are the keeper transistors which limit the swing on the input. The operation is same as the DTSL but with the reduced power consumption. The proposed circuit maintains the lower power consumption characteristics as compared to the DTSL. This designed HDTSL is connected in buffer insertion technique with particular interconnect length.

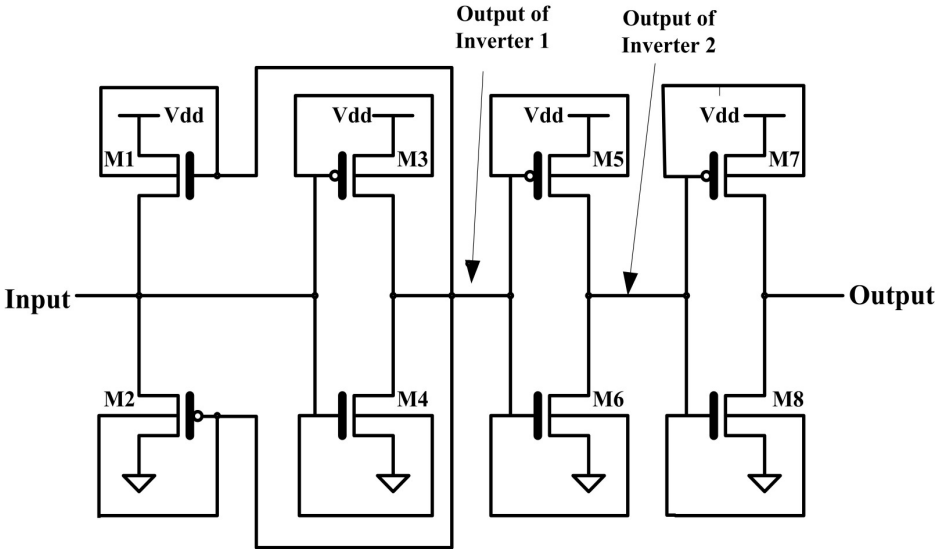


Figure 6. High Dynamic Threshold Swing Limited (HDTSL)

4. SIMULATION RESULTS

All the circuits are simulated in 45nm technology using Cadence Virtuoso tool. Power, delay and Power Delay Product (PDP) is compared for the various alternative repeaters. Table 1 shows the comparison results of various circuits' interms of power, delay and PDP. It shows that TSA

consumes less power when compared to other circuits. Table 2. shows Comparison of Power, delay and PDP for DTSL and HDTSL at 45nm technology. HDTSL consumes less power than the DTSL. Table 3. shows comparison of proposed DTSL and HDTSL circuits interms of power and delay with supply voltage variation at room temperature. Table 4. shows comparison of proposed DTSL and HDTSL circuits interms of power and delay with temperature variations operating at V_{dd}=1V.

Table 1. Comparison of Power, delay and PDP for various circuits at 45nm technology

Designs	**Power(µW)**	**Delay(ns)**	**PDP(fJ)**
Booster	11.09	0.26	2.88
Schmitt trigger	4.968	0.31	1.54
TSA	2.11	0.84	1.79
SLIC	6920	0.079	480

Table 2. Comparison of Power, delay and PDP for DTSL and HDTSL at 45nm technology

Designs	**Power(µW)**	**Delay(ns)**	**PDP(fJ)**
DTSL	116.8	0.19	22.19
HDTSL	76.31	0.28	21.63

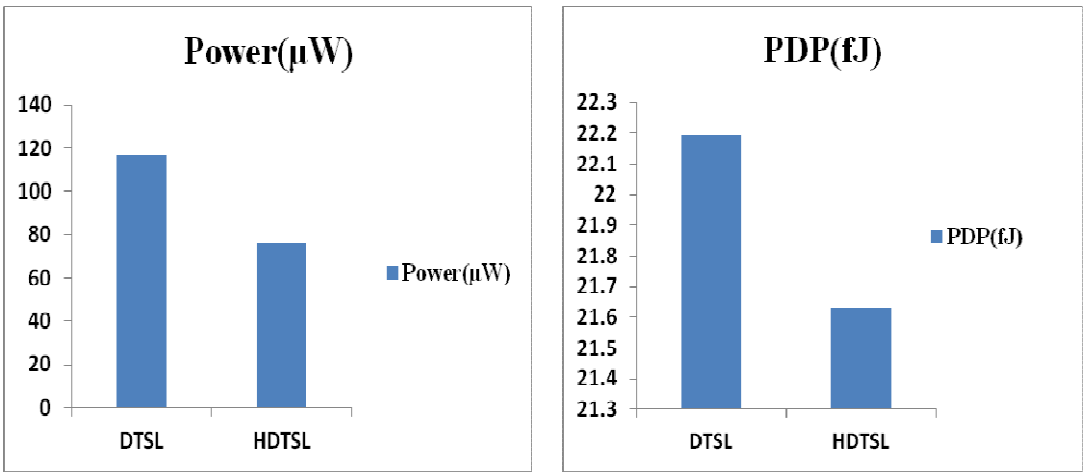
Table 3. Comparison of proposed DTSL and HDTSL circuits interms of power and delay with supply voltage variation at room temperature

Supply Voltage	**DTSL**		**HDTSL**	
	Power(µW)	**Delay(ns)**	**Power(µW)**	**Delay(ns)**
0.7V	103.5	0.23	58.93	0.35
0.8V	108.8	0.21	69.54	0.32
0.9V	112.4	0.20	73.86	0.30
1V	116.8	0.19	76.31	0.28
1.2V	122.2	0.18	80.72	0.27

Table 4. Comparison of proposed DTSL and HDTSL circuits interms of power and delay with temperature variations operating at V_{dd}=1V

Temperature	DTSL		HDTSL	
	Power(µW)	Delay(ns)	Power(µW)	Delay(ns)
-40°C	127.4	0.141	85.83	0.19
-27°C	127.3	0.149	85.49	0.21
0°C	124.3	0.158	82.66	0.24
27°C	116.8	0.19	76.31	0.28
40°C	111.2	0.20	72.32	0.31

The Supply voltage is varied ranging from 0.7V to 1.2V and observed that power increases as the supply voltage is increased and delay also is increased for both DTSL and HDTSL. The Temperature is varied from -40°C to 40°C and observed that the power increases as the voltage is increased and delay also increased for both the DTSL and HDTSL. There is a trade off between these Power, Delay and PDP. Figure 7. A) shows the histogram comparing the power for proposed DTSL and HDTSL. B) shows the histogram comparing the PDP for proposed DTSL and HDTSL. The power consumption is less for the HDTSL than the DTSL. So this HDTSL is power efficient. The PDP is also less for HDTSL. Figure 8. shows the simulation waveform of proposed HDTSL in Cadence Virtuoso using 45nm technology. By analyzing the result it can be observed that the output of interconnect is reduced rail when compared to input.



A) B)

Figure 7. A) Comparison of power consumption for DTSL and HDTSL

B) Comparison of PDP for DTSL and HDTSL

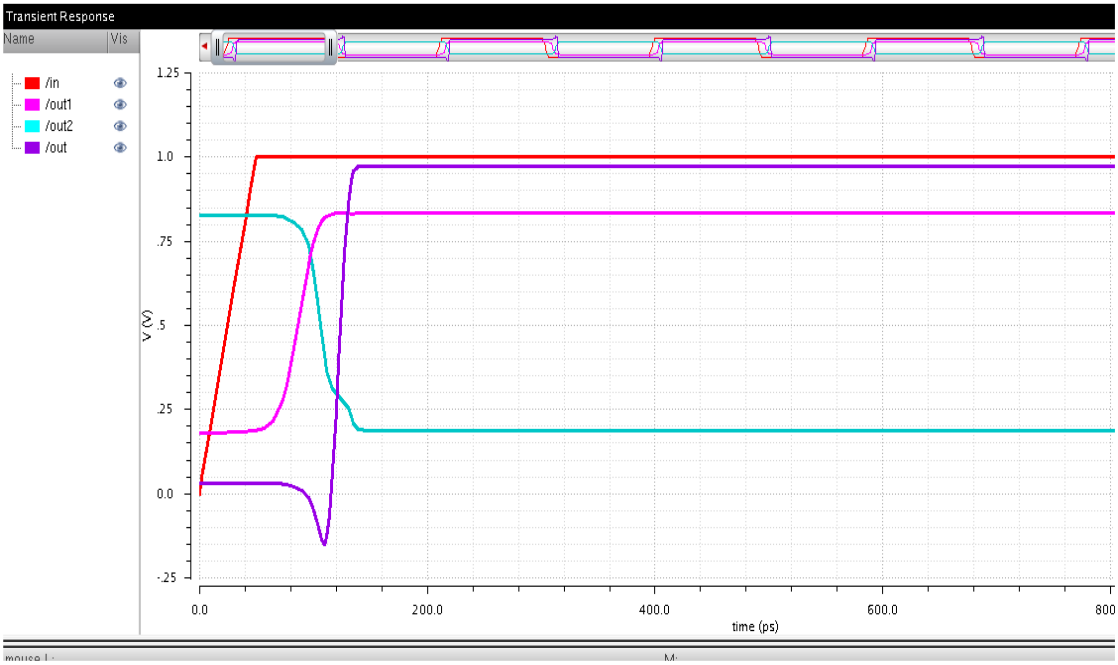
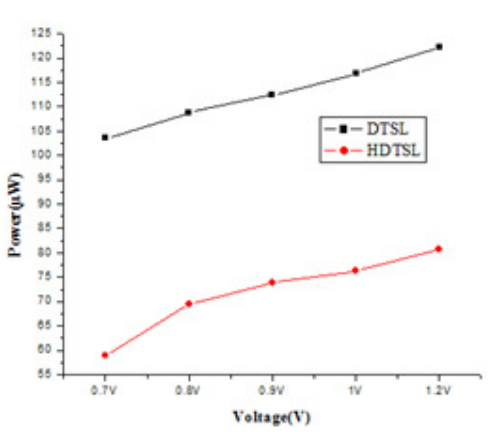
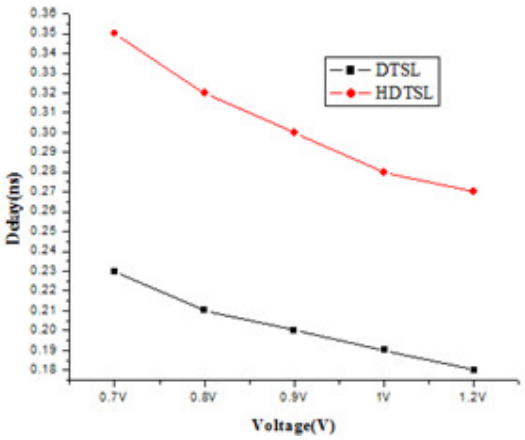


Figure 8. Simulation waveform of proposed HDTSL in Cadence Virtuoso using 45nm technology

The High Dynamic threshold swing limited interconnect system does not break interconnects. This system uses the receiver, reduces the voltage swing on interconnects from rail- to rail to a reduced rail. The waveform of SLIC is shown in figure 8. It can been observed that the output of interconnect is reduced rail as compared to the input. This is due to M1 and M2 transistors. The low swing at output of interconnect is restored to fully rail by the subsequent three inverters. Figure 9. A) shows the Power versus voltage variations B) shows the Delay versus Voltage variations C) shows the Power versus Temperature variations D) shows the Delay versus Temperature variations.



A)



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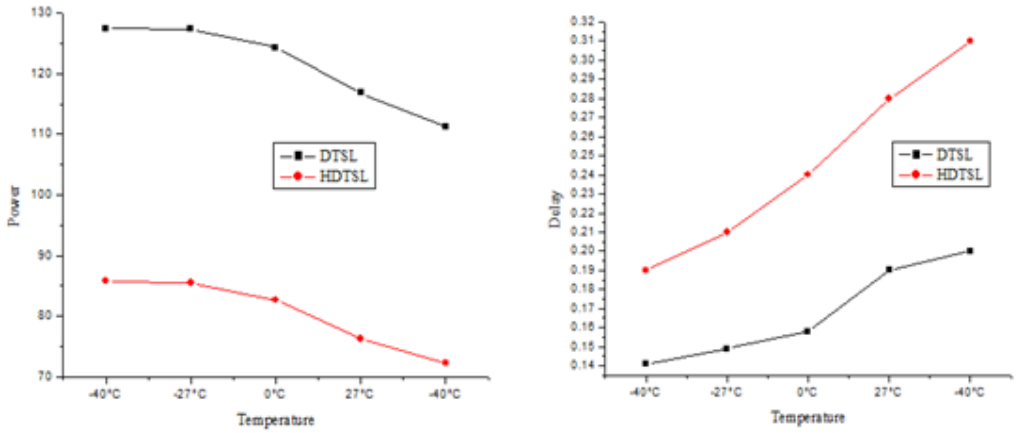

C) D)

Figure 9. A) Power versus Voltage variations B) Delay versus Voltage variations
C) Power versus Temperature variations D) Delay versus Temperature variations

5. CONCLUSIONS

The performance estimation of various existing alternative repeaters and proposed circuits are analyzed and compared for on-chip inter-connect system in Cadence Virtuoso tool using 45nm technology. From the simulation results it is analyzed that the proposed techniques output is the reduced rail when compared to the input. From comparisons table it is analyzed that booster as a buffer improves the switching speed than Schmitt trigger but the power gets reduced. TSA consumes less power when compared to Schmitt trigger. The delay of SLIC is very low but the power consumed is very high than the other two. So two new techniques are proposed. The proposed DTSL uses the Dynamic threshold technology, which consumes less power than SLIC. Another proposed HDTSL uses the high-Vth CMOS technology, which offer significant power savings upto 34.66% than DTSL. The Supply voltage is varied ranging from 0.7V to 1.2V are done and observed that power increases as the supply voltage is increased for both DTSL and HDTSL. The Temperature is varied from -40°C to 40°C and observed that the power increases as the voltage is increased for both the DTSL and HDTSL. There is a trade off between these Power, Delay and PDP. Hence HDTSL is both Power and Energy efficient when compared to DTSL.

REFERENCES

[1] Magdy A. El-Moursy & Eby G. Friedman, (2004) "Optimum wire sizing of RLC interconnect with repeaters", *in proc. INTEGRATION, the VLSI journal 38 205–225.*

[2] A. Mahesh Kumar, SreehariVeeramachaneni & M.B.Srinivas, (2010) "Alternative approach to Buffer Insertion for Delay and Power Reduction in VLSI Interconnects", *in proc* Center for VLSI and Embedded Systems Technologies, January.

[3] K. Banerjee Mehnotra, A.(2002), "A power optimal repeater insertion methodology for global interconnects in nanometer designs," *IEEE Trans. Electron Devices*, vol. 49, pp. 2001-2007.

[4] FarshadMoradi, Dag T. Wisland, Hamid Mahmoodi, Tuan Vu Cao, & MalihehZarreDooghabadi, (2009) "Adaptive Supply Voltage Circuit Using Body BiasTechnique" *in proc. 16th International Conference "Mixed Design of Integrated Circuits and Systems"*, June 25-27, pp. 215-219.

[5] Kyu-Nam shim & Jiang Hu, (2013)" Boostable Repeater design for variation Resilience in VLSI Interconnects" *in proc. IEEE Trans. Very Large Scale Integr(VLSI) syst.*, vol. 21,No. 9,sept pp1619-1631.

[6] **Saini.S,** (2009)"Schmitt Trigger as an alternative to Buffer Insertion for Delay and Power Reduction in VLSI Inter-connects", IEEE Region10Conference-TENCON.

[7] Hong-Yi Huang & Shih-Lun Chen, (2006) "High-Speed Transition Detecting Circuits for On-Chip Interconnections" *in proc Tamkang Journal of Science and Engineering,* Vol. 9, No 1, pp. 37_44.

[8] Iima, T., Mizuno, M., Horiuchi, T. & Yamashina,M., (1996) "Capacitor Coupling Immune, Transient SensitiveAccelerator for Resistive Interconnect Signals of Subquarter Micron ULSI," in proc. *IEEE J. Solid-State Circuits*, Vol. 31, pp531_536.

[9] Volkan Kurusun, Radu M.Secareanu and Eby G. Fredeman (2002) "Cmos voltage interface circuit for low power system." in proccedings of IEEE international Sympoism on circuits and systems, Vol 3, May pp 667-670.

[10] VishakVenkatraman, Mark Anders, HimanshuKaul, Wayne Burleson & Ram Krishnamurthy " A Low Swing Signalling Circuit Technique for 65-nm On Chip Interconnects" *in proc IEEE Soc Conference*, pp289 – 292.

[11] FariborzAssaderaghi, Dennis Sinitsky, Stephen A. Parke, Jeffrey Bokor, Ping K. Ko & Chenming Hu , (1997)"Dynamic Threshold-Voltage MOSFET(DTMOS) for Ultra-Low Voltage VLSI" *in proc IEEE Transactions On Electron Devices,* Vol. 44, No. 3, March pp 414-422.

[12] Zhang, H., George, V. and Rabaey, J. M., (2000) "Low-swing on-chip Signaling Techniques: Effectiveness and Robustness," *IEEE Trans. VLSI Systems*, Vol. 8, pp. 264_ 272.

[13] V. Kursun and E. G. Friedman, "Multi-Voltage CMOS Circuit Design." New York: Wiley, 2006

[14] P.Sreenivasulu, G.Vinatha, Dr. K.Srinivasa Rao, Dr. A.Vinaya babu, (2013) " Novel Ultra Low Power Multi-threshold CMOS Technology", *in proc International Journal of Advanced Research in Computer Science and Software Engg. 3(8),* August , pp 81-88.

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